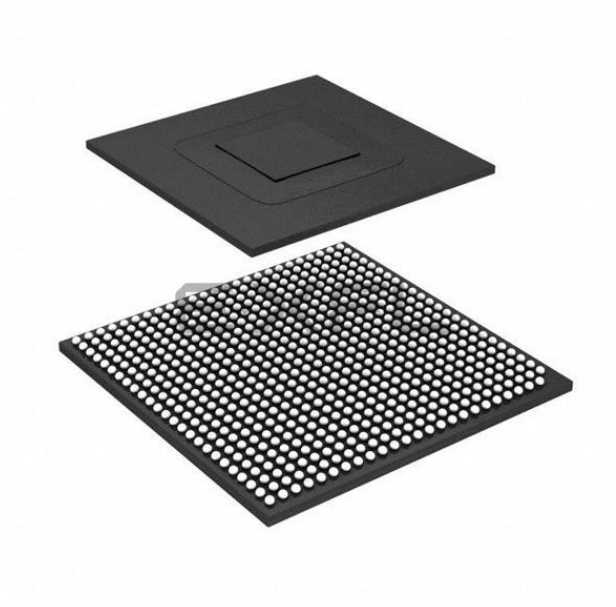

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6u6avm08ac

such as WLAN, Bluetooth™, GPS, hard drive, displays, and camera sensors.

The i.MX 6Solo/6DualLite processors are specifically useful for applications such as:

- Automotive navigation and entertainment
- Graphics rendering for Human Machine Interfaces (HMI)
- High-performance speech processing with large databases
- Audio playback
- Video processing and display

The i.MX 6Solo/6DualLite processors have some very exciting features, for example:

- Multilevel memory system—The multilevel memory system of each processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processors support many types of external memory devices, including DDR3, low voltage DDR3, LPDDR2, NOR Flash, PSRAM, cellular RAM, NAND Flash (MLC and SLC), OneNAND™, and managed NAND, including eMMC up to rev 4.4.
- Smart speed technology—The processors have power management throughout the IC that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product, requiring levels of power far lower than industry expectations.
- Dynamic voltage and frequency scaling—The processors improve the power efficiency of devices by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—The multimedia performance of each processor is enhanced by a multilevel cache system, Neon MPE (Media Processor Engine) co-processor, a multi-standard hardware video codec, an image processing unit (IPU), and a programmable smart DMA (SDMA) controller.
- Powerful graphics acceleration—Each processor provides two independent, integrated graphics processing units: an OpenGL® ES 2.0 3D graphics accelerator with a shader and a 2D graphics accelerator.
- Interface flexibility—Each processor supports connections to a variety of interfaces: LCD controller for up to two displays (including parallel display, HDMI1.4, MIPI display, and LVDS display), dual CMOS sensor interface (parallel or through MIPI), high-speed USB on-the-go with PHY, high-speed USB host with PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), 10/100/1000 Mbps Gigabit Ethernet controller, and a variety of other popular interfaces (such as UART, I^2C, and I^2S serial audio, and PCIe-II).
- Automotive environment support—Each processor includes interfaces, such as two CAN ports, an MLB150/50 port, an ESAI audio interface, and an asynchronous sample rate converter for multichannel/multisource audio.
- Advanced security—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features will be discussed in detail in the *i.MX 6Solo/6DualLite Security Reference Manual* (to be released soon).

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
512x8 Fuse Box	Electrical Fuse Array	Security	Electrical Fuse Array. Enables to setup Boot Modes, Security Levels, Security Keys, and many other system parameters. The i.MX 6Solo/6DualLite processors consist of 512x8-bit fuse fox accessible through OCOTP_CTRL interface.
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5 GPIO-6 GPIO-7	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.
GPMI	General Media Interface	Connectivity Peripherals	The GPMI module supports up to 8x NAND devices. 40-bit ECC encryption/decryption for NAND Flash controller (GPMI2). The GPMI supports separate DMA channels per NAND device.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU3Dv5	Graphics Processing Unit, ver.5	Multimedia Peripherals	The GPU3Dv5 provides hardware acceleration for 3D graphics algorithms with sufficient processor power to run desktop quality interactive graphics applications on displays up to HD1080 resolution. The GPU3D provides OpenGL ES 2.0, including extensions, OpenGL ES 1.1, and OpenVG 1.1
GPU2Dv2	Graphics Processing Unit-2D, ver 2	Multimedia Peripherals	The GPU2Dv2 provides hardware acceleration for 2D graphics algorithms, such as Bit BLT, stretch BLT, and many other 2D functions.
HDMI Tx	HDMI Tx i/f	Multimedia Peripherals	The HDMI module provides HDMI standard i/f port to an HDMI 1.4 compliant display.
HSI	MIPI HSI i/f	Connectivity Peripherals	The MIPI HSI provides a standard MIPI interface to the applications processor.
I^2C-1 I^2C-2 I^2C-3 I^2C-4	I^2C Interface	Connectivity Peripherals	I^2C provide serial interface for external devices. Data rates of up to 400 kbps are supported.

Table 23. OSC32K Main Characteristics

	Min	Typ	Max	Comments
Bias resistor		14 MΩ		This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amp. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.
Crystal Properties				
Cload		10 pF		Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR		50 kΩ	100 kΩ	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

4.6 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3 modes
- LVDS I/O
- MLB I/O

NOTE

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output.

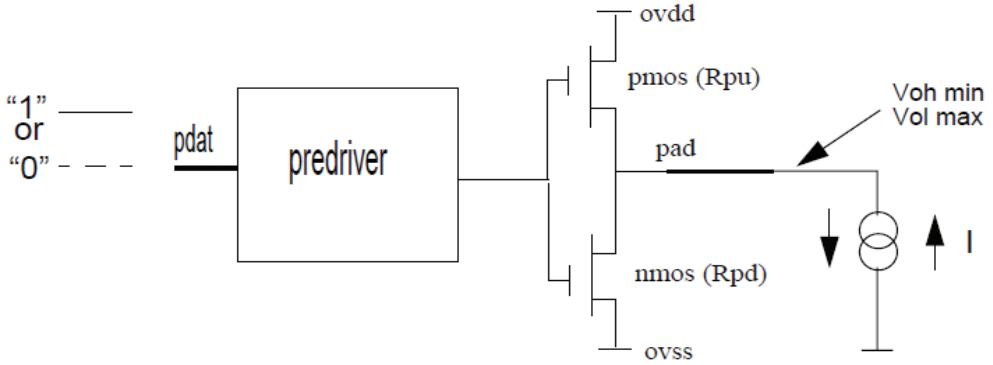

Figure 3. Circuit for Parameters Voh and Vol for I/O Cells

Table 27 shows the Low Voltage Differential Signaling (LVDS) I/O DC parameters.

Table 27. LVDS I/O DC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Differential Voltage	VOD	Rload-100 Ω Diff	250	350	450	mV
Output High Voltage	VOH	IOH = 0 mA	1.25	1.375	1.6	V
Output Low Voltage	VOL	IOL = 0 mA	0.9	1.025	1.25	V
Offset Voltage	VOS		1.125	1.2	1.375	V

4.6.4 MLB I/O DC Parameters

The MLB interface complies with Analog Interface of 6-pin differential Media Local Bus specification version 4.1. See 6-pin differential MLB specification v4.1, “MediaLB 6-pin interface Electrical Characteristics” for details.

NOTE

The MLB 6-pin interface does not support speed mode 8192 fs.

Table 28 shows the Media Local Bus (MLB) I/O DC parameters.

Table 28. MLB I/O DC Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Differential Voltage	VOD	Rload-50Ω Diff	300	500	mV
Output High Voltage	VOH	Rload-50Ω Diff	1.25	1.75	V
Output Low Voltage	VOL	Rload-50Ω Diff	0.75	1.25	V
Common-mode output voltage ((Vpadp*+Vpadn*)/2)	Vocm	Rload-50Ω Diff	1	1.5	V
Differential output impedance	Zo		1.6		kΩ

4.7 I/O AC Parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3/DDR3L modes
- LVDS I/O
- MLB I/O

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 4 and Figure 5.

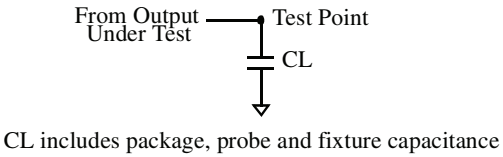

Figure 4. Load Circuit for Output

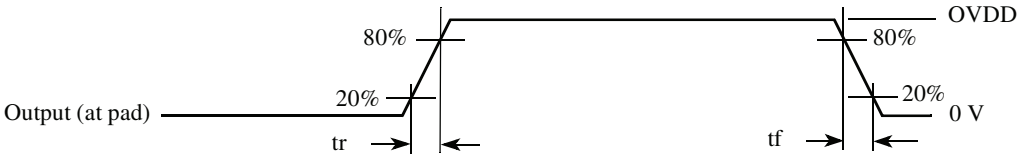

Figure 5. Output Transition Time Waveform

4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 29 and Table 30, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 29. General Purpose I/O AC Parameters 1.8 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=111)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.72/2.79 1.51/1.54	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.20/3.36 1.96/2.07	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=100)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.64/3.88 2.27/2.53	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	4.32/4.50 3.16/3.17	
Input Transition Times[1]	trm	—	—	—	25	ns

[1] Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 33 shows the AC parameters for LVDS I/O.

Table 33. I/O AC Parameters of LVDS Pad

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential pulse skew[1]	t_{SKD}	Rload = 100 Ω, Cload = 2 pF	—	—	0.25	ns
Transition Low to High Time[2]	t_{TLH}		—	—	0.5	
Transition High to Low Time[2]	t_{THL}		—	—	0.5	
Operating Frequency	f	—	—	600	800	MHz
Offset voltage imbalance	Vos	—	—	—	150	mV

1 t_{SKD} = | t_{PHLD} - t_{PLHD} |, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

2 Measurement levels are 20-80% from output voltage.

4.7.4 MLB I/O AC Parameters

The differential output transition time waveform is shown in Figure 7.

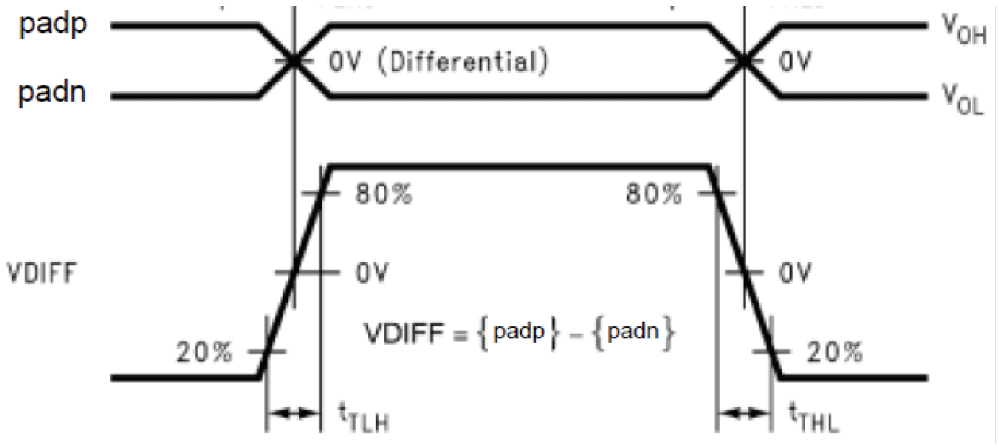

Figure 7. Differential MLB Driver Transition Time Waveform

A 4-stage pipeline is utilized in the MLB 6-pin implementation in order to facilitate design, maximize throughput, and allow for reasonable PCB trace lengths. Each cycle is one ipp_clk_in* (internal clock from MLB PLL) clock period. Cycles 2, 3, and 4 are MLB PHY related. Cycle 2 includes clock-to-output delay of Signal/Data sampling flip-flop and Transmitter, Cycle 3 includes clock-to-output delay of Signal/Data clocked receiver, Cycle 4 includes clock-to-output delay of Signal/Data sampling flip-flop.

MLB 6-pin pipeline diagram is shown in Figure 8.

4.9.2 WDOG Reset Timing Parameters

Figure 11 shows the WDOG reset timing and Table 40 lists the timing parameters.

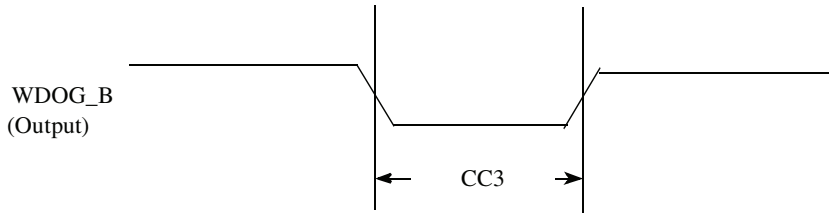

Figure 11. WDOG_B Timing Diagram

Table 40. WDOG_B Timing Parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WDOG_B Assertion	1	—	RTC_XTALI cycle

NOTE

RTC_XTALI is approximately 32 kHz. RTC_XTALI cycle is one period or approximately 30 µs.

NOTE

WDOG_B output signals (for each one of the Watchdog modules) do not have dedicated pins, but are muxed out through the IOMUX. See the IOMUX manual for detailed information.

4.9.3 External Interface Module (EIM)

The following subsections provide information on the EIM.

4.9.3.1 EIM Signal Cross Reference

Table 41 is a guide intended to help the user identify signals in the External Interface Module chapter of the reference manual that are identical to those mentioned in this data sheet.

Table 41. EIM Signal Cross Reference

Reference Manual EIM Chapter Nomenclature	Data Sheet Nomenclature, Reference Manual External Signals and Pin Multiplexing Chapter, and IOMUXC Controller Chapter Nomenclature
BCLK	EIM_BCLK
CSx_B	EIM_CSx
WE_B	EIM_RW
OE_B	EIM_OE
BEy_B	EIM_EBx

Table 43. EIM Bus Timing Parameters (continued)[1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE19	Input Data hold time from Clock rise	2	—	2	—	—	—	—	—
WE20	WAIT_B setup time to Clock rise	2	—	4	—	—	—	—	—
WE21	WAIT_B hold time from Clock rise	2	—	2	—	—	—	—	—

1 t is the maximal EIM logic (axi_clk) cycle time. The maximum allowed axi_clk frequency depends on the fixed/non-fixed latency configuration, whereas the maximum allowed BCLK frequency is:

—Fixed latency for both read and write is 132 MHz.

—Variable latency for read only is 132 MHz.

—Variable latency for write only is 52 MHz.

In variable latency configuration for write, if BCD = 0 & WBCDD = 1 or BCD = 1, axi_clk must be 104 MHz.Write BCD = 1 and 104 MHz axi_clk, will result in a BCLK of 52 MHz. When the clock branch to EIM is decreased to 104 MHz, other buses are impacted which are clocked from this source. See the CCM chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for a detailed clock tree description.

2 BCLK parameters are being measured from the 50% point, that is, high is defined as 50% of signal value and low is defined as 50% as signal value.

3 For signal measurements, “High” is defined as 80% of signal value and “Low” is defined as 20% of signal value.

Figure 14 to Figure 17 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

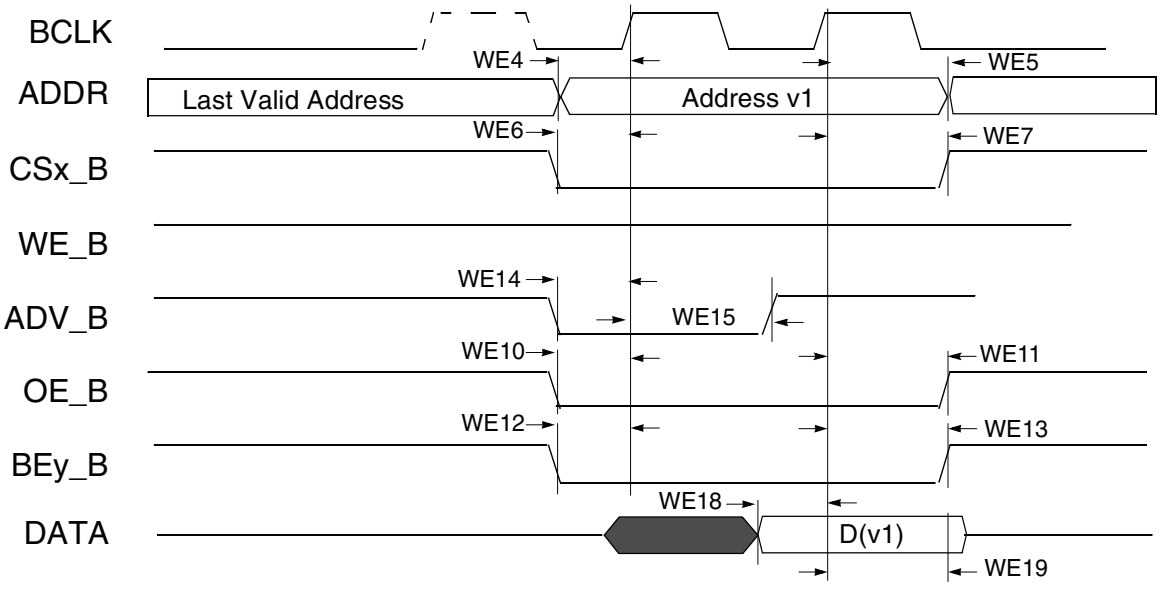

Figure 14. Synchronous Memory Read Access, WSC=1

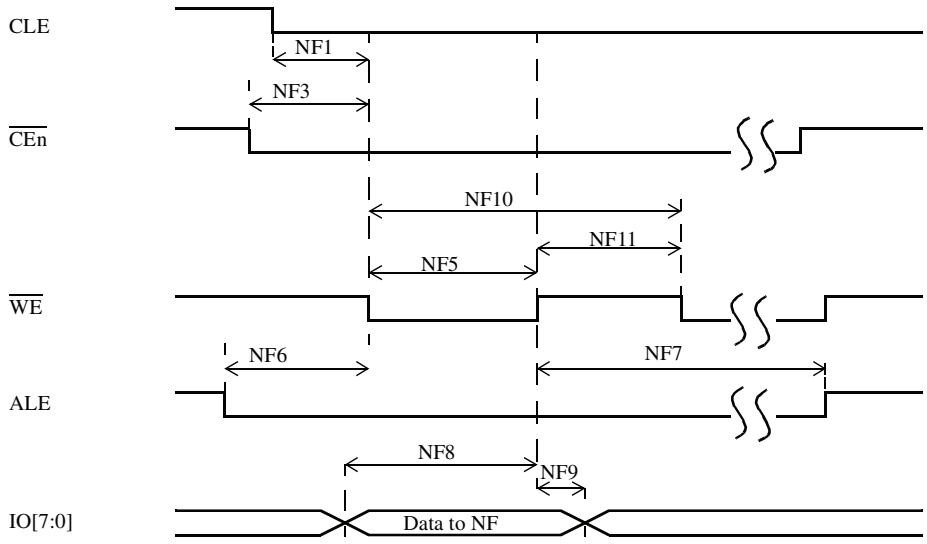

Figure 32. Write Data Latch Cycle Timing Diagram

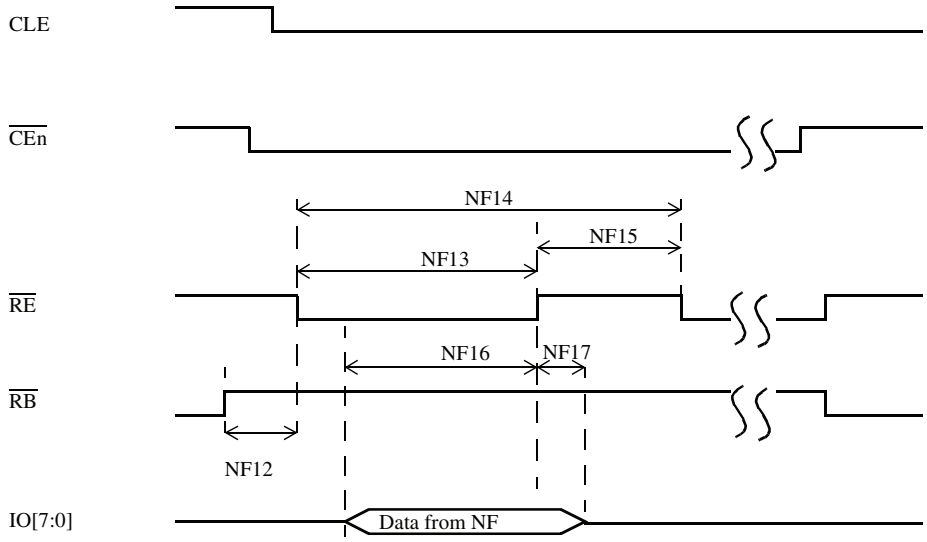

Figure 33. Read Data Latch Cycle Timing Diagram

Table 51. Asynchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Example Timing for GPMI Clock ≈ 100 MHz T = 10 ns		Unit
			Min.	Max.	Min.	Max.	
NF1	CLE setup time	tCLS	(AS+1) x T	—	10	—	ns
NF2	CLE hold time	tCLH	(DH+1) x T	—	20	—	ns
NF3	$\overline{\text{CE}}$n setup time	tCS	(AS+1) x T	—	10	—	ns
NF4	$\overline{\text{CE}}$ hold time	tCH	(DH+1) x T	—	20	—	ns

Table 51. Asynchronous Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Example Timing for GPMI Clock ≈ 100 MHz T = 10 ns		Unit
			Min.	Max.	Min.	Max.	
NF5	$\overline{WE}$ pulse width	tWP	DS x T		10		ns
NF6	ALE setup time	tALS	(AS+1) x T	—	10	—	ns
NF7	ALE hold time	tALH	(DH+1) x T	—	20	—	ns
NF8	Data setup time	tDS	DS x T	—	10	—	ns
NF9	Data hold time	tDH	DH x T	—	10	—	ns
NF10	Write cycle time	tWC	(DS+DH) x T		20		ns
NF11	$\overline{WE}$ hold time	tWH	DH x T		10		ns
NF12	Ready to $\overline{RE}$ low	tRR	(AS+1) x T	—	10	—	ns
NF13	$\overline{RE}$ pulse width	tRP	DS x T	—	10	—	ns
NF14	READ cycle time	tRC	(DS+DH) x T	—	20	—	ns
NF15	$\overline{RE}$ high hold time	tREH	DH x T		10	—	ns
NF16	Data setup on read	tDSR	N/A		10	—	ns
NF17	Data hold on read	tDHR	N/A		10	—	ns

1 GPMI's Async Mode output timing could be controlled by module's internal registers, say HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers' settings. In the above table, we use AS/DS/DH to represent each of these settings.

2) AS minimum value could be 0, while DS/DH minimum value is 1.

3) T represents for the GPMI clock period.

In EDO mode (Figure 33), NF16/NF17 are different from the definition in non-EDO mode (Figure 32). They are called tREA/tRHOH (RE# access time/RE# HIGH to output hold). The typical value for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI will sample IO[7:0] at rising edge of delayed RE provided by an internal DPLL. The delay value can be controlled by GPMI_CTRL1.RDN_DELAY (see the GPMI chapter of the i.MX 6Solo/6DualLite reference manual). The typical value of this control register is 0x8 at 50 MT/s EDO mode. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.11.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing, eMMC4.4 (Dual Date Rate) timing and SDR104/50(SD3.0) timing.

4.11.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 44 depicts the timing of SD/eMMC4.3, and Table 57 lists the SD/eMMC4.3 timing characteristics.

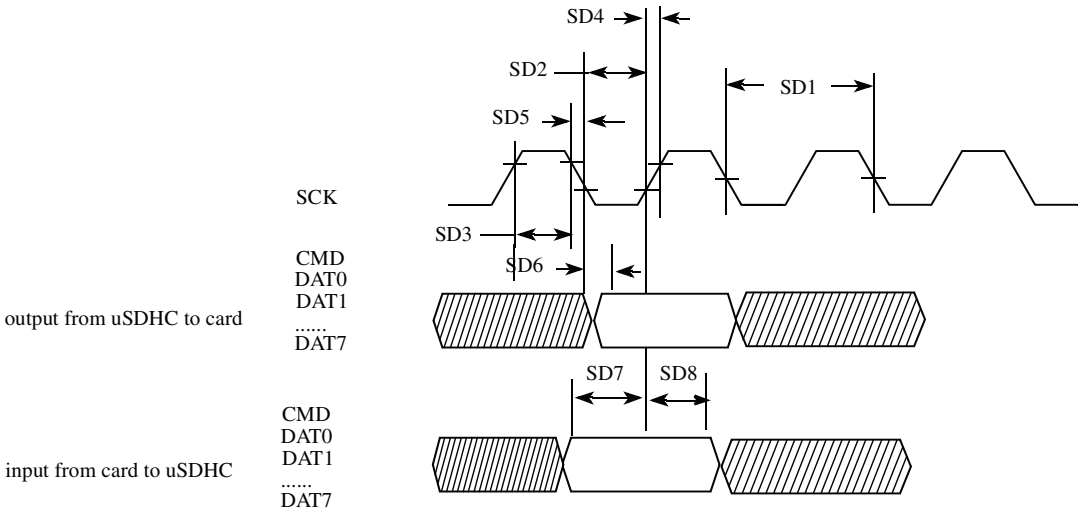

Figure 44. SD/eMMC4.3 Timing

Table 57. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
uSDHC Output/Card Inputs CMD, DAT (Reference to CLK)					
SD6	uSDHC Output Delay	t_{OD}	-6.6	3.6	ns

Figure 48 shows MII transmit signal timings. Table 61 describes the timing parameters (M5–M8) shown in the figure.

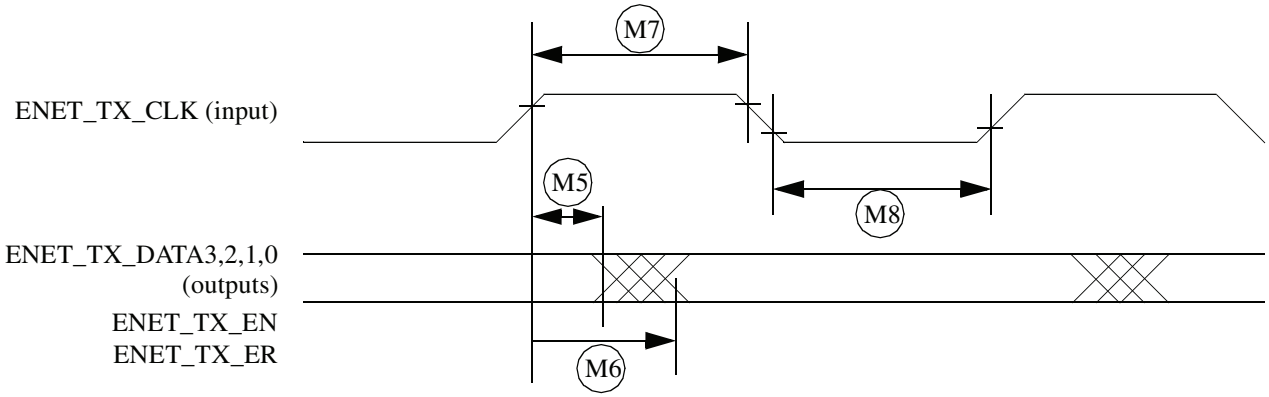

Figure 48. MII Transmit Signal Timing Diagram

Table 61. MII Transmit Signal Timing

ID	Characteristic[1]	Min.	Max.	Unit
M5	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER invalid	5	—	ns
M6	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER valid	—	20	ns
M7	ENET_TX_CLK pulse width high	35%	65%	ENET_TX_CLK period
M8	ENET_TX_CLK pulse width low	35%	65%	ENET_TX_CLK period

[1] ENET_TX_EN, ENET_TX_CLK, and ENET0_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

4.11.5.1.3 MII Asynchronous Inputs Signal Timing (ENET_CRS and ENET_COL)

Figure 49 shows MII asynchronous input timings. Table 62 describes the timing parameter (M9) shown in the figure.

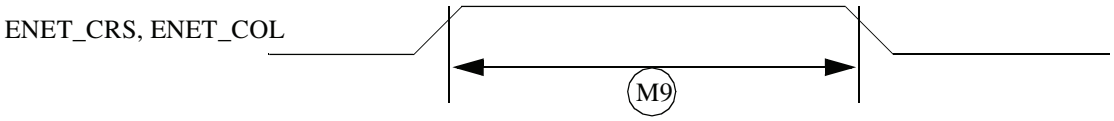

Figure 49. MII Async Inputs Timing Diagram

Table 62. MII Asynchronous Inputs Signal Timing

ID	Characteristic	Min.	Max.	Unit
M9[1]	ENET_CRS to ENET_COL minimum pulse width	1.5	—	ENET_TX_CLK period

[1] ENET_COL has the same timing in 10-Mbit 7-wire interface mode.

4.11.10.3 Electrical Characteristics

Figure 66 depicts the sensor interface timing. SENSB_MCLK signal described here is not generated by the IPU. Table 70 lists the sensor interface timing characteristics.

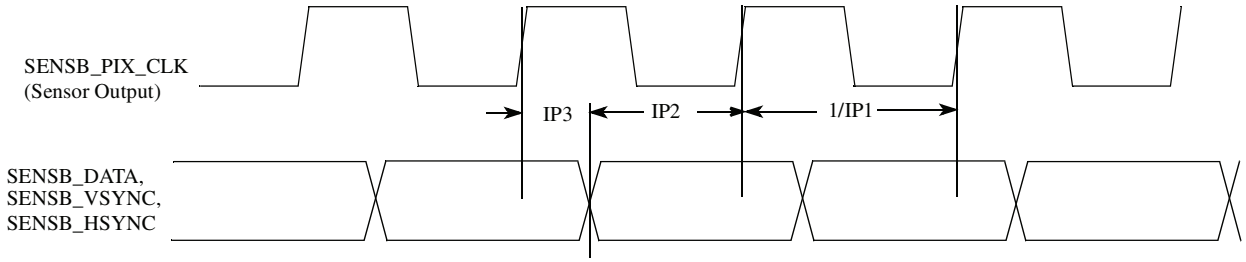

Figure 66. Sensor Interface Timing Diagram

Table 70. Sensor Interface Timing Characteristics

ID	Parameter	Symbol	Min	Max	Unit
IP1	Sensor output (pixel) clock frequency	Fpck	0.01	180	MHz
IP2	Data and control setup time	Tsu	2	—	ns
IP3	Data and control holdup time	Thd	1	—	ns

4.11.10.4 IPU Display Interface Signal Mapping

The IPU supports a number of display output video formats. Table 71 defines the mapping of the Display Interface Pins used during various supported video interface formats.

NOTE

Table 71 provides information for both the Disp0 and Disp1 ports. However, Disp1 port has reduced pinout depending on IOMUXC configuration and therefore may not support all the above configurations. See the IOMUXC table for details.

4.11.10.5 IPU Display Interface Timing

The IPU Display Interface supports two kinds of display accesses: synchronous and asynchronous. There are two groups of external interface pins to provide synchronous and asynchronous controls accordantly.

4.11.10.5.1 Synchronous Controls

The synchronous control changes its value as a function of a system or of an external clock. This control has a permanent period and a permanent wave form.

There are special physical outputs to provide synchronous controls:

- The ipp_disp_clk is a dedicated base synchronous signal that is used to generate a base display (component, pixel) clock for a display.
- The ipp_pin_1– ipp_pin_7 are general purpose synchronous pins, that can be used to provide HSYNC, VSYNC, DRDY or any else independent signal to a display.

The IPU has a system of internal binding counters for internal events (such as, HSYNC/VSYCN) calculation. The internal event (local start point) is synchronized with internal DI_CLK. A suitable control starts from the local start point with predefined UP and DOWN values to calculate control's changing points with half DI_CLK resolution. A full description of the counters system can be found in the IPU chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)*.

4.11.10.5.2 Asynchronous Controls

The asynchronous control is a data-oriented signal that changes its value with an output data according to additional internal flags coming with the data.

There are special physical outputs to provide asynchronous controls, as follows:

- The ipp_d0_cs and ipp_d1_cs pins are dedicated to provide chip select signals to two displays.
- The ipp_pin_11– ipp_pin_17 are general purpose asynchronous pins, that can be used to provide WR. RD, RS or any other data oriented signal to display.

NOTE

The IPU has independent signal generators for asynchronous signals toggling. When a DI decides to put a new asynchronous data in the bus, a new internal start (local start point) is generated. The signals generators calculate predefined UP and DOWN values to change pins states with half DI_CLK resolution.

The maximal accuracy of UP/DOWN edge of IPP_DATA is:

$$Accuracy = T_{diclk} \pm 0.62ns$$

The DISP_CLK_PERIOD, DI_CLK_PERIOD parameters are programmed through the registers.

Figure 70 depicts the synchronous display interface timing for access level. The DISP_CLK_DOWN and DISP_CLK_UP parameters are set through the Register. Table 73 lists the synchronous display interface timing characteristics.

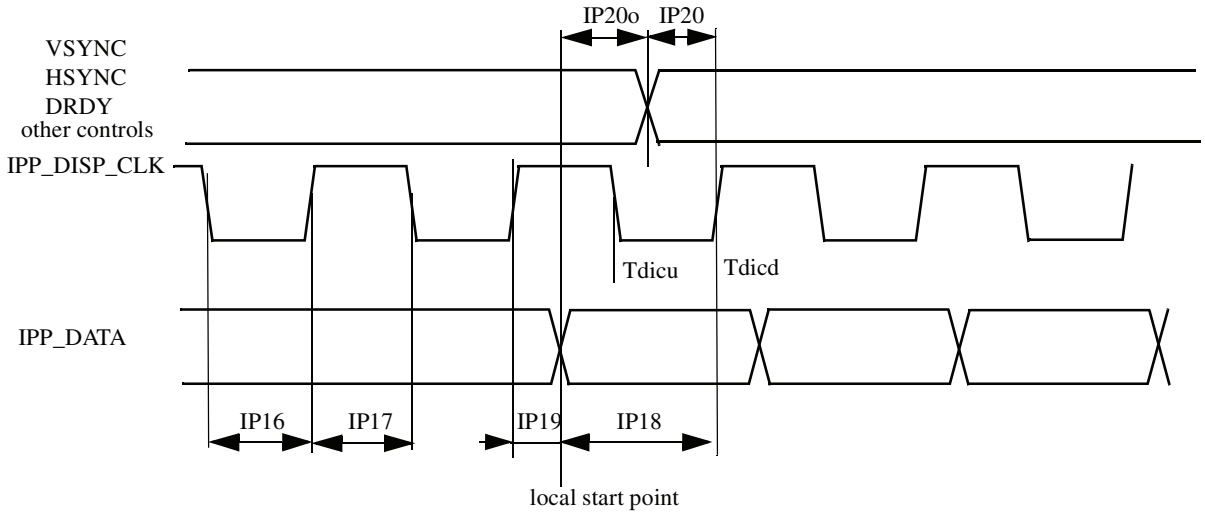

Figure 70. Synchronous Display Interface Timing Diagram—Access Level

Table 73. Synchronous Display Interface Timing Characteristics (Access Level)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP16	Display interface clock low time	Tckl	Tdicd-Tdicu-1.24	Tdicd[2]-Tdicu[3]	Tdicd-Tdicu+1.24	ns
IP17	Display interface clock high time	Tckh	Tdicp-Tdicd+Tdicu-1.24	Tdicp-Tdicd+Tdicu	Tdicp-Tdicd+Tdicu+1.2	ns
IP18	Data setup time	Tdsu	Tdicd-1.24	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp-Tdicd-1.24	Tdicp-Tdicu	—	ns
IP20o	Control signals offset times (defines for each pin)	Tocsu	Tocsu-1.24	Tocsu	Tocsu+1.24	ns
IP20	Control signals setup time to display interface clock (defines for each pin)	Tcsu	Tdicd-1.24-Tocsu%Tdicp	Tdicu	—	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

[2] Display interface clock down time

$$Tdicd = \frac{1}{2}\left(T_{diclk} \times ceil\left[\frac{2 \times DISP\_CLK\_DOWN}{DI\_CLK\_PERIOD}\right]\right)$$

4.11.12.2 MIPI D-PHY Signaling Levels

The signal levels are different for differential HS mode and single-ended LP mode. Figure 71 shows both the HS and LP signal levels on the left and right sides, respectively. The HS signaling levels are below the LP low-level input threshold such that LP receiver always detects low on HS signals.

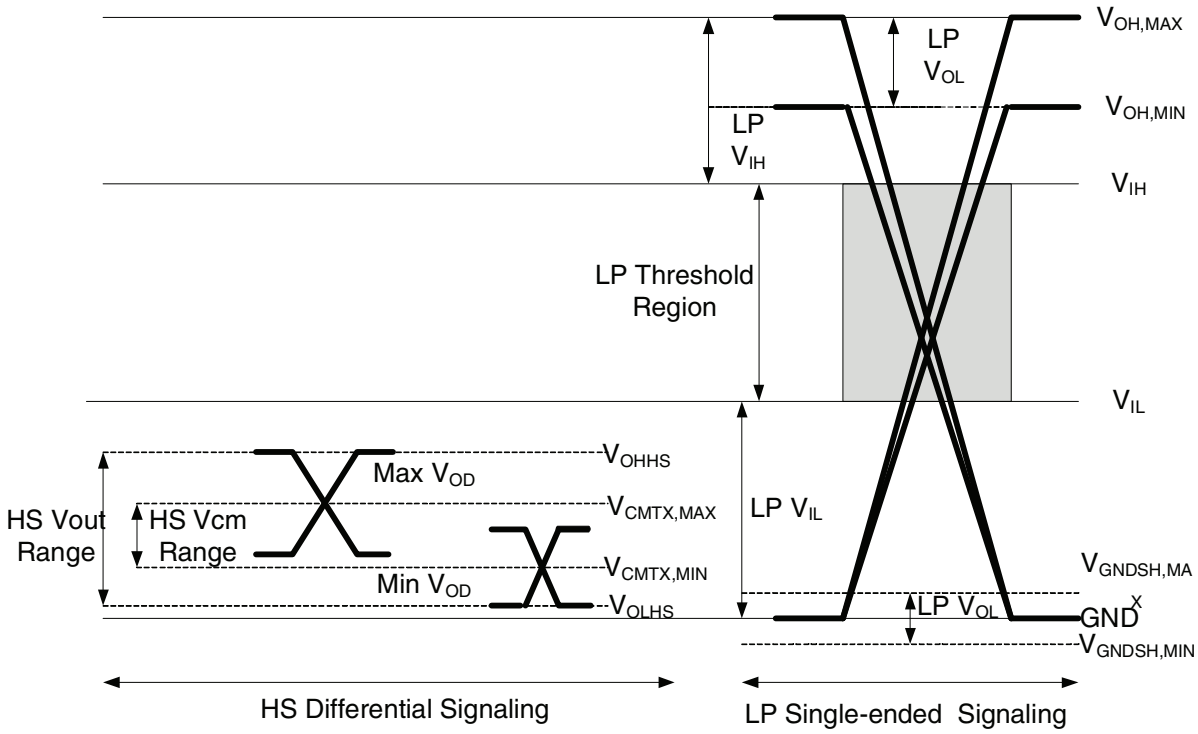

Figure 71. D-PHY Signaling Levels

4.11.12.3 MIPI HS Line Driver Characteristics

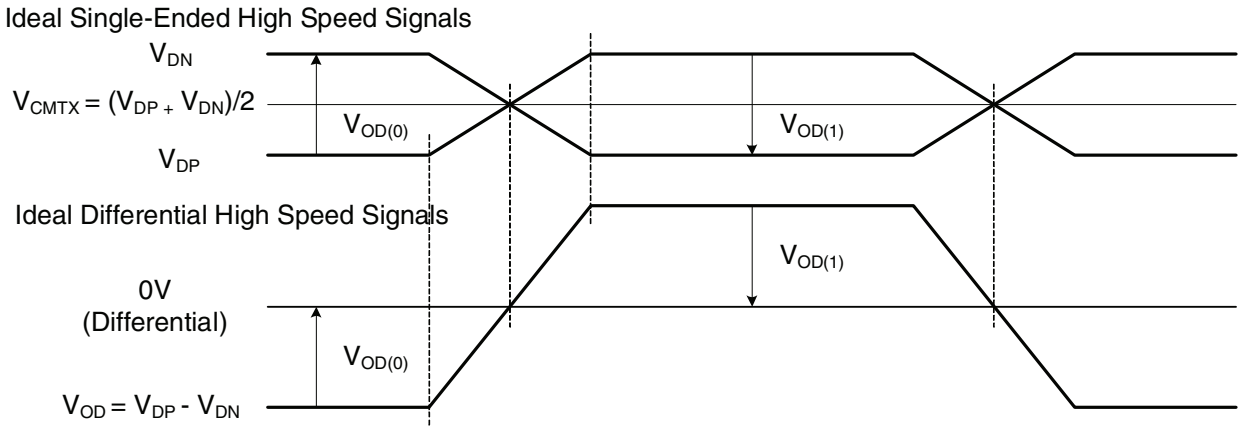

Figure 72. Ideal Single-ended and Resulting Differential HS Signals

Table 76. Electrical and Timing Information

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	Unit
$\Delta V_{CMTX(LF)}$	Common level variation between 50 MHz and 450 MHz.	80 Ω<= RL< = 125 Ω			25	mV_p
LP Line Drivers AC Specifications						
t_{rlp}, t_{flp}	Single ended output rise/fall time	15% to 85%, C_L<70 pF			25	ns
t_{reo}		30% to 85%, C_L<70 pF			35	ns
$\delta V/\delta t_{SR}$	Signal slew rate	15% to 85%, C_L<70 pF			120	mV/ns
C_L	Load capacitance		0		70	pF
HS Line Receiver AC Specifications						
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz				200	mVpp
$\Delta V_{CMRX(LF)}$	Common mode interference between 50 MHz and 450 MHz.		-50		50	mVpp
C_{CM}	Common mode termination				60	pF
LP Line Receiver AC Specifications						
e_{SPIKE}	Input pulse rejection				300	Vps
T_{MIN}	Minimum pulse response		50			ns
V_{INT}	Pk-to-Pk interference voltage				400	mV
f_{INT}	Interference frequency		450			MHz
Model Parameters used for Driver Load switching performance evaluation						
C_{PAD}	Equivalent Single ended I/O PAD capacitance.				1	pF
C_{PIN}	Equivalent Single ended Package + PCB capacitance.				2	pF
L_S	Equivalent wire bond series inductance				1.5	nH
R_S	Equivalent wire bond series resistance				0.15	Ω
R_L	Load resistance		80	100	125	Ω

4.11.12.6 High-Speed Clock Timing

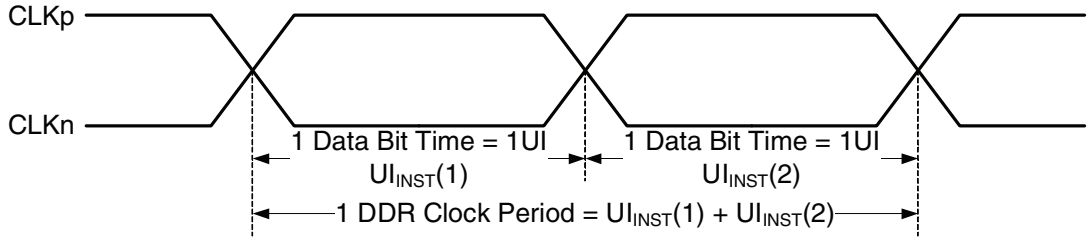

Figure 74. DDR Clock Definition

Table 101. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
CSI0_DAT6	N4	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[24]	Input	100 kΩ pull-up
CSI0_DAT7	N3	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[25]	Input	100 kΩ pull-up
CSI0_DAT8	N6	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[26]	Input	100 kΩ pull-up
CSI0_DAT9	N5	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[27]	Input	100 kΩ pull-up
CSI0_DATA_EN	P3	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[20]	Input	100 kΩ pull-up
CSI0_MCLK	P4	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[19]	Input	100 kΩ pull-up
CSI0_PIXCLK	P1	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[18]	Input	100 kΩ pull-up
CSI0_VSYNC	N2	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[21]	Input	100 kΩ pull-up
DI0_DISP_CLK	N19	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[16]	Input	100 kΩ pull-up
DI0_PIN15	N21	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[17]	Input	100 kΩ pull-up
DI0_PIN2	N25	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[18]	Input	100 kΩ pull-up
DI0_PIN3	N20	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[19]	Input	100 kΩ pull-up
DI0_PIN4	P25	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[20]	Input	100 kΩ pull-up
DISP0_DAT0	P24	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[21]	Input	100 kΩ pull-up
DISP0_DAT1	P22	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[22]	Input	100 kΩ pull-up
DISP0_DAT10	R21	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[31]	Input	100 kΩ pull-up
DISP0_DAT11	T23	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[5]	Input	100 kΩ pull-up
DISP0_DAT12	T24	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[6]	Input	100 kΩ pull-up
DISP0_DAT13	R20	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[7]	Input	100 kΩ pull-up
DISP0_DAT14	U25	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[8]	Input	100 kΩ pull-up
DISP0_DAT15	T22	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[9]	Input	100 kΩ pull-up
DISP0_DAT16	T21	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[10]	Input	100 kΩ pull-up
DISP0_DAT17	U24	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[11]	Input	100 kΩ pull-up
DISP0_DAT18	V25	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[12]	Input	100 kΩ pull-up
DISP0_DAT19	U23	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[13]	Input	100 kΩ pull-up
DISP0_DAT2	P23	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[23]	Input	100 kΩ pull-up
DISP0_DAT20	U22	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[14]	Input	100 kΩ pull-up
DISP0_DAT21	T20	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[15]	Input	100 kΩ pull-up
DISP0_DAT22	V24	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[16]	Input	100 kΩ pull-up
DISP0_DAT23	W24	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[17]	Input	100 kΩ pull-up

Table 101. 21 x 21 mm Functional Contact Assignments[1] (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value
DRAM_D12	AB5	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[12]	Input	100 kΩ pull-up
DRAM_D13	AC5	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[13]	Input	100 kΩ pull-up
DRAM_D14	AB6	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[14]	Input	100 kΩ pull-up
DRAM_D15	AC7	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[15]	Input	100 kΩ pull-up
DRAM_D16	AB7	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[16]	Input	100 kΩ pull-up
DRAM_D17	AA8	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[17]	Input	100 kΩ pull-up
DRAM_D18	AB9	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[18]	Input	100 kΩ pull-up
DRAM_D19	Y9	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[19]	Input	100 kΩ pull-up
DRAM_D2	AC4	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[2]	Input	100 kΩ pull-up
DRAM_D20	Y7	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[20]	Input	100 kΩ pull-up
DRAM_D21	Y8	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[21]	Input	100 kΩ pull-up
DRAM_D22	AC8	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[22]	Input	100 kΩ pull-up
DRAM_D23	AA9	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[23]	Input	100 kΩ pull-up
DRAM_D24	AE9	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[24]	Input	100 kΩ pull-up
DRAM_D25	Y10	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[25]	Input	100 kΩ pull-up
DRAM_D26	AE11	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[26]	Input	100 kΩ pull-up
DRAM_D27	AB11	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[27]	Input	100 kΩ pull-up
DRAM_D28	AC9	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[28]	Input	100 kΩ pull-up
DRAM_D29	AD9	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[29]	Input	100 kΩ pull-up
DRAM_D3	AA5	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[3]	Input	100 kΩ pull-up
DRAM_D30	AD11	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[30]	Input	100 kΩ pull-up
DRAM_D31	AC11	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[31]	Input	100 kΩ pull-up
DRAM_D32	AA17	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[32]	Input	100 kΩ pull-up
DRAM_D33	AA18	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[33]	Input	100 kΩ pull-up
DRAM_D34	AC18	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[34]	Input	100 kΩ pull-up
DRAM_D35	AE19	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[35]	Input	100 kΩ pull-up
DRAM_D36	Y17	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[36]	Input	100 kΩ pull-up
DRAM_D37	Y18	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[37]	Input	100 kΩ pull-up
DRAM_D38	AB19	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[38]	Input	100 kΩ pull-up
DRAM_D39	AC19	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[39]	Input	100 kΩ pull-up

Table 102. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

R	P	N	M	L	K	J	H
GPIO_17	CSI0_PIXCLK	CSI0_DAT4	CSI0_DAT10	CSI0_DAT13	HDMI_HPD	HDMI_REF	DSI_D1P
GPIO_16	CSI0_DAT5	CSI0_VSYNC	CSI0_DAT12	GND	HDMI_DDCCEC	GND	DSI_D1M
GPIO_7	CSI0_DATA_EN	CSI0_DAT7	CSI0_DAT11	CSI0_DAT17	HDMI_D2M	HDMI_D1M	DSI_CLK0M
GPIO_5	CSI0_MCLK	CSI0_DAT6	CSI0_DAT14	CSI0_DAT16	HDMI_D2P	HDMI_D1P	DSI_CLK0P
GPIO_8	GPIO_19	CSI0_DAT9	CSI0_DAT15	GND	HDMI_D0M	HDMI_CLKM	JTAG_TCK
GPIO_4	GPIO_18	CSI0_DAT8	CSI0_DAT18	CSI0_DAT19	HDMI_D0P	HDMI_CLKP	JTAG_MOD
GPIO_3	NVCC_GPIO	NVCC_CSI	HDMI_VPH	HDMI_VP	NVCC_MIPI	NVCC_JTAG	PCIE_VP
GND	GND	GND	GND	GND	GND	GND	GND
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDHIGH_IN	VDDHIGH_IN
VDDSOC_CAP	GND	GND	GND	GND	GND	VDDHIGH_CAP	VDDHIGH_CAP
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
GND	GND	NC	GND	GND	GND	GND	GND
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN
GND	GND	GND	GND	GND	GND	GND	GND
VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN
GND	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP
NVCC_DRAM	GND	GND	GND	GND	GND	GND	GND
NVCC_ENET	NVCC_LCD	DI0_DISP_CLK	NVCC_EIM	NVCC_EIM	NVCC_EIM	EIM_D29	EIM_A25
DISP0_DAT13	DISP0_DAT4	DI0_PIN3	EIM_DA11	EIM_DA0	EIM_RW	EIM_D30	EIM_D21
DISP0_DAT10	DISP0_DAT3	DI0_PIN15	EIM_DA9	EIM_DA2	EIM_EB0	EIM_A23	EIM_D31
DISP0_DAT8	DISP0_DAT1	EIM_BCLK	EIM_DA10	EIM_DA4	EIM_LBA	EIM_A18	EIM_A20
DISP0_DAT6	DISP0_DAT2	EIM_DA14	EIM_DA13	EIM_DA5	EIM_EB1	EIM_CS1	EIM_A21
DISP0_DAT7	DISP0_DAT0	EIM_DA15	EIM_DA12	EIM_DA8	EIM_DA3	EIM_OE	EIM_CS0
DISP0_DAT5	DI0_PIN4	DI0_PIN2	EIM_WAIT	EIM_DA7	EIM_DA6	EIM_DA1	EIM_A16
R	P	N	M	L	K	J	H