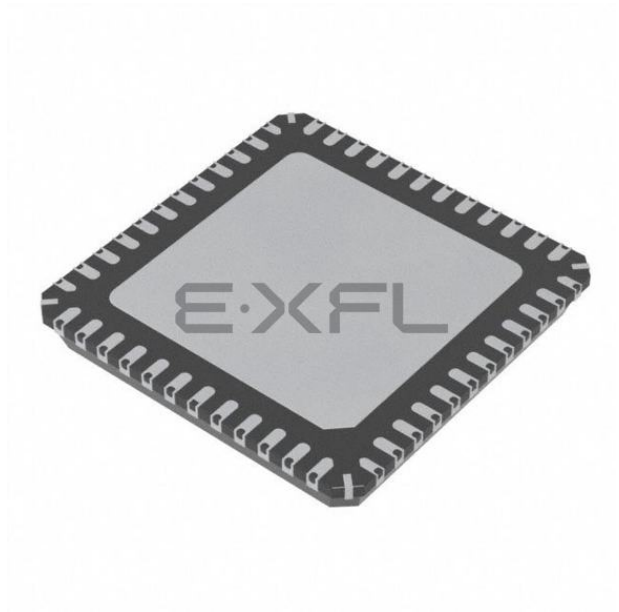

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Automotive
Core Processor	ARM® Cortex®-M0
Program Memory Type	FLASH (64kB)
Controller Series	-
RAM Size	4K x 8
Interface	LIN, SSI, UART
Number of I/O	10
Voltage - Supply	3V ~ 28V
Operating Temperature	-40°C ~ 150°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-31
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9844qxxuma1

Table of Contents

5.2.2 PMU Modes Overview

The following state diagram shows the available modes of the device.

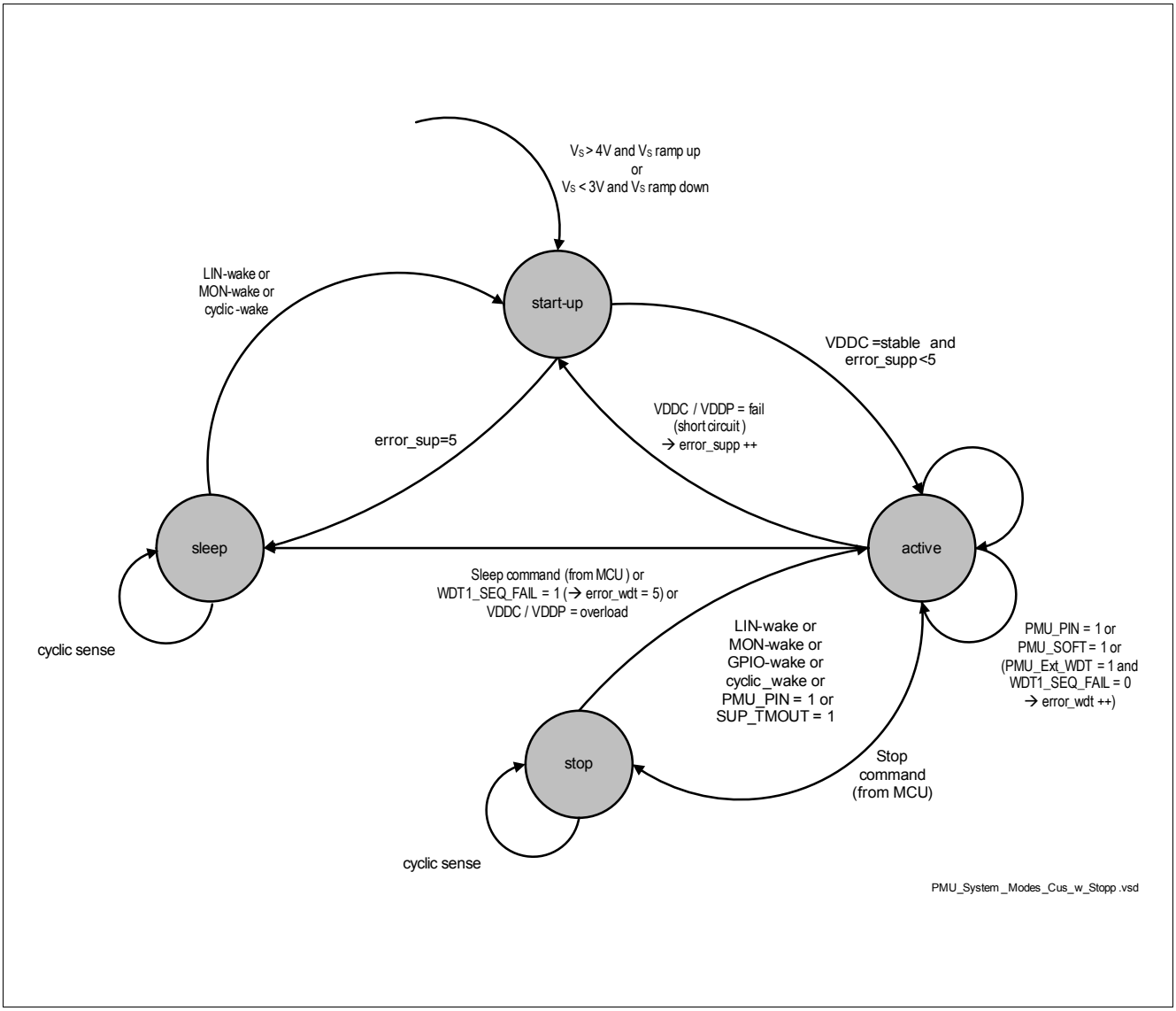

Figure 5 Power Management Unit System Modes

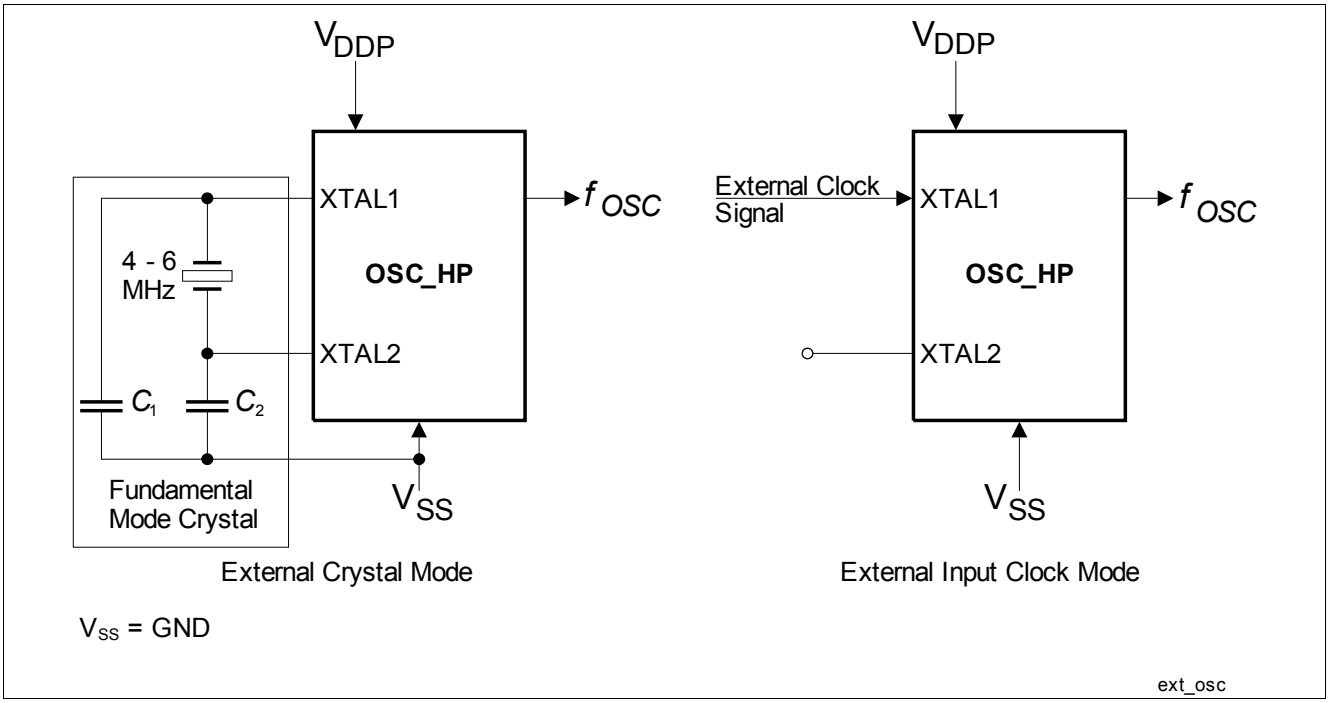

Figure 11 TLE9844QX External Circuitry for the OSC_HP

8.2 Introduction

The ARM Cortex-M0 processor is a leading 32-bit processor and provides a high-performance and cost-optimized platform for a broad range of applications including microcontrollers, automotive body systems and industrial control systems. Like the other Cortex-family processors, the Cortex-M0 processor implements the Thumb®-2 instruction set architecture. With the optimized feature set the Cortex-M0 delivers 32-bit performance in an application space that is usually associated with 8- and 16-bit microcontrollers.

8.2.1 Block Diagram

Figure 15 shows the functional blocks of the Cortex-M0.

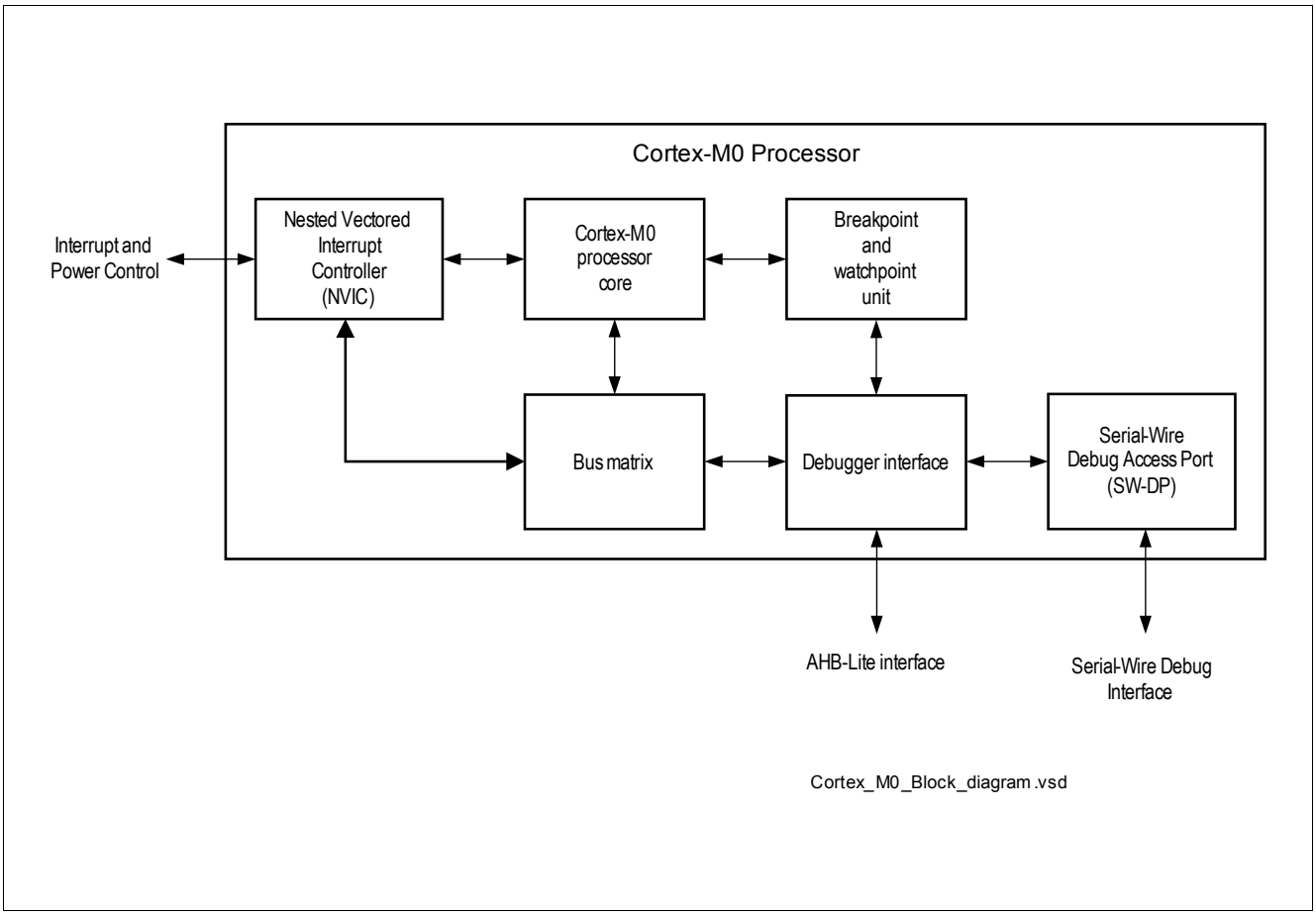

Figure 15 Cortex-M0 Block Diagram

Table 8 Port 0 Input/Output Functions (cont'd)

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P0.5	Input	GPI	P0_DATA.P5	
		INP1	SSC1_M_MRST	SSC1
		INP2	EXINT0_0	SCU
		INP3	T21EX_2	Timer 21
		INP4	T5INA	GPT12
		INP5	CCPOS2_1	CCU6
	Output	GPO	P0_DATA.P5	
		ALT1	SSC1_S_MRST	SSC1
		ALT2	COUT60_0	CCU6
		ALT3	LIN_RXD	LIN

14.3.2 Port 1

14.3.2.1 Port 1 Functions

Port 1alternate function mapping according **Table 9**

Table 9 Port 1 Input / Output Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P1.0	Input	GPI	P1_DATA.P0	
		INP1	T3INC	GPT12
		INP2	CC61_0	CCU6
		INP3	SSC2_S_SCK	SSC2
		INP4	T4EUDB	GPT12
	Output	GPO	P1_DATA.P0	
		ALT1	SSC2_M_SCK	SSC2
		ALT2	CC61_0	CCU6
		ALT3	UART2_TXD	UART2
P1.1	Input	GPI	P1_DATA.P1	
		INP1	T6EUDA	GPT12
		INP2	T5INB	GPT12
		INP3	T3EUDC	GPT12
		INP4	SSC2_S_MTSR	SSC2
		INP5	T21EX_3	Timer 21
		INP6	UART2_RXD	UART2
	Output	GPO	P1_DATA.P1	
		ALT1	SSC2_M_MTSR	SSC2
		ALT2	COUT61_0	CCU6
		ALT3	EXF21_1	Timer 21
P1.2	Input	GPI	P1_DATA.P2	
		INP1	EXINT0_1	SCU
		INP2	T21_1	Timer 21
		INP3	T2INA	GPT12
		INP4	SSC2_M_MRST	SSC2
		INP5	CCPOS2_2	CCU6
	Output	GPO	P1_DATA.P2	
		ALT1	SSC2_S_MRST	SSC2
		ALT2	COUT63_0	CCU6
		ALT3	T3OUT_1	GPT12

15 General Purpose Timer Units (GPT12)

15.1 Features

15.1.1 Features Block GPT1

The following list summarizes the supported features:

- f_{GPT}/4 maximum resolution
- 3 independent timers/counters
- Timers/counters can be concatenated
- 4 operating modes:
  - Timer Mode
  - Gated Timer Mode
  - Counter Mode
  - Incremental Interface Mode
- Reload and Capture functionality
- Shared interrupt: Node 0

15.1.2 Features Block GPT2

The following list summarizes the supported features:

- f_{GPT}/2 maximum resolution
- 2 independent timers/counters
- Timers/counters can be concatenated
- 3 operating modes:
  - Timer Mode
  - Gated Timer Mode
  - Counter Mode
- Extended capture/reload functions via 16-bit capture/reload register CAPREL
- Shared interrupt: Node 1

15.2 Introduction

The General Purpose Timer Unit blocks GPT1 and GPT2 have very flexible multifunctional timer structures which may be used for timing, event counting, pulse width measurement, pulse generation, frequency multiplication, and other purposes.

They incorporate five 16-bit timers that are grouped into the two timer blocks GPT1 and GPT2. Each timer in each block may operate independently in a number of different modes such as Gated timer or Counter Mode, or may be concatenated with another timer of the same block.

Each block has alternate input/output functions and specific interrupts associated with it. Input signals can be selected from several sources by register PISEL.

The GPT module is clocked with clock f_{GPT}. f_{GPT} is a clock derived from f_{SYS}.

18 UART1/UART2

18.1 Features

- Full-duplex asynchronous modes
  - 8-Bit or 9-Bit data frames, LSB first
  - fixed or variable baud rate
- Receive buffered (1 Byte)
- Multiprocessor communication
- Interrupt generation on the completion of a data transmission or reception
- Baud-rate generator with fractional divider for generating a wide range of baud rates, e.g. 9.6kBaud, 19.2kBaud, 115.2kBaud, 125kBaud, 250kBaud, 500kBaud
- Hardware logic for break and sync byte detection
- for UART1: LIN support: connected to timer channel for synchronization to LIN baud rate

In all modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in the modes by the incoming start bit if REN = 1.

The serial interface also provides interrupt requests when transmission or reception of the frames has been completed. The corresponding interrupt request flags are TI or RI, respectively. If the serial interrupt is not used (i.e., serial interrupt not enabled), TI and RI can also be used for polling the serial interface.

18.2 Introduction

The UART1/UART2 provide a full-duplex asynchronous receiver/transmitter, i.e., it can transmit and receive simultaneously. They are also receive-buffered, i.e., they can commence reception of a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time reception of the second byte is complete, the previous byte will be lost. The serial port receive and transmit registers are both accessed at Special Function Register (SFR) SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

20.2.1 Block Diagram

Figure 28 shows all functional relevant interfaces associated with the SSC Kernel.

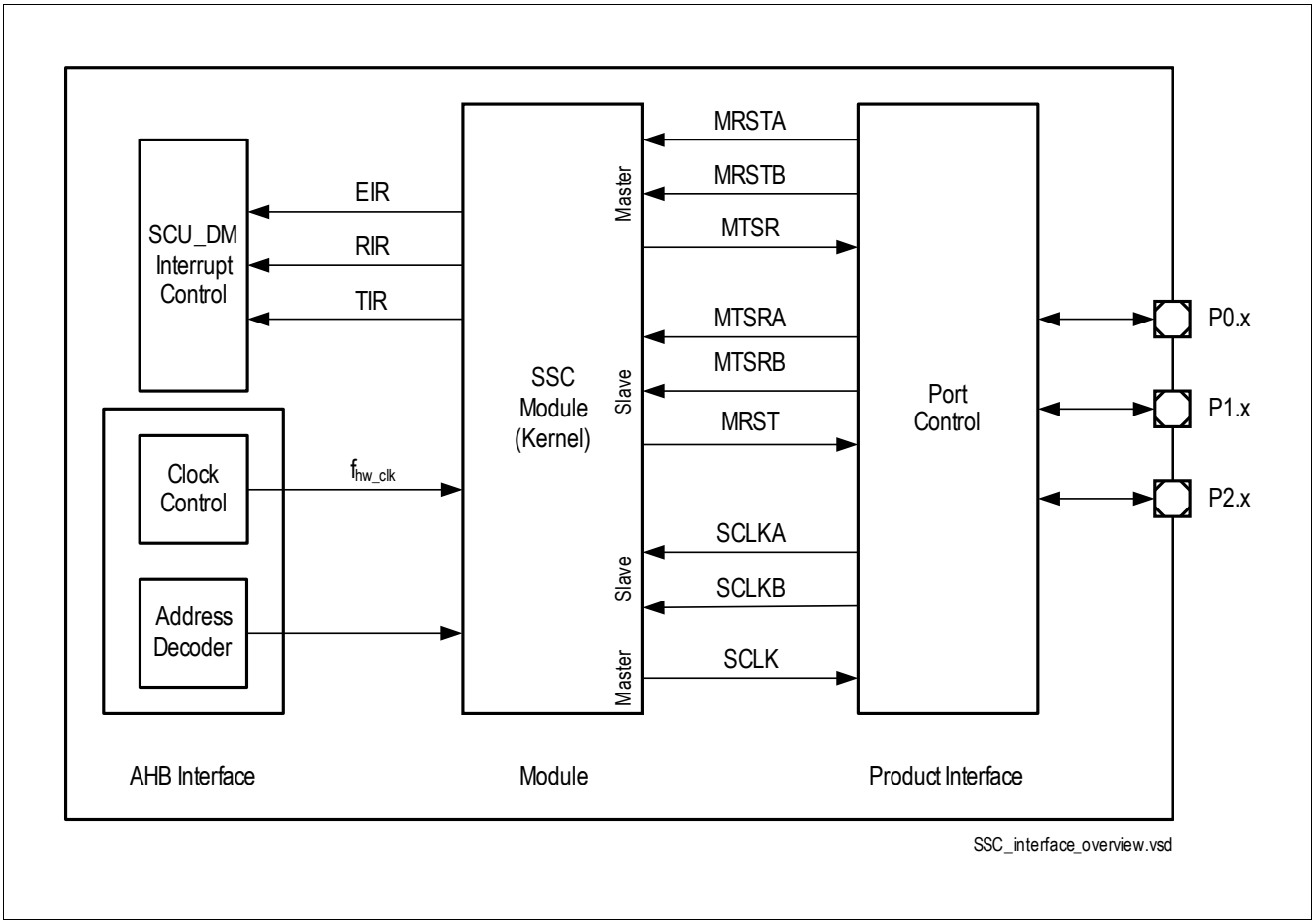

Figure 28 SSC Interface Diagram

25 High-Side Switch

25.1 Features

The high-side switch is optimized for driving resistive loads. Only small line inductance are allowed. Typical applications are single or multiple LEDs of a dashboard, switch illumination or other loads that require a high-side switch.

A cyclic switch activation during Sleep Mode or Stop Mode of the system is also available.

Functional Features

- Multi-purpose high-side switch for resistive load connections (only small line inductances are allowed)
- Overcurrent limitation
- Overcurrent detection with thresholds: 25 mA, 50 mA, 100 mA, 150 mA and automatic shutdown
- Overtemperature detection and automatic shutdown
- Open load detection in on mode with open load current of max. 1.5 mA.
- Interrupt signalling of overcurrent, overtemperature and open load condition
- Cyclic switch activation in Sleep Mode and Stop Mode with cyclic sense support and reduced driver capability: max. 40 mA
- PWM capability up to 25 kHz
- Internal connection to System-PWM Generator (CCU6)
- Slew rate control for low EMI characteristic

Applications hints

- The voltage at HSx must not exceed the supply voltage by more than 0.3V to prevent a reverse current from HSx to VS.

27 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

27.1 Relay Window Lift Application diagram

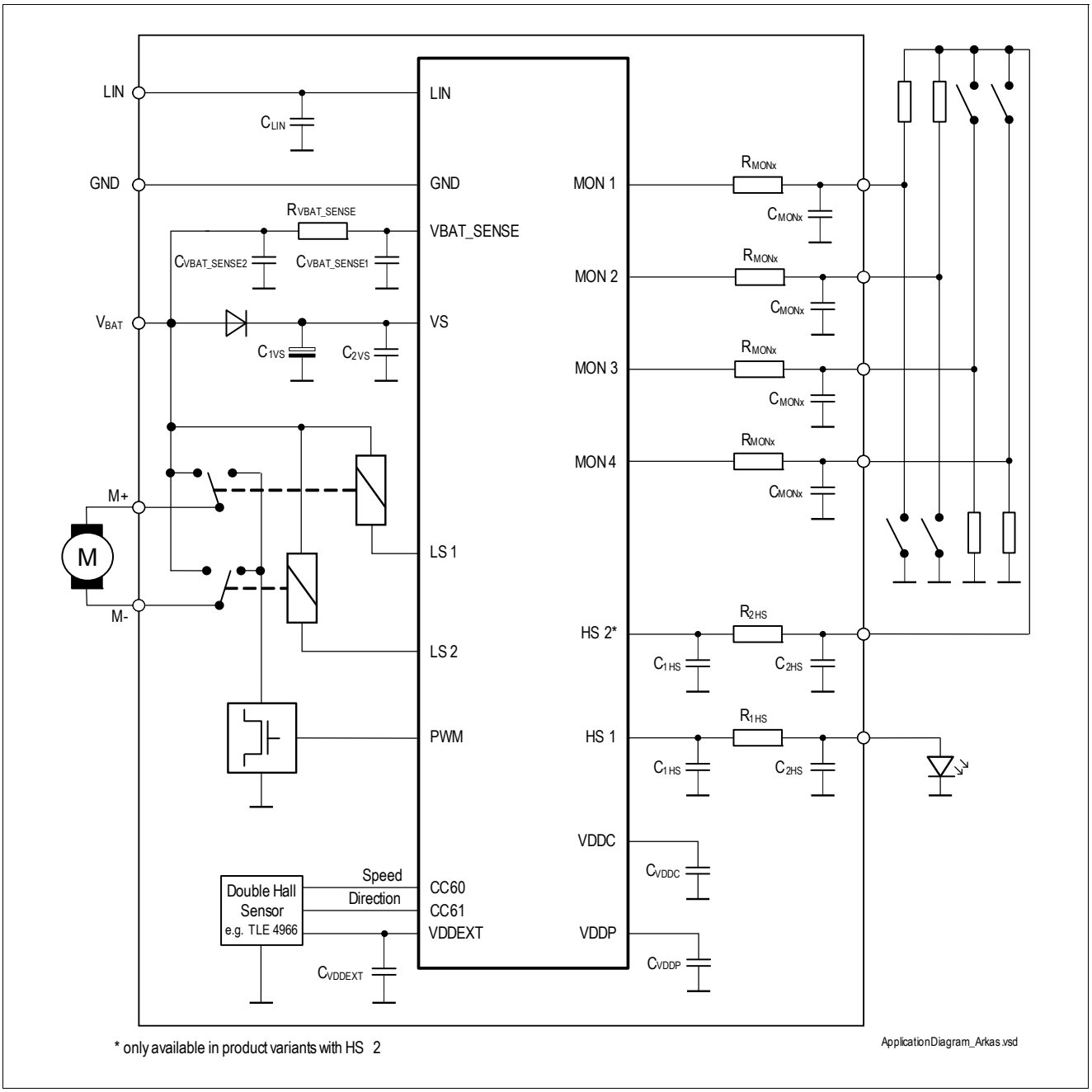

Figure 35 Simplified Application Diagram Example

Note: This is a very simplified example of an application circuit and bill of material. The function must be verified in the actual application.

Table 14 External Component (BOM)

Symbol	Function	Component
C_{1VS}	Capacitor 1 at VS pin	22 µF[1)]
C_{2VS}	Capacitor 2 at VS pin	100 nF[2)3)]
C_{VDDEXT}	Capacitor at VDDEXT pin	330 nF[2)]
C_{VDDC}	Capacitor at VDDC pin	100 nF[2)3)] + 330 nF[2)]
C_{VDDP}	Capacitor at VDDP pin	470 nF[2)3)] + 470 nF[2)]
R_{MONx}	Resistor at MONx pin	3.9 kΩ
C_{MONx}	Capacitor at MONx connector	6.8 nF[4)]
R_{VBAT_SENSE}	Resistor at VBAT_SENSE pin	3.9 kΩ
C_{VBAT_SENSE1}	Capacitor 1at VBAT_SENSE pin	10 nF[2)]
C_{VBAT_SENSE2}	Capacitor 2 at VBAT_SENSE connector	6.8 nF[4)]
C_{LIN}	Capacitor at LIN pin	220 pF
R_{1HS}	Resistor at HS pin for LED	e.g. 2.7kΩ
R_{2HS}	Resistor at HS pin	160 Ω[5)]
C_{1HS}	Capacitor at HS pin	6.8nF[2)]
C_{2HS}	Capacitor at HS connector	33nF[4)]

1) to be dimensioned according to application requirements
2) to reduce the effect of fast voltage transients of Vs, these capacitors should be placed close to the device pin
3) ceramic capacitor
4) for ESD GUN
5) optional, for short to battery protection, calculated for 24V (jump start)

27.2 Connection of N.C. / N.U. pins

The device contains several N.C. (not connected, no bond wire) and N.U. (not used, but bonded) pins.

Table 15 Recommendation for connecting N.C. / N.U. pins

type	pin number	recommendation 1	recommendation 2	comment
N.C.	27, 28, 29, 38, 40, 41	GND		
N.C.	10, 46	open	GND	neighboring high-voltage pins
N.U.	4	VS	open	
N.U.	9	GND		

27.3 Connection of unused pins

Table 16 shows recommendations how to connect pins, in case they are not needed by the application.

Table 19 Functional Range

T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage in Active Mode	V_{S_AM}	5.5	–	28	V	–	P_1.2.1
Extended Supply voltage in Active Mode - Range 1	$V_{S\_AM\_extend\_1}$	28	–	40	V	Functional with parameter deviation[1)]	P_1.2.12
Extended Supply voltage in Active Mode with reduced functionality (Microcontroller / Flash with full operation) - Range 2	$V_{S\_AM\_extend\_2}$	3.0	–	5.5	V	Functional with parameter deviation[2)]	P_1.2.2
Specified Supply voltage for LIN Transceiver - Active Mode	$V_{S\_AM\_LIN}$	5.5	–	18	V	Parameter Specification	P_1.2.3
Extended Supply voltage for LIN Transceiver - Active Mode	$V_{S\_AM\_LIN\_extend}$	4.8	–	28	V	Functional with parameter deviation	P_1.2.4
Extended Supply voltage for LIN & Monitoring Input (MON) - Stop & Sleep Mode	$V_{S\_SSM\_LIN\_MON\_extend}$	3.6	–	5.5	V	Wakeup functionality ensured	P_1.2.13
Min. Supply voltage in Stop Mode	$V_{S\_Stopmin}$	3.0	–	–	V		P_1.2.5
Min. Supply voltage in Sleep Mode	$V_{S\_Sleepmin}$	3.0	–	–	V		P_1.2.6
Supply Voltage transients slew rate	dV_S/dt	-5	–	5	V/µs	3)	P_1.2.7
Output current on any GPIO	I_{OH} , I_{OL}	-10	–	10	mA	3)	P_1.2.8
Output sum current for all GPIO pins	$I_{GPIO,sum}$	-50	–	50	mA	3)	P_1.2.9
Operating frequency	f_{sys} 4)	5	–	25	MHz	3)	P_1.2.10
Junction Temperature	T_j	-40	–	150	°C	–	P_1.2.11

1) This operation voltage range is only allowed for a short duration: $t_{max} \leq 400$ ms.

2) Hall-Supply, ADC, SPI, UART, NVM, RAM, CPU fully functional and in spec down to 3V VS. Actuators (HS, LS) in VS range from 3V < VS < 5.5V functional but some parameters can be out of spec

3) Not subject to production test, specified by design.

4) Function not specified when limits are exceeded.

28.1.3 Current Consumption

28.2.6 Power Down Voltage Regulator (PMU Subblock) Parameters

The PMU Power Down voltage regulator consists of two subblocks:

- Power Down Pre regulator: VDD5VPD
- Power Down Core regulator: VDD1V5_PD (Supply used for GPUDATAxy registers)

Both regulators are used as purely internal supplies. The following table contains all relevant parameter:

Table 28 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Power-On Reset Threshold	$V_{DD1V5\_PD\_RSTTH}$	1.2	–	1.5	V	[1] I_{load} = internal load connected to VDD1V5_PD	P_2.5.1

1) Not subject to production test, specified by design

Table 30 Functional Range (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Low time	t_{2_PLLNM}	12	–	–	ns	[5)6)] –	P_3.2.11
Rise time	t_{3_PLLNM}	–	7	7	ns	[5)6)] –	P_3.2.12
Fall time	t_{4_PLLNM}	–	7	7	ns	[5)6)] –	P_3.2.13

1) Not subject to production test, specified by design.
2) Overload conditions must not occur on pin XTAL1.
3) The amplitude voltage V_{AX1} refers to the offset voltage V_{OFF}. This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by V_{IX1}.
4) this performance is only valid for Prescaler Mode (VCO Bypass mode).
5) tested with rectangular signal with $V_{IN\_Low} = 0V$ to $V_{IN\_High} = V_{DDC}$
6) this performance is only valid for PLL Normal Mode.

28.5 Parallel Ports (GPIO)

28.5.1 Description of Keep and Force Current

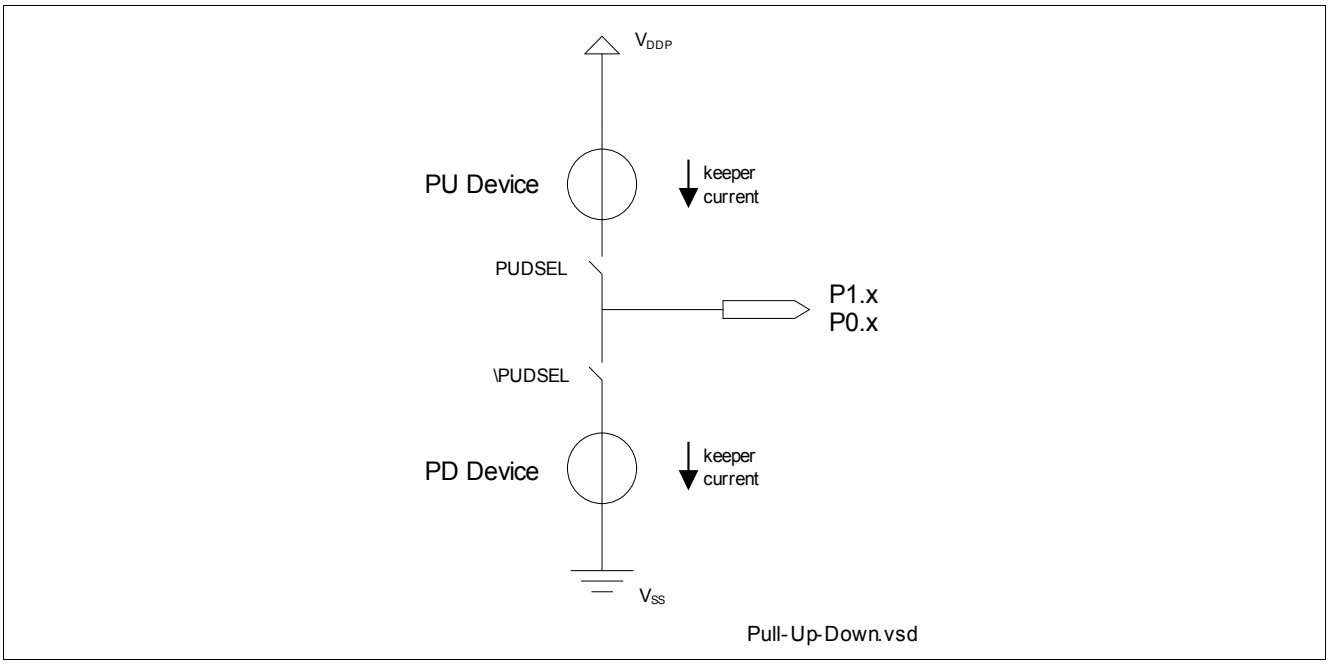

Figure 37 Pull-Up/Down Device

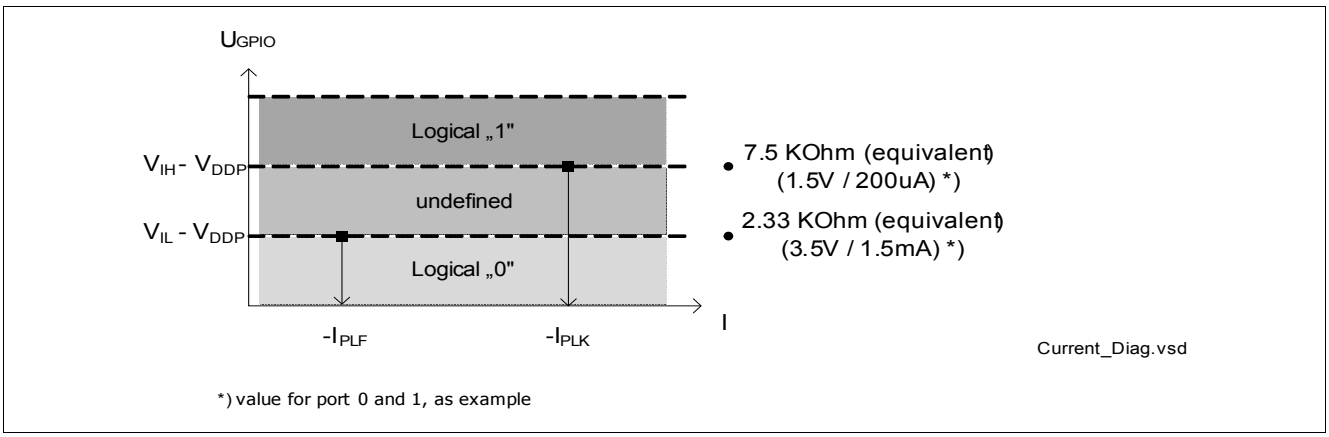

Figure 38 Pull-Up Keep and Forced Current

Table 33 Current Limits for Port Output Drivers[1)] (cont'd)

Port Output Driver Mode	Maximum Output Current (I_{OLmax} , - I_{OHmax})		Output Current (I_{OLnom} , - I_{OHnom})		Number
	VDDP ≥ 4.5V	2.55V < VDDP < 4.5V	VDDP ≥ 4.5V	2.55V < VDDP < 4.5V	
Medium Driver	3 mA	1.8 mA	1.0 mA	0.8 mA	P_5.2.21
Weak Driver	0.5 mA	0.3 mA	0.25 mA	0.15 mA	P_5.2.22

1) Not subject to production test, specified by design.

28.5.3 DC Parameters Port 2

These parameters apply to the IO voltage range, 2.55 V ≤ V_{DDP} ≤ 5.5 V.

Note: Operating Conditions apply.
Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

Table 34 DC Characteristics Port 2

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input low voltage	V_{IL_P2}	-0.3	–	0.3 x V_{DDP}	V	[1)] 4.5V ≤ V_{DDP} ≤ 5.5V	P_5.3.1
Input low voltage	$V_{IL\_P2\_extend}$	-0.3	0.42 x V_{DDP}	–	V	[2)] 2.6V ≤ V_{DDP} < 4.5V	P_5.3.8
Input high voltage	V_{IH_P2}	0.7 x V_{DDP}	–	V_{DDP} + 0.3	V	[1)] 4.5V ≤ V_{DDP} ≤ 5.5V	P_5.3.2
Input high voltage	$V_{IH\_P2\_extend}$	–	0.52 x V_{DDP}	V_{DDP} + 0.3	V	[2)] 2.6V ≤ V_{DDP} < 4.5V	P_5.3.9
Input Hysteresis	HYS_{P2}	0.11 x V_{DDP}	–	–	V	[2)] 4.5V ≤ V_{DDP} ≤ 5.5V; Series resistance = 0 Ω	P_5.3.3
Input Hysteresis	HYS_{P2_extend}	–	0.09 x V_{DDP}	–	V	[2)] 2.6V ≤ V_{DDP} < 4.5V; Series resistance = 0 Ω	P_5.3.10
Input leakage current	I_{OZ1_P2}	-400	–	+400	nA	4.5V ≤ V_{DDP} ≤ 5.5V T_j ≤ 85°C, 0 V < V_{IN} < V_{DDP}	P_5.3.4
Input leakage current (extended temperature range)	$I_{OZ1\_P2\_T\_extend}$	-1	–	+1	uA	2.6V ≤ V_{DDP} < 4.5V T_j ≤ 150°C, 0 V < V_{IN} < V_{DDP}	P_5.3.11
Pull level keep current[4)]	I_{PLK_P2}	–	–	±30	µA	[3)] VPIN ≥ VIH (up) VPIN ≤ VIL (dn)	P_5.3.5

28.8.2 Central Temperature Sensor Module

28.8.2.1 Electrical Characteristics

Table 39 Electrical Characteristics Temperature Sensor Module

V_S = 5.5 V to 28 V, , T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output voltage V_{TEMP} at T_0=0°C (273 K)[2]	a	–	0.628	–	V	T_0=0°C (273 K)	P_8.2.1
Temperature sensitivity b [2]	b	–	2.31	–	mV/K		P_8.2.2
Accuracy_1	Acc_1	-10	–	10	°C	[1]-40°C < T_j < 85°C	P_8.2.3
Accuracy_2	Acc_2	-15	–	15	°C	125°C < T_j < 175°C	P_8.2.4
Accuracy_3	Acc_3	-5	–	5	°C	[2]85°C < T_j < 125°C	P_8.2.5

1) Accuracy with reference to on-chip temperature calibration measurement.

2) Not subject to production test, specified by design.

Table 41 A/D Converter Characteristics (cont'd)

V_S = 5.5 V to 28 V, , T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input referred noise	V_{Noise_LSB}	–	–	1.5	LSB rms	4) T_j = 25°C; this value is determined out of 4 consecutive measurements which are averaged.	P_9.2.34
Cross-coupling Attenuation between LV Channels	EA_{CCOUP}	–	±1	± 2	LSB	4) –	P_9.2.12
Input capacitance of a HV analog input	C_{AINT_HVI}	–	–	200	fF	4)	P_9.2.13
Input capacitance of a LV analog input	C_{AINT_LVI}	–	–	200	fF	4)	P_9.2.19

1) The limit values for f_{ADCI} must not be exceeded when selecting the peripheral frequency and the prescaler setting.
2) this parameter is measured with disabled hardware calibration
3) this Gain error is calibrated by IFX end of line
4) Not subject to production test