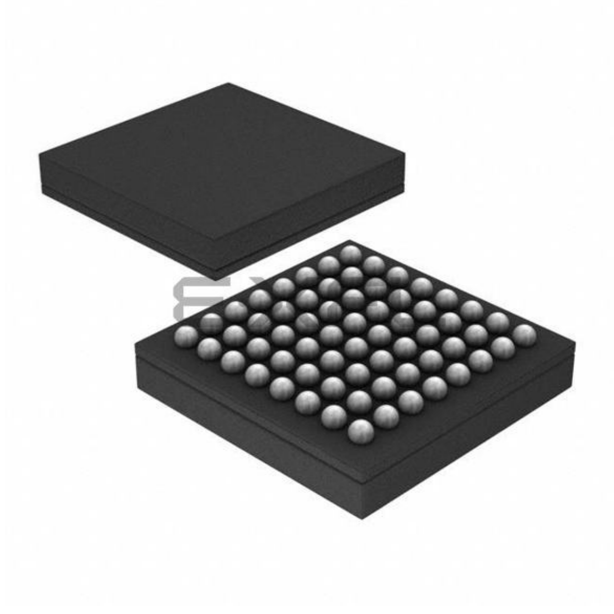

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I²S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 20x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TFBGA
Supplier Device Package	64-TFBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151r6h6a

2.1 Device overview

Table 2. Ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A device features and peripheral counts

Peripheral		STM32L15xCxxxA			STM32L15xRxxxA			STM32L15xVxxxA	
Flash (Kbytes)		32	64	128	32	64	128	64	128
Data EEPROM (Kbytes)		4							
RAM (Kbytes)		16	32	32	16	32	32	32	32
Timers	**General-purpose**	6							
	Basic	2							
Communication interfaces	**SPI**	2							
	I^2C	2							
	USART	3							
	USB	1							
GPIOs		37			51/50(1)			83	
12-bit synchronized ADC **Number of channels**		1 14 channels			1 20/19 channels(1)			1 24 channels	
12-bit DAC **Number of channels**		2 2							
LCD (STM32L152xxxxA Only) **COM x SEG**		4x16			4x32/4x31(1) 8x28/8x27(1)			4x44 8x40	
Comparator		2							
Capacitive sensing channels		13			20				
Max. CPU frequency		32 MHz							
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 V to 3.6 V without BOR option							
Operating temperatures		Ambient operating temperatures: –40 to +85 °C / –40 to + 105 °C Junction temperature: -40 to +110°C							
Packages		LQFP48, UFQFPN48			LQFP64, TFBGA64			LQFP100, UFBGA100	

1. For TFBGA64 package (instead of PC3 pin there is V_{REF+} pin).

line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB wakeup.

Stop mode consumption: refer to *Table 23*.

- **Standby** mode with RTC

  Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI RC and HSE crystal oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.
- **Standby** mode without RTC

  Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI, RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

  Standby mode consumption: refer to *Table 24*.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering the Stop or Standby mode.

Table 3. Functionalities depending on the operating power supply range

Operating power supply range	Functionalities depending on the operating power supply range			
	DAC and ADC operation	USB	Dynamic voltage scaling range	I/O operation
V_{DD} = 1.65 to 1.71 V	Not functional	Not functional	Range 2 or Range 3	Degraded speed performance
V_{DD}= 1.71 to 1.8 V (1)	Not functional	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance
V_{DD} = 1.8 to 2.0 V(1)	Conversion time up to 500 Ksps	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance

Table 3. Functionalities depending on the operating power supply range (continued)

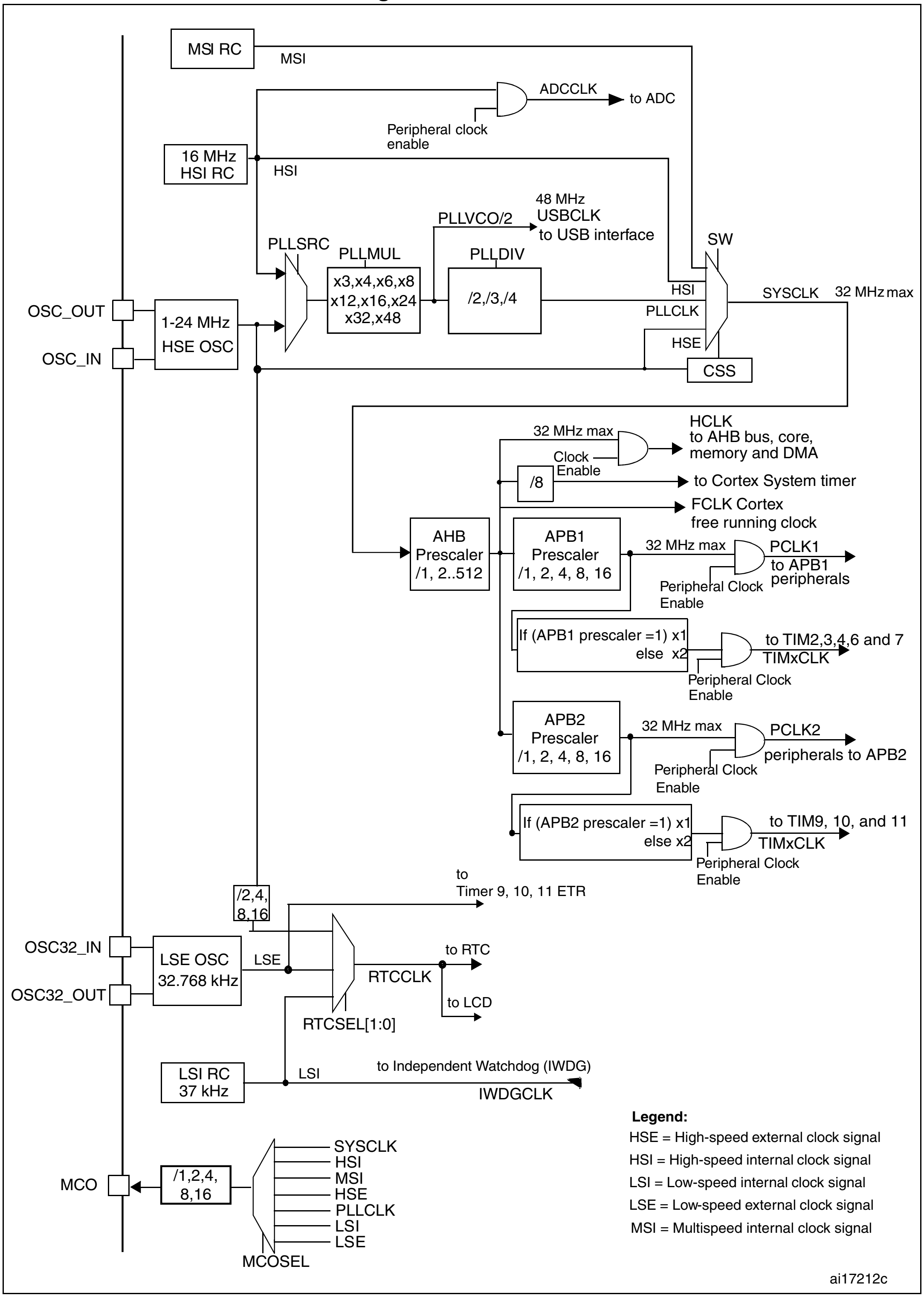
Operating power supply range	Functionalities depending on the operating power supply range			
	DAC and ADC operation	USB	Dynamic voltage scaling range	I/O operation
V_{DD} = 2.0 to 2.4 V	Conversion time up to 500 Ksps	Functional(2)	Range 1, Range 2 or Range 3	Full speed operation
V_{DD} = 2.4 to 3.6 V	Conversion time up to 1 Msps	Functional(2)	Range 1, Range 2 or Range 3	Full speed operation

1. CPU frequency changes from initial to final must respect "F_{CPU} initial < 4*F_{CPU} final" to limit V_{CORE} drop due to current consumption peak when frequency increases. It must also respect 5 µs delay between two changes. For example to switch from 4.2 MHz to 32 MHz, you can switch from 4.2 MHz to 16 MHz, wait 5 µs, then switch from 16 MHz to 32 MHz.
2. Should be USB-compliant from I/O voltage standpoint, the minimum V_{DD} is 3.0 V.

Table 4. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
2.1 MHz to 4.2 MHz (1ws) 32 kHz to 2.1 MHz (0ws)	Range 3

Figure 2. Clock tree



3.9 LCD (liquid crystal display)

The LCD drives up to 8 common terminals and 44 segment terminals to drive up to 320 pixels.

- Internal step-up converter to guarantee functionality and contrast control irrespective of V_{DD}. This converter can be deactivated, in which case the V_{LCD} pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Up to 8 pixels can be programmed to blink
- Unneeded segments and common pins can be used as general I/O pins
- LCD RAM can be updated at any time owing to a double-buffer
- The LCD controller can operate in Stop mode
- V_{LCD} rail decoupling capability

Table 6. V_{LCD} rail decoupling

	Bias			Pin	
	1/2	1/3	1/4		
$V_{LCDrail1}$	1/2 V_{LCD}	2/3 V_{LCD}	1/2 V_{LCD}	PB2	
$V_{LCDrail2}$	NA	1/3 V_{LCD}	1/4 V_{LCD}	PB12	PE11
$V_{LCDrail3}$	NA	NA	3/4 V_{LCD}	PB0	PE12

3.10 ADC (analog-to-digital converter)

A 12-bit analog-to-digital converters is embedded into STM32L151x6/8/B-A and STM32L152x6/8/B-A devices with up to 24 external channels, performing conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start trigger and injection trigger, to allow the application to synchronize A/D conversions and timers. An injection mode allows high priority conversions to be done by interrupting a scan mode which runs in as a background task.

The ADC includes a specific low-power mode. The converter is able to operate at maximum speed even if the CPU is operating at a very low frequency and has an auto-shutdown function. The ADC’s runtime and analog front-end current consumption are thus minimized whatever the MCU operating mode.

3.15.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit down-counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.16 Communication interfaces

3.16.1 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7- and 10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

3.16.2 Universal synchronous/asynchronous receiver transmitter (USART)

All USART interfaces are able to communicate at speeds of up to 4 Mbit/s. They provide hardware management of the CTS and RTS signals and are ISO 7816 compliant. They support IrDA SIR ENDEC and have LIN Master/Slave capability.

All USART interfaces can be served by the DMA controller.

3.16.3 Serial peripheral interface (SPI)

Up to two SPIs are able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

Both SPIs can be served by the DMA controller.

3.16.4 Universal serial bus (USB)

The STM32L151x6/8/B-A and STM32L152x6/8/B-A devices embed a USB device peripheral compatible with the USB full speed 12 Mbit/s. The USB interface implements a full speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and supports suspend/resume. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

3.17 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.18 Development support

Serial wire JTAG debug port (SWJ-DP)

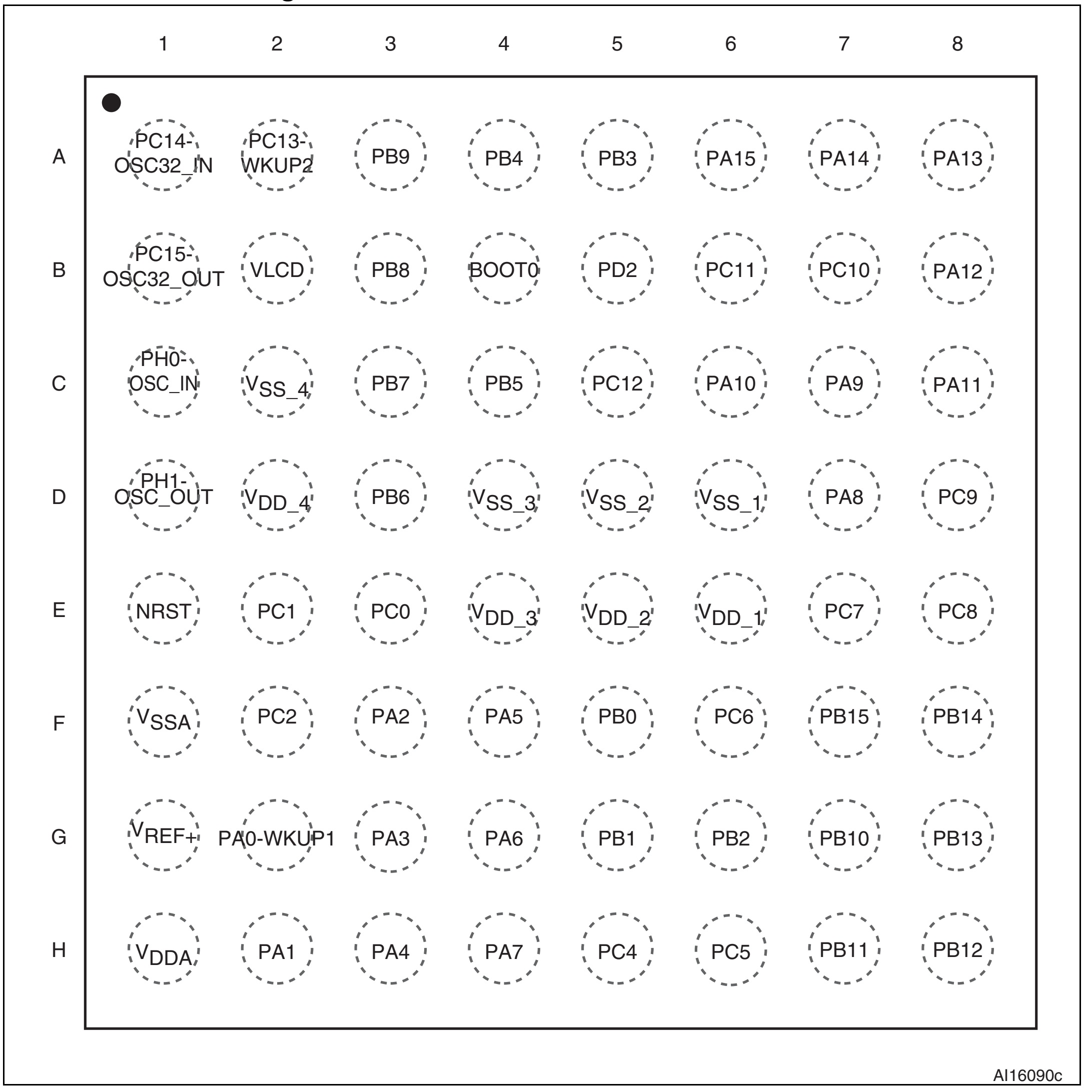
The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG JTMS and JTCK pins are shared with SWDAT and SWCLK, respectively, and a specific sequence on the JTMS pin is used to switch between JTAG-DP and SW-DP.

The JTAG port can be permanently disabled with a JTAG fuse.

Embedded Trace Macrocell™

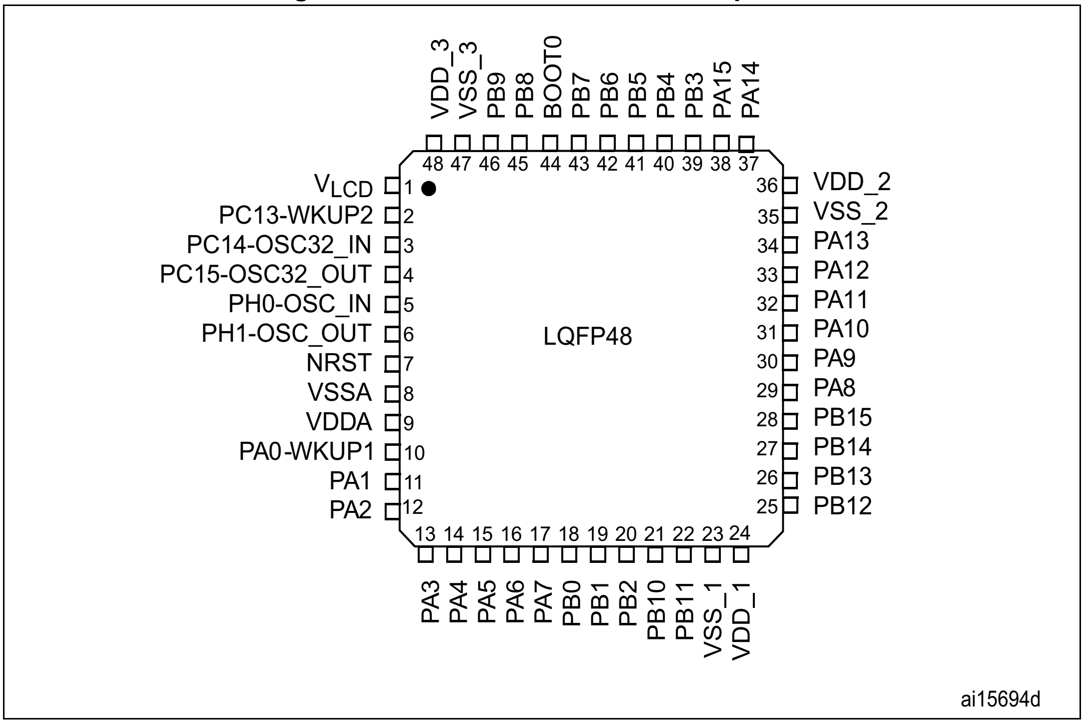
The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32L151x6/8/B-A and STM32L152x6/8/B-A device through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

Figure 5. STM32L15xRxxxA TFBGA64 ballout



1. This figure shows the package top view.

Figure 7. STM32L15xCxxxA LQFP48 pinout



1. This figure shows the package top view.

Table 9. STM32L151x6/8/B-A and STM32L152x6/8/B-A pin definitions (continued)

Pins					Pin name	Pin type(1)	I/O structure	Main function(2) (after reset)	Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48					Alternate functions	Additional functions
51	33	H8	L12	25	PB12	I/O	FT	PB12	SPI2_NSS/I2C2_SMBA/ USART3_CK/ LCD_SEG12/ TIM10_CH1	ADC_IN18/ COMP1_INP /VLCDRAIL2
52	34	G8	K12	26	PB13	I/O	FT	PB13	SPI2_SCK/ USART3_CTS/ LCD_SEG13/TIM9_CH1	ADC_IN19/ COMP1_INP
53	35	F8	K11	27	PB14	I/O	FT	PB14	SPI2_MISO/ USART3_RTS/ LCD_SEG14/TIM9_CH2	ADC_IN20/ COMP1_INP
54	36	F7	K10	28	PB15	I/O	FT	PB15	SPI2_MOSI/ LCD_SEG15/ TIM11_CH1	ADC_IN21/ COMP1_INP/ RTC_REFIN
55	-	-	K9	-	PD8	I/O	FT	PD8	USART3_TX/ LCD_SEG28	-
56	-	-	K8	-	PD9	I/O	FT	PD9	USART3_RX/ LCD_SEG29	-
57	-	-	J12	-	PD10	I/O	FT	PD10	USART3_CK/ LCD_SEG30	-
58	-	-	J11	-	PD11	I/O	FT	PD11	USART3_CTS/ LCD_SEG31	-
59	-	-	J10	-	PD12	I/O	FT	PD12	TIM4_CH1/ USART3_RTS/ LCD_SEG32	-
60	-	-	H12	-	PD13	I/O	FT	PD13	TIM4_CH2/LCD_SEG33	-
61	-	-	H11	-	PD14	I/O	FT	PD14	TIM4_CH3/LCD_SEG34	-
62	-	-	H10	-	PD15	I/O	FT	PD15	TIM4_CH4/LCD_SEG35	-
63	37	F6	E12	-	PC6	I/O	FT	PC6	TIM3_CH1/LCD_SEG24	-
64	38	E7	E11	-	PC7	I/O	FT	PC7	TIM3_CH2/LCD_SEG25	-
65	39	E8	E10	-	PC8	I/O	FT	PC8	TIM3_CH3/LCD_SEG26	-
66	40	D8	D12	-	PC9	I/O	FT	PC9	TIM3_CH4/LCD_SEG27	-

Table 9. STM32L151x6/8/B-A and STM32L152x6/8/B-A pin definitions (continued)

Pins					Pin name	Pin type(1)	I/O structure	Main function(2) (after reset)	Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48					Alternate functions	Additional functions
98	-	-	A2	-	PE1	I/O	FT	PE1	LCD_SEG37/ TIM11_CH1	-
99	63	D4	D3	47	V_{SS_3}	S	-	V_{SS_3}	-	-
100	64	E4	C4	48	V_{DD_3}	S	-	V_{DD_3}	-	-

1. I = input, O = output, S = supply.
2. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripheral that is included. For example, if a device has only one SPI and two USARTs, they will be called SPI1 and USART1 & USART2, respectively. Refer to *Table 2 on page 11*.
3. Applicable to STM32L152xxxxA devices only. In STM32L151xxxxA devices, this pin should be connected to V_{DD}.
4. The PC14 and PC15 I/Os are only configured as OSC32_IN/OSC32_OUT when the LSE oscillator is on (by setting the LSEON bit in the RCC_CSR register). The LSE oscillator pins OSC32_IN/OSC32_OUT can be used as general-purpose PC14/PC15 I/Os, respectively, when the LSE oscillator is off (after reset, the LSE oscillator is off). The LSE has priority over the GPIO function. For more details, refer to Using the OSC32_IN/OSC32_OUT pins as GPIO PC14/PC15 port pins section in the STM32L1xxxx reference manual (RM0038).
5. The PH0 and PH1 I/Os are only configured as OSC_IN/OSC_OUT when the HSE oscillator is on (by setting the HSEON bit in the RCC_CR register). The HSE oscillator pins OSC_IN/OSC_OUT can be used as general-purpose PH0/PH1 I/Os, respectively, when the HSE oscillator is off (after reset, the HSE oscillator is off). The HSE has priority over the GPIO function.
6. Unlike in the LQFP64 package, there is no PC3 in the TFBGA64 package. The V_{REF+} functionality is provided instead.

Table 14. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
P_D	Power dissipation at TA = 85 °C for suffix 6 or TA = 105 °C for suffix 7(4)	UFBGA100 package	-	339	mW
		LQFP100 package	-	435	
		TFBGA64 package	-	308	
		LQFP64 package	-	444	
		LQFP48 package	-	364	
		UFQFPN48 package	-	606	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation(5)	–40	85	°C
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	
T_J	Junction temperature range	6 suffix version	–40	105	°C
	Junction temperature range	7 suffix version	–40	110	

1. When the ADC is used, refer to *Table 55: ADC characteristics*.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.
3. To sustain a voltage higher than V_{DD}+0.3 V, the internal pull-up/pull-down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_J max (see *Table 13: Thermal characteristics on page 56*).
5. In low-power dissipation state, T_A can be extended to -40°C to 105°C temperature range as long as T_J does not exceed T_J max (see *Table 13: Thermal characteristics on page 56*).

6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the ambient temperature condition summarized in the following table.

Table 15. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}(1)	V_{DD} rise time rate	BOR detector enabled	0	-	∞	µs/V
		BOR detector disabled	0	-	1000	
	V_{DD} fall time rate	BOR detector enabled	20	-	∞	
		BOR detector disabled	0	-	1000	
$T_{RSTTEMPO}$(1)	Reset temporization	V_{DD} rising, BOR enabled	-	2	3.3	ms
		V_{DD} rising, BOR disabled(2)	0.4	0.7	1.6	
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1	1.5	1.65	V
		Rising edge	1.3	1.5	1.65	

Table 23. Typical and maximum current consumptions in Stop mode (continued)

Symbol	Parameter	Conditions		Typ[1]	Max [1][2]	Unit
$I_{DD\ (Stop)}$	Supply current in Stop mode (RTC disabled)	Regulator in LP mode, HSI and HSE OFF, independent watchdog and LSI enabled	T_A = -40°C to 25°C	1.80	2.2	µA
		Regulator in LP mode, LSI, HSI and HSE OFF (no independent watchdog)	T_A = -40°C to 25°C	0.434	1	
			T_A = 55°C	0.735	3	
			T_A= 85°C	2.350	9	
			T_A = 105°C	6.84	22[6]	
$I_{DD\ (WU\ from\ Stop)}$	RMS (root mean square) supply current during wakeup time when exiting from Stop mode	MSI = 4.2 MHz	V_{DD} = 3.0 V T_A = -40°C to 25°C	2	-	mA
		MSI = 1.05 MHz		1.45	-	
		MSI = 65 kHz[7]		1.45	-	

1. The typical values are given for V_{DD} = 3.0 V and max values are given for V_{DD} = 3.6 V, unless otherwise specified.
2. Guaranteed by characterization results, unless otherwise specified.
3. LCD enabled with external VLCD, static duty, division ratio = 256, all pixels active, no LCD connected.
4. LCD enabled with external VLCD, 1/8 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
5. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8pF loading capacitors.
6. Guaranteed by test in production.
7. When MSI = 64 kHz, the RMS current is measured over the first 15 µs following the wakeup event. For the remaining time of the wakeup period, the current is similar to the Run mode current.

6.3.7 Internal clock source characteristics

The parameters given in the following table are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Table 14.

High-speed internal (HSI) RC oscillator

Table 31. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz
$TRIM$ (1)(2)	HSI user-trimmed resolution	Trimming code is not a multiple of 16	-	±0.4	0.7	%
		Trimming code is a multiple of 16	-	-	±1.5	%
ACC_{HSI} (2)	Accuracy of the factory-calibrated HSI oscillator	V_{DDA} = 3.0 V, T_A = 25 °C	-1 (3)	-	1 (3)	%
		V_{DDA} = 3.0 V, T_A = 0 to 55 °C	-1.5	-	1.5	%
		V_{DDA} = 3.0 V, T_A = -10 to 70 °C	-2	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 85 °C	-2.5	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 105 °C	-4	-	2	%
		V_{DDA} = 1.65 V to 3.6 V T_A = -40 to 105 °C	-4	-	3	%
$t_{SU(HSI)}$ (2)	HSI oscillator startup time	-	-	3.7	6	μs
$I_{DD(HSI)}$ (2)	HSI oscillator power consumption	-	-	100	140	μA

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).
2. Guaranteed by characterization results.
3. Guaranteed by test in production.

Low-speed internal (LSI) RC oscillator

Table 32. LSI oscillator characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI} (1)	LSI frequency	26	38	56	kHz
D_{LSI} (2)	LSI oscillator frequency drift 0°C ≤ T_A ≤ 85°C	-10	-	4	%
$t_{su(LSI)}$ (3)	LSI oscillator startup time	-	-	200	µs
$I_{DD(LSI)}$ (3)	LSI oscillator power consumption	-	400	510	nA

1. Guaranteed by test in production.
2. This is a deviation for an individual part, once the initial frequency has been measured.
3. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 19* and *Table 45*, respectively.

Unless otherwise specified, the parameters given in *Table 45* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 45. I/O AC characteristics(1)

OSPEEDRx [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Max(2)	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	400	kHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	400	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	625	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	625	
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	2	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	1	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	125	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	250	
10	$F_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	10	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	2	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	25	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	125	
11	$F_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	50	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	8	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	30	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	8	-	

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. The maximum frequency is defined in *Figure 19*.

SPI characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 14*.

Refer to *Section 6.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 50. SPI characteristics[1]

Symbol	Parameter	Conditions	Min	Max[2]	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	16	MHz
		Slave mode	-	16	
		Slave transmitter	-	12[3]	
$t_{r(SCK)}$[2] $t_{f(SCK)}$[2]	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	6	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode	$4t_{HCLK}$	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2t_{HCLK}$	-	
$t_{w(SCKH)}$[2] $t_{w(SCKL)}$[2]	SCK high and low time	Master mode	$t_{SCK}/2-5$	$t_{SCK}/2+3$	
$t_{su(MI)}$[2]	Data input setup time	Master mode	5	-	
$t_{su(SI)}$[2]		Slave mode	6	-	
$t_{h(MI)}$[2]	Data input hold time	Master mode	5	-	
$t_{h(SI)}$[2]		Slave mode	5	-	
$t_{a(SO)}$[4]	Data output access time	Slave mode	0	$3t_{HCLK}$	
$t_{v(SO)}$[2]	Data output valid time	Slave mode	-	33	
$t_{v(MO)}$[2]	Data output valid time	Master mode	-	6.5	
$t_{h(SO)}$[2]	Data output hold time	Slave mode	17	-	
$t_{h(MO)}$[2]		Master mode	0.5	-	

1. The characteristics above are given for voltage Range 1.
2. Guaranteed by characterization results.
3. The maximum SPI clock frequency in slave transmitter mode is given for an SPI slave input clock duty cycle (DuCy(SCK)) ranging between 40 to 60%.
4. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.

6.3.21 LCD controller (STM32L152x6/8/B-A devices only)

The STM32L152xx-A devices embed a built-in step-up converter to provide a constant LCD reference voltage independently from the V_{DD} voltage. An external capacitor C_{ext} must be connected to the V_{LCD} pin to decouple this converter.

Table 63. LCD controller characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{LCD}	LCD external voltage	-	-	3.6	V
V_{LCD0}	LCD internal reference voltage 0	-	2.6	-	V
V_{LCD1}	LCD internal reference voltage 1	-	2.73	-	V
V_{LCD2}	LCD internal reference voltage 2	-	2.86	-	V
V_{LCD3}	LCD internal reference voltage 3	-	2.98	-	V
V_{LCD4}	LCD internal reference voltage 4	-	3.12	-	V
V_{LCD5}	LCD internal reference voltage 5	-	3.26	-	V
V_{LCD6}	LCD internal reference voltage 6	-	3.4	-	V
V_{LCD7}	LCD internal reference voltage 7	-	3.55	-	V
C_{ext}	V_{LCD} external capacitance	0.1	-	2	µF
I_{LCD}(1)	Supply current at V_{DD} = 2.2 V	-	3.3	-	µA
	Supply current at V_{DD} = 3.0 V	-	3.1	-	µA
R_{Htot}(2)	Low drive resistive network overall value	5.28	6.6	7.92	MΩ
R_L(2)	High drive resistive network total value	192	240	288	kΩ
V_{44}	Segment/Common highest level voltage	-	-	V_{LCD}	V
V_{34}	Segment/Common 3/4 level voltage	-	3/4 V_{LCD}	-	V
V_{23}	Segment/Common 2/3 level voltage	-	2/3 V_{LCD}	-	V
V_{12}	Segment/Common 1/2 level voltage	-	1/2 V_{LCD}	-	V
V_{13}	Segment/Common 1/3 level voltage	-	1/3 V_{LCD}	-	V
V_{14}	Segment/Common 1/4 level voltage	-	1/4 V_{LCD}	-	V
V_0	Segment/Common lowest level voltage	0	-	-	V
ΔVxx(2)	Segment/Common level voltage error T_A = -40 to 105 °C	-	-	±50	mV

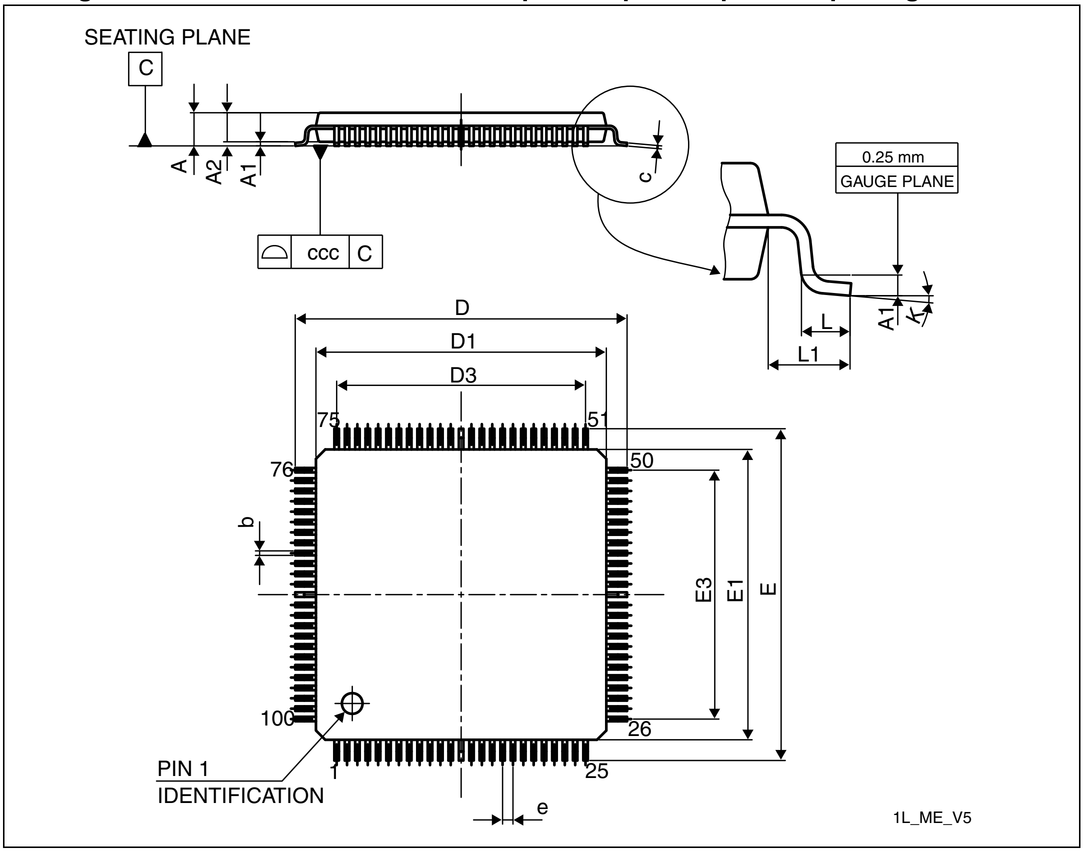
1. LCD enabled with 3 V internal step-up active, 1/8 duty, 1/4 bias, division ratio= 64, all pixels active, no LCD connected
2. Guaranteed by characterization results.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 LQFP100 14 x 14 mm, 100-pin low-profile quad flat package information

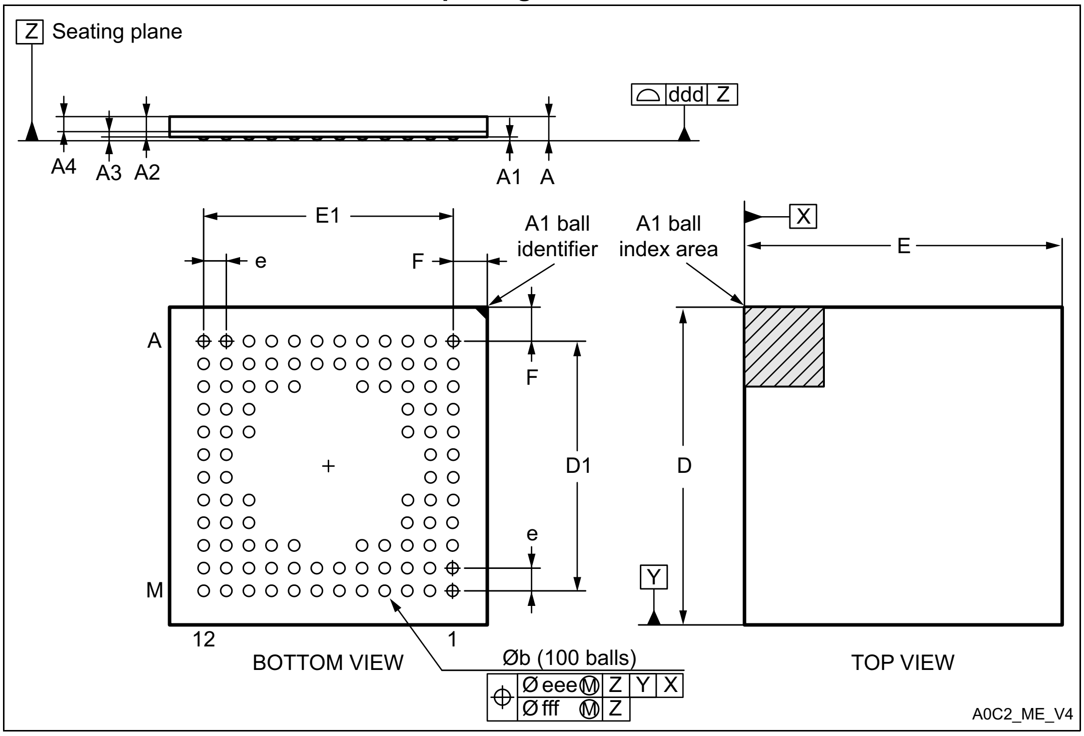
Figure 30. LQFP100 14 x 14 mm, 100-pin low-profile quad flat package outline



1. Drawing is not to scale.

7.5 UFBGA100 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package information

Figure 42. UFBGA100, 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package outline



1. Drawing is not to scale.

Table 68. UFBGA100 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.6	-	-	0.0236
A1	0.05	0.08	0.11	0.002	0.0031	0.0043
A2	0.4	0.45	0.5	0.0157	0.0177	0.0197
A3	0.08	0.13	0.18	0.0031	0.0051	0.0071
A4	0.27	0.32	0.37	0.0106	0.0126	0.0146
b	0.2	0.25	0.3	0.0079	0.0098	0.0118
D	6.95	7	7.05	0.2736	0.2756	0.2776
D1	5.45	5.5	5.55	0.2146	0.2165	0.2185
E	6.95	7	7.05	0.2736	0.2756	0.2776
E1	5.45	5.5	5.55	0.2146	0.2165	0.2185
e	-	0.5	-	-	0.0197	-

Table 68. UFBGA100 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
F	0.7	0.75	0.8	0.0276	0.0295	0.0315
ddd	-	-	0.1	-	-	0.0039
eee	-	-	0.15	-	-	0.0059
fff	-	-	0.05	-	-	0.002

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 43. UFBGA100 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package recommended footprint

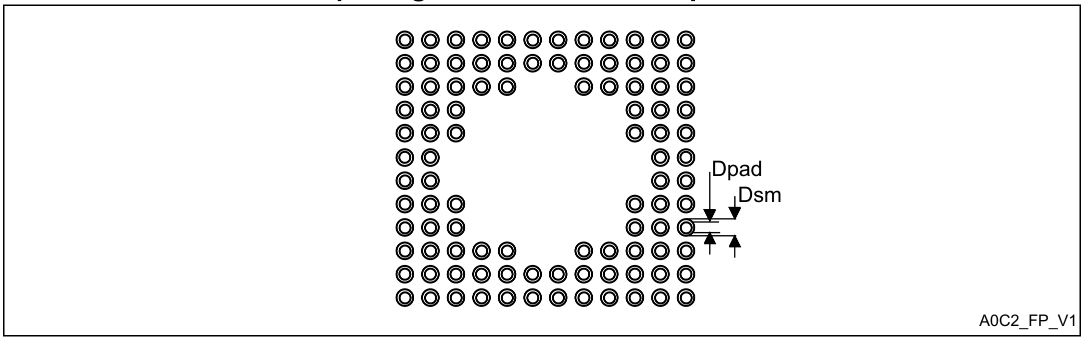


Table 69. UFBGA100 7 x 7 mm, 0.5 mm pitch, recommended PCB design rules

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm