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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I ² S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 20x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151r6t6a

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line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB wakeup.

Stop mode consumption: refer to [Table 23](#).

- **Standby mode with RTC**

Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI RC and HSE crystal oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

The device exits Standby mode in 60 μ s when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby mode without RTC**

Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI, RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

The device exits Standby mode in 60 μ s when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Standby mode consumption: refer to [Table 24](#).

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering the Stop or Standby mode.

Table 3. Functionalities depending on the operating power supply range

Operating power supply range	Functionalities depending on the operating power supply range			
	DAC and ADC operation	USB	Dynamic voltage scaling range	I/O operation
$V_{DD} = 1.65$ to 1.71 V	Not functional	Not functional	Range 2 or Range 3	Degraded speed performance
$V_{DD} = 1.71$ to 1.8 V ⁽¹⁾	Not functional	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance
$V_{DD} = 1.8$ to 2.0 V ⁽¹⁾	Conversion time up to 500 Ksps	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance

3.12 Ultra-low-power comparators and reference voltage

The STM32L151x6/8/B-A and STM32L152x6/8/B-A devices embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- one comparator with fixed threshold
- one comparator with rail-to-rail inputs, fast or slow mode. The threshold can be one of the following:
 - DAC output
 - External I/O
 - Internal reference voltage (V_{REFINT}) or V_{REFINT} submultiple (1/4, 1/2, 3/4)

Both comparators can wake up from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 μ A typical).

3.13 Routing interface

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM3 and TIM4 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1 and COMP2 and the internal reference voltage V_{REFINT} .

3.14 Touch sensing

The STM32L151x6/8/B-A and STM32L152x6/8/B-A devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 20 capacitive sensing channels distributed over 10 analog I/O groups. Both software and timer capacitive sensing acquisition modes are supported.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. The capacitive sensing acquisition only requires few external components to operate. This acquisition is managed directly by the GPIOs, timers and analog I/O groups (see [Section 3.13: Routing interface](#)).

Reliable touch sensing functionality can be quickly and easily implemented using the free STM32L1xx STMTouch touch sensing firmware library.

3.15 Timers and watchdogs

The ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A devices include six general-purpose timers, two basic timers and two watchdog timers.

[Table 7](#) compares the features of the general-purpose and basic timers.

Table 7. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2, TIM3, TIM4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM9	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No
TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.15.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit down-counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.16 Communication interfaces

3.16.1 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7- and 10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

3.16.2 Universal synchronous/asynchronous receiver transmitter (USART)

All USART interfaces are able to communicate at speeds of up to 4 Mbit/s. They provide hardware management of the CTS and RTS signals and are ISO 7816 compliant. They support IrDA SIR ENDEC and have LIN Master/Slave capability.

All USART interfaces can be served by the DMA controller.

3.16.3 Serial peripheral interface (SPI)

Up to two SPIs are able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

Both SPIs can be served by the DMA controller.

3.16.4 Universal serial bus (USB)

The STM32L151x6/8/B-A and STM32L152x6/8/B-A devices embed a USB device peripheral compatible with the USB full speed 12 Mbit/s. The USB interface implements a full speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and supports suspend/resume. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

Table 9. STM32L151x6/8/B-A and STM32L152x6/8/B-A pin definitions (continued)

Pins					Pin name	Pin type ⁽¹⁾	I/O structure	Main function ⁽²⁾ (after reset)	Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48					Alternate functions	Additional functions
51	33	H8	L12	25	PB12	I/O	FT	PB12	SPI2_NSS/I2C2_SMBA/ USART3_CK/ LCD_SEG12/ TIM10_CH1	ADC_IN18/ COMP1_INP /VLCDRAIL2
52	34	G8	K12	26	PB13	I/O	FT	PB13	SPI2_SCK/ USART3_CTS/ LCD_SEG13/TIM9_CH1	ADC_IN19/ COMP1_INP
53	35	F8	K11	27	PB14	I/O	FT	PB14	SPI2_MISO/ USART3_RTS/ LCD_SEG14/TIM9_CH2	ADC_IN20/ COMP1_INP
54	36	F7	K10	28	PB15	I/O	FT	PB15	SPI2_MOSI/ LCD_SEG15/ TIM11_CH1	ADC_IN21/ COMP1_INP/ RTC_REFIN
55	-	-	K9	-	PD8	I/O	FT	PD8	USART3_TX/ LCD_SEG28	-
56	-	-	K8	-	PD9	I/O	FT	PD9	USART3_RX/ LCD_SEG29	-
57	-	-	J12	-	PD10	I/O	FT	PD10	USART3_CK/ LCD_SEG30	-
58	-	-	J11	-	PD11	I/O	FT	PD11	USART3_CTS/ LCD_SEG31	-
59	-	-	J10	-	PD12	I/O	FT	PD12	TIM4_CH1/ USART3_RTS/ LCD_SEG32	-
60	-	-	H12	-	PD13	I/O	FT	PD13	TIM4_CH2/LCD_SEG33	-
61	-	-	H11	-	PD14	I/O	FT	PD14	TIM4_CH3/LCD_SEG34	-
62	-	-	H10	-	PD15	I/O	FT	PD15	TIM4_CH4/LCD_SEG35	-
63	37	F6	E12	-	PC6	I/O	FT	PC6	TIM3_CH1/LCD_SEG24	-
64	38	E7	E11	-	PC7	I/O	FT	PC7	TIM3_CH2/LCD_SEG25	-
65	39	E8	E10	-	PC8	I/O	FT	PC8	TIM3_CH3/LCD_SEG26	-
66	40	D8	D12	-	PC9	I/O	FT	PC9	TIM3_CH4/LCD_SEG27	-

6.3.3 Embedded internal reference voltage

The parameters given in the following table are based on characterization results, unless otherwise specified.

Table 16. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 30 °C \pm 5 °C, $V_{DDA} = 3 \text{ V} \pm 10 \text{ mV}$	0x1FF8 0078-0x1FF8 0079

Table 17. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{\text{REFINT_out}}^{(1)}$	Internal reference voltage	$-40\text{ °C} < T_J < +110\text{ °C}$	1.202	1.224	1.242	V
I_{REFINT}	Internal reference current consumption	-	-	1.4	2.3	μA
T_{VREFINT}	Internal reference startup time	-	-	2	3	ms
$V_{\text{VREF_MEAS}}$	V_{DDA} and $V_{\text{REF+}}$ voltage during V_{REFINT} factory measure	-	2.99	3	3.01	V
$A_{\text{VREF_MEAS}}$	Accuracy of factory-measured V_{REF} value ⁽²⁾	Including uncertainties due to ADC and $V_{\text{DDA}}/V_{\text{REF+}}$ values	-	-	± 5	mV
$T_{\text{Ccoeff}}^{(3)}$	Temperature coefficient	$-40\text{ °C} < T_J < +110\text{ °C}$	-	25	100	ppm/°C
$A_{\text{Ccoeff}}^{(3)}$	Long-term stability	1000 hours, $T = 25\text{ °C}$	-	-	1000	ppm
$V_{\text{DDCcoeff}}^{(3)(4)}$	Voltage coefficient	$3.0\text{ V} < V_{\text{DDA}} < 3.6\text{ V}$	-	-	2000	ppm/V
$T_{\text{S_vrefint}}^{(3)}$	ADC sampling time when reading the internal reference voltage	-	4	-	-	μs
$T_{\text{ADC_BUF}}^{(3)}$	Startup time of reference voltage buffer for ADC	-	-	-	10	μs
$I_{\text{BUF_ADC}}^{(3)}$	Consumption of reference voltage buffer for ADC	-	-	13.5	25	μA
$I_{\text{VREF_OUT}}^{(3)}$	VREF_OUT output current ⁽⁵⁾	-	-	-	1	μA
$C_{\text{VREF_OUT}}^{(3)}$	VREF_OUT output load	-	-	-	50	pF
$I_{\text{LPBUF}}^{(3)}$	Consumption of reference voltage buffer for VREF_OUT and COMP	-	-	730	1200	nA
$V_{\text{REFINT_DIV1}}^{(3)}$	1/4 reference voltage	-	24	25	26	% V_{REFINT}
$V_{\text{REFINT_DIV2}}^{(3)}$	1/2 reference voltage	-	49	50	51	
$V_{\text{REFINT_DIV3}}^{(3)}$	3/4 reference voltage	-	74	75	76	

1. Guaranteed by test in production.

2. The internal V_{REF} value is individually measured in production and stored in dedicated EEPROM bytes.

3. Guaranteed by characterization results.

4. Shortest sampling time can be determined in the application by multiple interactions.

5. To guarantee less than 1% VREF_OUT deviation.

Table 21. Current consumption in Low-power run mode

Symbol	Parameter	Conditions			Typ	Max ⁽¹⁾	Unit
I_{DD} (LP Run)	Supply current in Low-power run mode	All peripherals OFF, code executed from RAM, Flash switched OFF, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz $f_{HCLK} = 32$ kHz	$T_A = -40\text{ °C to }25\text{ °C}$	10.9	12	μA
				$T_A = 85\text{ °C}$	16.5	23	
				$T_A = 105\text{ °C}$	26	47	
			MSI clock, 65 kHz $f_{HCLK} = 65$ kHz	$T_A = -40\text{ °C to }25\text{ °C}$	15	16	
				$T_A = 85\text{ °C}$	22	29	
				$T_A = 105\text{ °C}$	32	51	
			MSI clock, 131 kHz $f_{HCLK} = 131$ kHz	$T_A = -40\text{ °C to }25\text{ °C}$	29	37	
				$T_A = 55\text{ °C}$	32.5	40	
				$T_A = 85\text{ °C}$	35.5	54	
		All peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz $f_{HCLK} = 32$ kHz	$T_A = -40\text{ °C to }25\text{ °C}$	23	24	
				$T_A = 85\text{ °C}$	31	34	
				$T_A = 105\text{ °C}$	42.5	56	
			MSI clock, 65 kHz $f_{HCLK} = 65$ kHz	$T_A = -40\text{ °C to }25\text{ °C}$	29	31	
				$T_A = 85\text{ °C}$	38	41	
				$T_A = 105\text{ °C}$	49	63	
			MSI clock, 131 kHz $f_{HCLK} = 131$ kHz	$T_A = -40\text{ °C to }25\text{ °C}$	46	55	
				$T_A = 55\text{ °C}$	48	59	
				$T_A = 85\text{ °C}$	53.5	72	
				$T_A = 105\text{ °C}$	64.8	84	
$I_{DD\text{ Max}}$ (LP Run) ⁽²⁾	Max allowed current in Low-power run mode	V_{DD} from 1.65 V to 3.6 V	-	-	-	200	

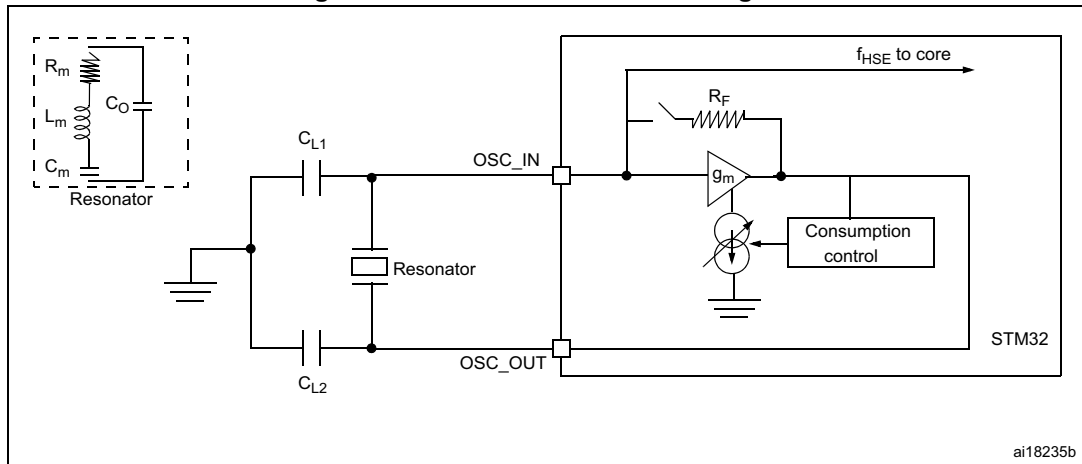
1. Guaranteed by characterization results, unless otherwise specified.

2. This limitation is related to the consumption of the CPU core and the peripherals that are powered by the regulator. Consumption of the I/Os is not included in this limitation.

Table 23. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions			Typ ⁽¹⁾	Max ⁽¹⁾⁽²⁾	Unit
I_{DD} (Stop with RTC)	Supply current in Stop mode with RTC enabled	RTC clocked by LSI, regulator in LP mode, HSI and HSE OFF (no independent watchdog)	LCD OFF	$T_A = -40^{\circ}\text{C}$ to 25°C $V_{DD} = 1.8\text{ V}$	1.13	-	μA
				$T_A = -40^{\circ}\text{C}$ to 25°C	1.38	4	
				$T_A = 55^{\circ}\text{C}$	1.70	6	
				$T_A = 85^{\circ}\text{C}$	3.30	10	
				$T_A = 105^{\circ}\text{C}$	7.80	23	
			LCD ON (static duty) ⁽³⁾	$T_A = -40^{\circ}\text{C}$ to 25°C	1.50	6	
				$T_A = 55^{\circ}\text{C}$	1.80	7	
				$T_A = 85^{\circ}\text{C}$	3.45	12	
				$T_A = 105^{\circ}\text{C}$	8.02	27	
		LCD ON (1/8 duty) ⁽⁴⁾		$T_A = -40^{\circ}\text{C}$ to 25°C	3.80	10	
				$T_A = 55^{\circ}\text{C}$	4.30	11	
				$T_A = 85^{\circ}\text{C}$	6.10	16	
				$T_A = 105^{\circ}\text{C}$	10.8	44	
		RTC clocked by LSE external clock (32.768 kHz), regulator in LP mode, HSI and HSE OFF (no independent watchdog)	LCD OFF	$T_A = -40^{\circ}\text{C}$ to 25°C	1.50	-	
				$T_A = 55^{\circ}\text{C}$	1.90	-	
				$T_A = 85^{\circ}\text{C}$	3.65	-	
				$T_A = 105^{\circ}\text{C}$	8.25	-	
			LCD ON (static duty) ⁽³⁾	$T_A = -40^{\circ}\text{C}$ to 25°C	1.60	-	
				$T_A = 55^{\circ}\text{C}$	2.05	-	
				$T_A = 85^{\circ}\text{C}$	3.75	-	
				$T_A = 105^{\circ}\text{C}$	8.40	-	
			LCD ON (1/8 duty) ⁽⁴⁾	$T_A = -40^{\circ}\text{C}$ to 25°C	3.90	-	
				$T_A = 55^{\circ}\text{C}$	4.55	-	
				$T_A = 85^{\circ}\text{C}$	6.35	-	
				$T_A = 105^{\circ}\text{C}$	11.10	-	
	RTC clocked by LSE (no independent watchdog) ⁽⁵⁾	LCD OFF		$T_A = -40^{\circ}\text{C}$ to 25°C $V_{DD} = 1.8\text{ V}$	1.23	-	
				$T_A = -40^{\circ}\text{C}$ to 25°C $V_{DD} = 3.0\text{ V}$	1.50	-	
				$T_A = -40^{\circ}\text{C}$ to 25°C $V_{DD} = 3.6\text{ V}$	1.75	-	

Figure 17. HSE oscillator circuit diagram



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 14](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 30. LSE oscillator characteristics ($f_{LSE} = 32.768 \text{ kHz}$)⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}	Low speed external oscillator frequency	-	-	32.768	-	kHz
R_F	Feedback resistor	-	-	1.2	-	MΩ
$C^{(2)}$	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S) ⁽³⁾	$R_S = 30 \text{ k}\Omega$	-	8	-	pF
I_{LSE}	LSE driving current	$V_{DD} = 3.3 \text{ V}, V_{IN} = V_{SS}$	-	-	1.1	μA
$I_{DD} \text{ (LSE)}$	LSE oscillator current consumption	$V_{DD} = 1.8 \text{ V}$	-	450	-	nA
		$V_{DD} = 3.0 \text{ V}$	-	600	-	
		$V_{DD} = 3.6 \text{ V}$	-	750	-	
g_m	Oscillator transconductance	-	3	-	-	μA/V
$t_{SU(LSE)}^{(4)}$	Startup time	V_{DD} is stabilized	-	1	-	s

1. Guaranteed by characterization results.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".
3. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details.
4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For CL1 and CL2, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see [Figure 18](#)). CL1 and CL2, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of CL1 and CL2.

Load capacitance CL has the following formula: $CL = CL1 \times CL2 / (CL1 + CL2) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: To avoid exceeding the maximum value of CL1 and CL2 (15 pF) it is strongly recommended to use a resonator with a load capacitance $CL \leq 7$ pF. Never use a resonator with a load capacitance of 12.5 pF.

Example: if you choose a resonator with a load capacitance of $CL = 6$ pF and $C_{stray} = 2$ pF, then $CL1 = CL2 = 8$ pF.

Figure 18. Typical application with a 32.768 kHz crystal

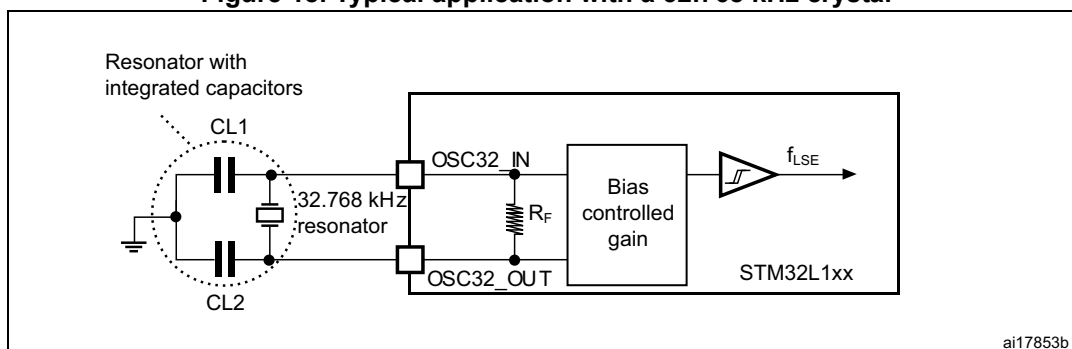
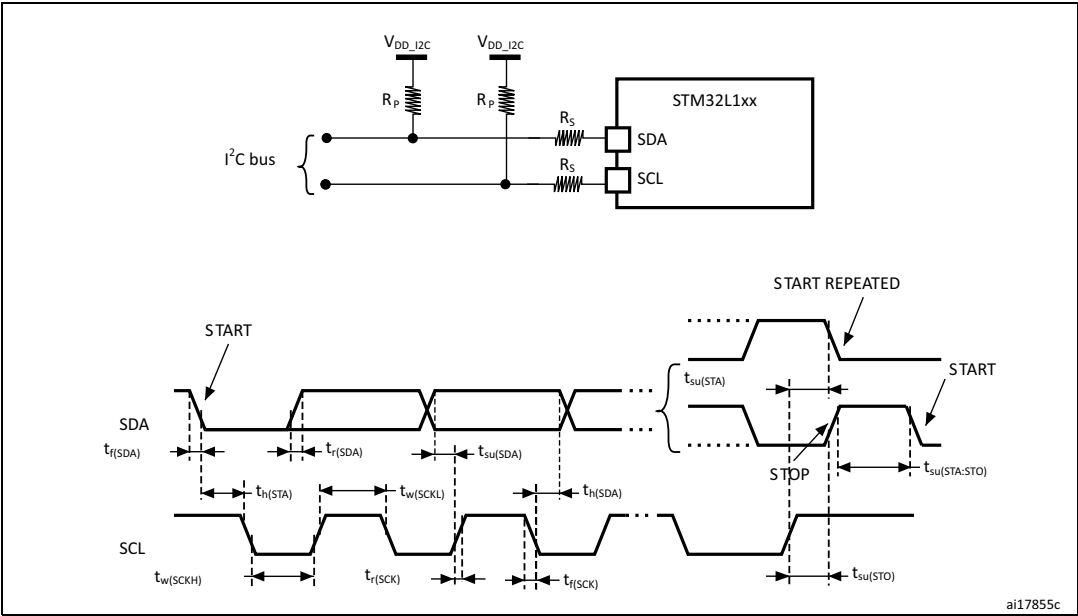


Figure 21. I²C bus AC waveforms and measurement circuit



1. R_S = series protection resistors
2. R_P = pull-up resistors
3. V_{DD_I2C} = I2C bus supply
4. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 49. SCL frequency ($f_{PCLK1} = 32 \text{ MHz}$, $V_{DD} = V_{DD_I2C} = 3.3 \text{ V}$)⁽¹⁾⁽²⁾

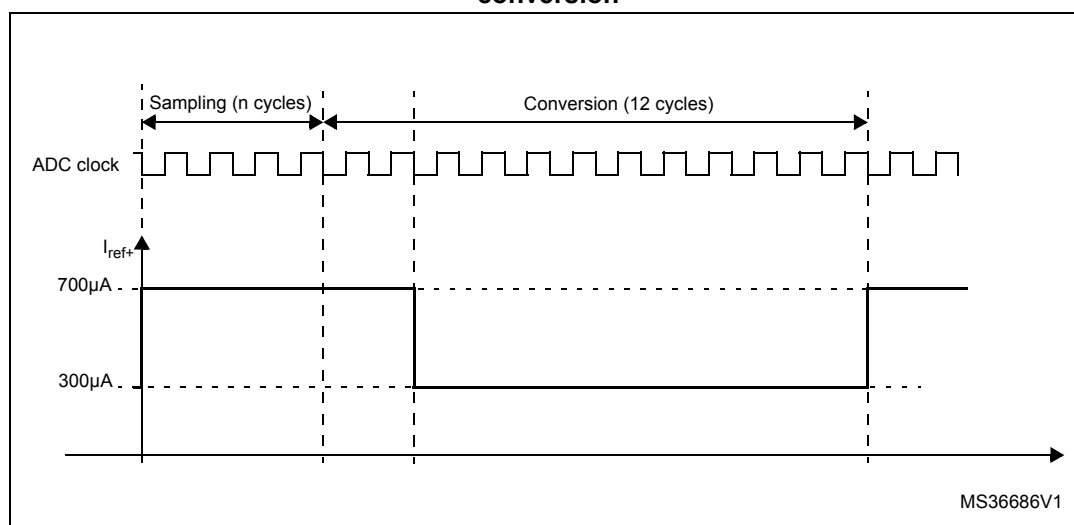
f_{SCL} (kHz)	I2C_CCR value
	$R_P = 4.7 \text{ k}\Omega$
400	0x801B
300	0x8024
200	0x8035
100	0x00A0
50	0x0140
20	0x0320

1. R_P = External pull-up resistance, f_{SCL} = I²C speed.
2. For speeds around 200 kHz, the tolerance on the achieved speed is of $\pm 5\%$. For other speed ranges, the tolerance on the achieved speed is $\pm 2\%$. These variations depend on the accuracy of the external components used to design the application.

Table 55. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_S	Sampling time ⁽⁵⁾	Direct channels $2.4\text{ V} \leq V_{DDA} \leq 3.6\text{ V}$	0.25	-	-	μs
		Multiplexed channels $2.4\text{ V} \leq V_{DDA} \leq 3.6\text{ V}$	0.56	-	-	
		Direct channels $1.8\text{ V} \leq V_{DDA} \leq 2.4\text{ V}$	0.56	-	-	
		Multiplexed channels $1.8\text{ V} \leq V_{DDA} \leq 2.4\text{ V}$	1	-	-	
		-	4	-	384	$1/f_{\text{ADC}}$
t_{CONV}	Total conversion time (including sampling time)	$f_{\text{ADC}} = 16\text{ MHz}$	1	-	24.75	μs
		-	4 to 384 (sampling phase) + 12 (successive approximation)			$1/f_{\text{ADC}}$
C_{ADC}	Internal sample and hold capacitor	Direct channels	-	16	-	pF
		Multiplexed channels	-		-	
f_{TRIG}	External trigger frequency Regular sequencer	12-bit conversions	-	-	$T_{\text{conv}}+1$	$1/f_{\text{ADC}}$
		6/8/10-bit conversions	-	-	T_{conv}	$1/f_{\text{ADC}}$
f_{TRIG}	External trigger frequency Injected sequencer	12-bit conversions	-	-	$T_{\text{conv}}+2$	$1/f_{\text{ADC}}$
		6/8/10-bit conversions	-	-	$T_{\text{conv}}+1$	$1/f_{\text{ADC}}$
R_{AIN}	Signal source impedance ⁽⁵⁾	-	-	-	50	$\text{k}\Omega$
t_{lat}	Injection trigger conversion latency	$f_{\text{ADC}} = 16\text{ MHz}$	219	-	281	ns
		-	3.5	-	4.5	$1/f_{\text{ADC}}$
t_{latr}	Regular trigger conversion latency	$f_{\text{ADC}} = 16\text{ MHz}$	156	-	219	ns
		-	2.5	-	3.5	$1/f_{\text{ADC}}$
t_{STAB}	Power-up time	-	-	-	3.5	μs

1. The $V_{\text{REF}+}$ input can be grounded if neither the ADC nor the DAC are used (this allows to shut down an external voltage reference).
2. The current consumption through V_{REF} is composed of two parameters:
 - one constant (max 300 μA)
 - one variable (max 400 μA), only during sampling time + 2 first conversion pulses.
 So, peak consumption is $300+400 = 700\text{ }\mu\text{A}$ and average consumption is $300 + [(4\text{ sampling} + 2)/16] \times 400 = 450\text{ }\mu\text{A}$ at 1Msps
3. $V_{\text{REF}+}$ can be internally connected to V_{DDA} and $V_{\text{REF}-}$ can be internally connected to V_{SSA} , depending on the package. Refer to [Section 4: Pin descriptions](#) for further details.
4. V_{SSA} or $V_{\text{REF}-}$ must be tied to ground.
5. See [Table 57: Maximum source impedance RAIN max](#) for R_{AIN} limitations

Figure 28. Maximum dynamic current consumption on V_{REF+} supply pin during ADC conversion**Table 57. Maximum source impedance $R_{AIN\ max}^{(1)}$**

Ts (μs)	R _{AIN} max (kOhm)				Ts (cycles) f _{ADC} = 16 MHz ⁽²⁾
	Multiplexed channels		Direct channels		
	2.4 V < V _{DDA} < 3.6 V	1.8 V < V _{DDA} < 2.4 V	2.4 V < V _{DDA} < 3.3 V	1.8 V < V _{DDA} < 2.4 V	
0.25	Not allowed	Not allowed	0.7	Not allowed	4
0.5625	0.8	Not allowed	2.0	1.0	9
1	2.0	0.8	4.0	3.0	16
1.5	3.0	1.8	6.0	4.5	24
3	6.8	4.0	15.0	10.0	48
6	15.0	10.0	30.0	20.0	96
12	32.0	25.0	50.0	40.0	192
24	50.0	50.0	50.0	50.0	384

1. Guaranteed by design.

2. Number of samples calculated for $f_{ADC} = 16\ MHz$. For $f_{ADC} = 8$ and $4\ MHz$ the number of sampling cycles can be reduced with respect to the minimum sampling time Ts (μs).

General PCB design guidelines

Power supply decoupling should be performed as shown in [Figure 12](#), depending on whether V_{REF+} is connected to V_{DDA} or not. The $100\ nF$ capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

Table 58. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
dOffset/dT ⁽¹⁾	Offset error temperature coefficient (code 0x800)	V _{DDA} = 3.3V, V _{REF+} = 3.0V T _A = 0 to 50 °C DAC output buffer OFF	-20	-10	0	μV/°C
		V _{DDA} = 3.3V, V _{REF+} = 3.0V T _A = 0 to 50 °C DAC output buffer ON	0	20	50	
Gain ⁽¹⁾	Gain error ⁽⁶⁾	C _L ≤ 50 pF, R _L ≥ 5 kΩ DAC output buffer ON	-	+0.1 / -0.2%	+0.2 / - 0.5%	%
		No R _L , C _L ≤ 50 pF DAC output buffer OFF	-	+0 / - 0.2%	+0 / - 0.4%	
dGain/dT ⁽¹⁾	Gain error temperature coefficient	V _{DDA} = 3.3V, V _{REF+} = 3.0V T _A = 0 to 50 °C DAC output buffer OFF	-10	-2	0	μV/°C
		V _{DDA} = 3.3V, V _{REF+} = 3.0V T _A = 0 to 50 °C DAC output buffer ON	-40	-8	0	
TUE ⁽¹⁾	Total unadjusted error	C _L ≤ 50 pF, R _L ≥ 5 kΩ DAC output buffer ON	-	12	30	LSB
		No R _L , C _L ≤ 50 pF DAC output buffer OFF	-	8	12	
t _{SETTLING}	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes till DAC_OUT reaches final value ±1LSB)	C _L ≤ 50 pF, R _L ≥ 5 kΩ	-	7	12	μs
Update rate	Max frequency for a correct DAC_OUT change (95% of final value) with 1 LSB variation in the input code	C _L ≤ 50 pF, R _L ≥ 5 kΩ	-	-	1	Msp/s
t _{WAKEUP}	Wakeup time from off state (setting the ENx bit in the DAC Control register) ⁽⁷⁾	C _L ≤ 50 pF, R _L ≥ 5 kΩ	-	9	15	μs
PSRR+	V _{DDA} supply rejection ratio (static DC measurement)	C _L ≤ 50 pF, R _L ≥ 5 kΩ	-	-60	-35	dB

1. Guaranteed by characterization results.

2. Difference between two consecutive codes - 1 LSB.

3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.

4. Difference between the value measured at Code (0x800) and the ideal value = V_{REF+}/2.

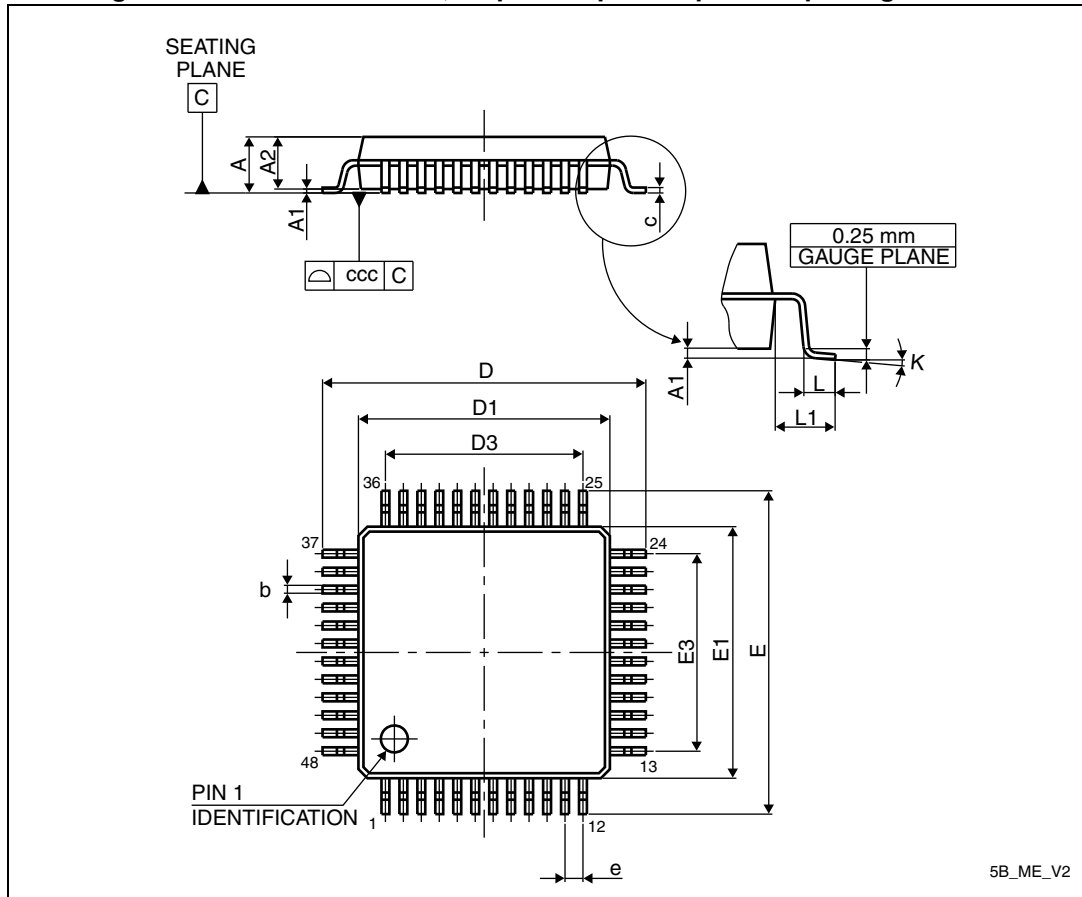
5. Difference between the value measured at Code (0x001) and the ideal value.

6. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFFF when buffer is OFF, and from code giving 0.2 V and (V_{DDA} - 0.2) V when buffer is ON.

7. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

7.3 LQFP48 7 x 7 mm, 48-pin low-profile quad flat package information

Figure 36. LQFP48 7 x 7 mm, 48-pin low-profile quad flat package outline



1. Drawing is not to scale.

7.5 UFBGA100 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package information

Figure 42. UFBGA100, 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package outline

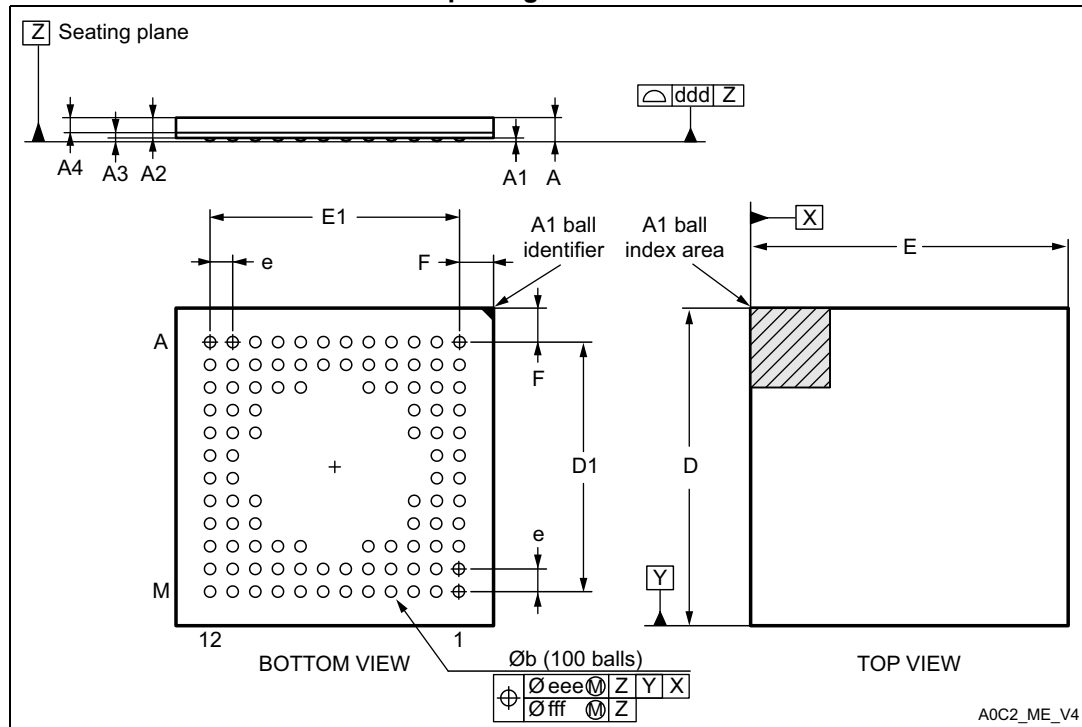


Table 68. UFBGA100 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.6	-	-	0.0236
A1	0.05	0.08	0.11	0.002	0.0031	0.0043
A2	0.4	0.45	0.5	0.0157	0.0177	0.0197
A3	0.08	0.13	0.18	0.0031	0.0051	0.0071
A4	0.27	0.32	0.37	0.0106	0.0126	0.0146
b	0.2	0.25	0.3	0.0079	0.0098	0.0118
D	6.95	7	7.05	0.2736	0.2756	0.2776
D1	5.45	5.5	5.55	0.2146	0.2165	0.2185
E	6.95	7	7.05	0.2736	0.2756	0.2776
E1	5.45	5.5	5.55	0.2146	0.2165	0.2185
e	-	0.5	-	-	0.0197	-

Table 68. UFBGA100 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
F	0.7	0.75	0.8	0.0276	0.0295	0.0315
ddd	-	-	0.1	-	-	0.0039
eee	-	-	0.15	-	-	0.0059
fff	-	-	0.05	-	-	0.002

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 43. UFBGA100 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package recommended footprint

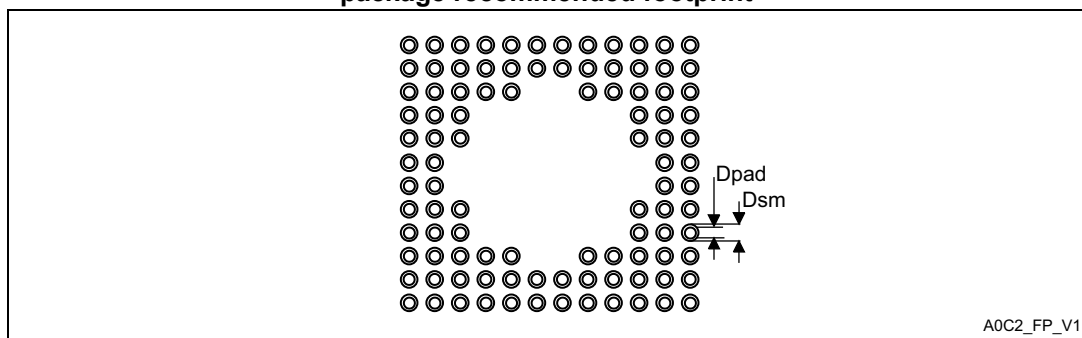
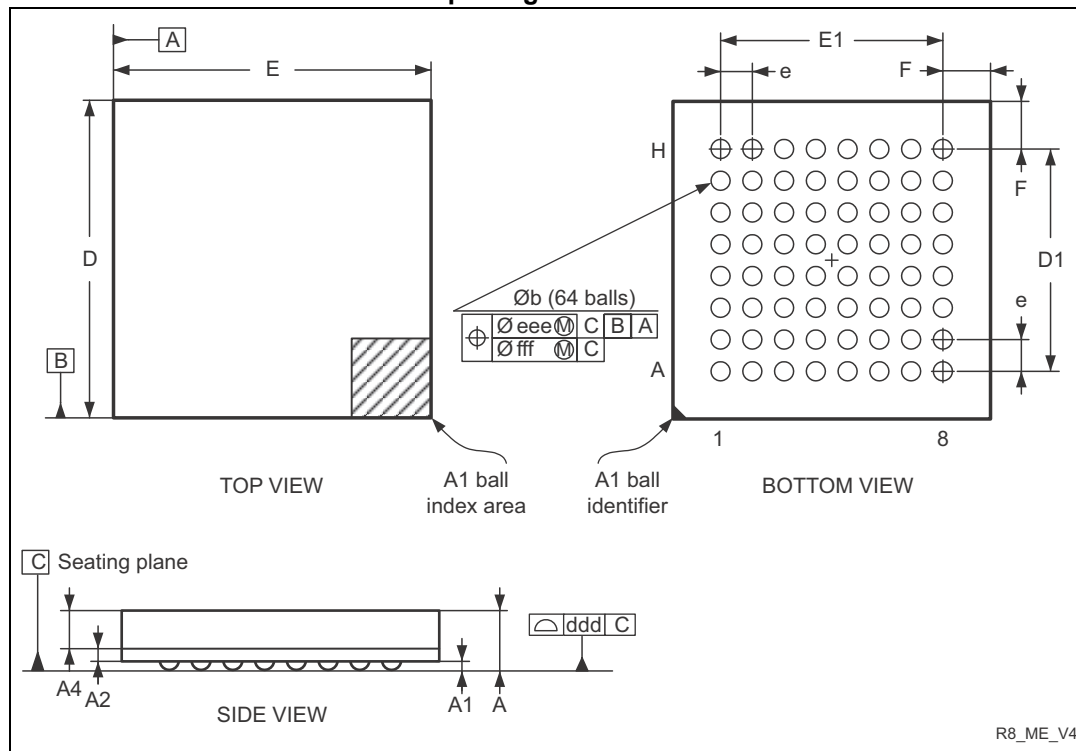


Table 69. UFBGA100 7 x 7 mm, 0.5 mm pitch, recommended PCB design rules

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm

7.6 TFBGA64 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package information

Figure 45. TFBGA64 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package outline



1. Drawing is not to scale.

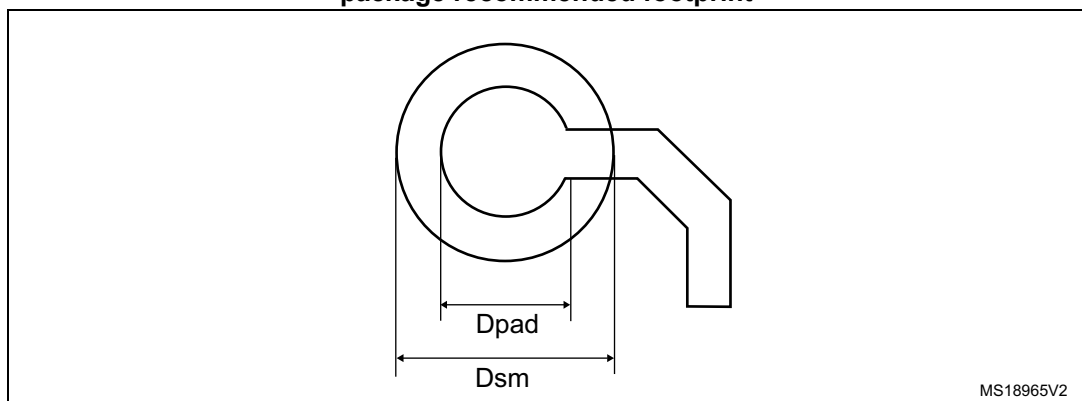
Table 70. TFBGA64 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.200	-	-	0.0472
A1	0.150	-	-	0.0059	-	-
A2	-	0.200	-	-	0.0079	-
A4	-	-	0.600	-	-	0.0236
b	0.250	0.300	0.350	0.0098	0.0118	0.0138
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	-	3.500	-	-	0.1378	-
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	-	3.500	-	-	0.1378	-
e	-	0.500	-	-	0.0197	-
F	-	0.750	-	-	0.0295	-

Table 70. TFBGA64 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.15	-	-	0.0059
fff	-	-	0.05	-	-	0.002

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 46. TFBGA64, 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package recommended footprint**Table 71. TFBGA64 5 x 5 mm, 0.5 mm pitch, recommended PCB design rules**

Dimension	Recommended values
Pitch	0.5
Dpad	0.27 mm
Dsm	0.35 mm typ. (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter.