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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I²S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 20x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151rbt6a

3.1 Low-power modes

The ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A devices support dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply:

- In Range 1 (V_{DD} range limited to 1.71-3.6 V), the CPU runs at up to 32 MHz (refer to *Table 18* for consumption).
- In Range 2 (full V_{DD} range), the CPU runs at up to 16 MHz (refer to *Table 18* for consumption)
- In Range 3 (full V_{DD} range), the CPU runs at up to 4 MHz (generated only with the multispeed internal RC oscillator clock source). Refer to *Table 18* for consumption.

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

  Sleep mode power consumption: refer to *Table 20*.

- **Low-power Run** mode

  This mode is achieved with the multispeed internal (MSI) RC oscillator set to the minimum clock (less than 131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In the low-power Run mode, the clock frequency and the number of enabled peripherals are both limited.

  Low-power Run mode consumption: refer to *Table 21*.

- **Low-power Sleep** mode

  This mode is achieved by entering the Sleep mode with the internal voltage regulator in low-power mode to minimize the regulator's operating current. In the low-power Sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.
  When wakeup is triggered by an event or an interrupt, the system reverts to the run mode with the regulator on.

  Low-power Sleep mode consumption: refer to *Table 22*.

- **Stop** mode with RTC

  Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSI RC and HSE crystal oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

  The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on), it can be the RTC alarm(s), the USB wakeup, the RTC tamper events, the RTC timestamp event or the RTC wakeup.

- **Stop** mode without RTC

  Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, LSE and HSE crystal oscillators are disabled. The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI

3.9 LCD (liquid crystal display)

The LCD drives up to 8 common terminals and 44 segment terminals to drive up to 320 pixels.

- Internal step-up converter to guarantee functionality and contrast control irrespective of V_{DD}. This converter can be deactivated, in which case the V_{LCD} pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Up to 8 pixels can be programmed to blink
- Unneeded segments and common pins can be used as general I/O pins
- LCD RAM can be updated at any time owing to a double-buffer
- The LCD controller can operate in Stop mode
- V_{LCD} rail decoupling capability

Table 6. V_{LCD} rail decoupling

	Bias			Pin	
	1/2	1/3	1/4		
$V_{LCDrail1}$	1/2 V_{LCD}	2/3 V_{LCD}	1/2 V_{LCD}	PB2	
$V_{LCDrail2}$	NA	1/3 V_{LCD}	1/4 V_{LCD}	PB12	PE11
$V_{LCDrail3}$	NA	NA	3/4 V_{LCD}	PB0	PE12

3.10 ADC (analog-to-digital converter)

A 12-bit analog-to-digital converters is embedded into STM32L151x6/8/B-A and STM32L152x6/8/B-A devices with up to 24 external channels, performing conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start trigger and injection trigger, to allow the application to synchronize A/D conversions and timers. An injection mode allows high priority conversions to be done by interrupting a scan mode which runs in as a background task.

The ADC includes a specific low-power mode. The converter is able to operate at maximum speed even if the CPU is operating at a very low frequency and has an auto-shutdown function. The ADC's runtime and analog front-end current consumption are thus minimized whatever the MCU operating mode.

Table 7. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2, TIM3, TIM4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM9	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No
TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Table 9. STM32L151x6/8/B-A and STM32L152x6/8/B-A pin definitions (continued)

Pins					Pin name	Pin type[1]	I/O structure	Main function[2] (after reset)	Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48					Alternate functions	Additional functions
20	-	-	K1	-	V_{REF-}	S	-	V_{REF-}	-	-
21	-	G1 (6)	L1	-	V_{REF+}	S	-	V_{REF+}	-	-
22	13	H1	M1	9	V_{DDA}	S	-	V_{DDA}	-	-
23	14	G2	L2	10	PA0-WKUP1	I/O	FT	PA0	USART2_CTS/ TIM2_CH1_ETR	WKUP1/ ADC_IN0/ COMP1_INP /RTC_TAMP2
24	15	H2	M2	11	PA1	I/O	FT	PA1	USART2_RTS/ TIM2_CH2/LCD_SEG0	ADC_IN1/ COMP1_INP
25	16	F3	K3	12	PA2	I/O	FT	PA2	USART2_TX/ TIM2_CH3/ TIM9_CH1/ LCD_SEG1	ADC_IN2/ COMP1_INP
26	17	G3	L3	13	PA3	I/O	TC	PA3	USART2_RX/ TIM2_CH4/ TIM9_CH2/ LCD_SEG2	ADC_IN3/ COMP1_INP
27	18	C2	E3	-	V_{SS_4}	S	-	V_{SS_4}	-	-
28	19	D2	H3	-	V_{DD_4}	S	-	V_{DD_4}	-	-
29	20	H3	M3	14	PA4	I/O	TC	PA4	SPI1_NSS/ USART2_CK	ADC_IN4/ DAC_OUT1/ COMP1_INP
30	21	F4	K4	15	PA5	I/O	TC	PA5	SPI1_SCK/ TIM2_CH1_ETR	ADC_IN5/ DAC_OUT2/ COMP1_INP
31	22	G4	L4	16	PA6	I/O	FT	PA6	SPI1_MISO/TIM3_CH1/ LCD_SEG3/TIM10_CH1	ADC_IN6/ COMP1_INP
32	23	H4	M4	17	PA7	I/O	FT	PA7	SPI1_MOSI/TIM3_CH2/ LCD_SEG4/TIM11_CH1	ADC_IN7/ COMP1_INP
33	24	H5	K5	-	PC4	I/O	FT	PC4	LCD_SEG22	ADC_IN14/ COMP1_INP
34	25	H6	L5	-	PC5	I/O	FT	PC5	LCD_SEG23	ADC_IN15/ COMP1_INP

Table 9. STM32L151x6/8/B-A and STM32L152x6/8/B-A pin definitions (continued)

Pins					Pin name	Pin type[1]	I/O structure	Main function[2] (after reset)	Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48					Alternate functions	Additional functions
98	-	-	A2	-	PE1	I/O	FT	PE1	LCD_SEG37/ TIM11_CH1	-
99	63	D4	D3	47	V_{SS_3}	S	-	V_{SS_3}	-	-
100	64	E4	C4	48	V_{DD_3}	S	-	V_{DD_3}	-	-

1. I = input, O = output, S = supply.
2. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripheral that is included. For example, if a device has only one SPI and two USARTs, they will be called SPI1 and USART1 & USART2, respectively. Refer to *Table 2 on page 11*.
3. Applicable to STM32L152xxxxA devices only. In STM32L151xxxxA devices, this pin should be connected to V_{DD}.
4. The PC14 and PC15 I/Os are only configured as OSC32_IN/OSC32_OUT when the LSE oscillator is on (by setting the LSEON bit in the RCC_CSR register). The LSE oscillator pins OSC32_IN/OSC32_OUT can be used as general-purpose PC14/PC15 I/Os, respectively, when the LSE oscillator is off (after reset, the LSE oscillator is off). The LSE has priority over the GPIO function. For more details, refer to Using the OSC32_IN/OSC32_OUT pins as GPIO PC14/PC15 port pins section in the STM32L1xxxx reference manual (RM0038).
5. The PH0 and PH1 I/Os are only configured as OSC_IN/OSC_OUT when the HSE oscillator is on (by setting the HSEON bit in the RCC_CR register). The HSE oscillator pins OSC_IN/OSC_OUT can be used as general-purpose PH0/PH1 I/Os, respectively, when the HSE oscillator is off (after reset, the HSE oscillator is off). The HSE has priority over the GPIO function.
6. Unlike in the LQFP64 package, there is no PC3 in the TFBGA64 package. The V_{REF+} functionality is provided instead.

Table 10. Alternate function input/output

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART 1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
BOOT0	BOOT0	-	-	-	-	-	-	-	-	-	-	-	-	-	-
NRST	NRST	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PA0-WKUP1	-	TIM2_CH1_ETR	-	-	-	-	-	USART2_CTS	-	-	-	-	-	TIMx_IC1	EVENTOUT
PA1	-	TIM2_CH2	-	-	-	-	-	USART2_RTS	-	-	[SEG0]	-	-	TIMx_IC2	EVENTOUT
PA2	-	TIM2_CH3	-	TIM9_CH1	-	-	-	USART2_TX	-	-	[SEG1]	-	-	TIMx_IC3	EVENTOUT
PA3	-	TIM2_CH4	-	TIM9_CH2	-	-	-	USART2_RX	-	-	[SEG2]	-	-	TIMx_IC4	EVENTOUT
PA4	-	-	-	-	-	SPI1_NSS	-	USART2_CK	-	-	-	-	-	TIMx_IC1	EVENTOUT
PA5	-	TIM2_CH1_ETR	-	-	-	SPI1_SCK	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PA6	-	-	TIM3_CH1	TIM10_CH1	-	SPI1_MISO	-	-	-	-	[SEG3]	-	-	TIMx_IC3	EVENTOUT
PA7	-	-	TIM3_CH2	TIM11_CH1	-	SPI1_MOSI	-	-	-	-	[SEG4]	-	-	TIMx_IC4	EVENTOUT
PA8	MCO	-	-	-	-	-	-	USART1_CK	-	-	[COM0]	-	-	TIMx_IC1	EVENTOUT
PA9	-	-	-	-	-	-	-	USART1_TX	-	-	[COM1]	-	-	TIMx_IC2	EVENTOUT
PA10	-	-	-	-	-	-	-	USART1_RX	-	-	[COM2]	-	-	TIMx_IC3	EVENTOUT
PA11	-	-	-	-	-	SPI1_MISO	-	USART1_CTS	-	-	-	-	-	TIMx_IC4	EVENTOUT
PA12	-	-	-	-	-	SPI1_MOSI	-	USART1_RTS	-	-	-	-	-	TIMx_IC1	EVENTOUT
PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PA15	JTDI	TIM2_CH1_ETR	-	-	-	SPI1_NSS	-	-	-	-	SEG17	-	-	TIMx_IC4	EVENTOUT
PB0	-	-	TIM3_CH3	-	-	-	-	-	-	-	[SEG5]	-	-	-	EVENTOUT
PB1	-	-	TIM3_CH4	-	-	-	-	-	-	-	[SEG6]	-	-	-	EVENTOUT
PB2	BOOT1	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PB3	JTDO	TIM2_CH2	-	-	-	SPI1_SCK	-	-	-	-	[SEG7]	-	-	-	EVENTOUT

Table 10. Alternate function input/output (continued)

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART 1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
PC10	-	-	-	-	-	-	-	USART3_TX	-	-	COM4 / SEG28 / SEG40	-	-	TIMx_IC3	EVENTOUT
PC11	-	-	-	-	-	-	-	USART3_RX	-	-	COM5 / SEG29 / SEG41	-	-	TIMx_IC4	EVENTOUT
PC12	-	-	-	-	-	-	-	USART3_CK	-	-	COM6 / SEG30 / SEG42	-	-	TIMx_IC1	EVENTOUT
PC13-WKUP2	-	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PC14-OSC32_IN	-	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PC15-OSC32_OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PD0	-	-	-	TIM9_CH1	-	SPI2_NSS	-	-	-	-	-	-	-	TIMx_IC1	EVENTOUT
PD1	-	-	-	-	-	SPI2_SCK	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PD2	-	-	TIM3_ETR	-	-	-	-	-	-	-	COM7 / SEG31 / SEG43	-	-	TIMx_IC3	EVENTOUT
PD3	-	-	-	-	-	SPI2_MISO	-	USART2_CTS	-	-	-	-	-	TIMx_IC4	EVENTOUT
PD4	-	-	-	-	-	SPI2_MOSI	-	USART2_RTS	-	-	-	-	-	TIMx_IC1	EVENTOUT
PD5	-	-	-	-	-	-	-	USART2_TX	-	-	-	-	-	TIMx_IC2	EVENTOUT
PD6	-	-	-	-	-	-	-	USART2_RX	-	-	-	-	-	TIMx_IC3	EVENTOUT
PD7	-	-	-	TIM9_CH2	-	-	-	USART2_CK	-	-	-	-	-	TIMx_IC4	EVENTOUT
PD8	-	-	-	-	-	-	-	USART3_TX	-	-	-	-	-	TIMx_IC1	EVENTOUT
PD9	-	-	-	-	-	-	-	USART3_RX	-	-	-	-	-	TIMx_IC2	EVENTOUT

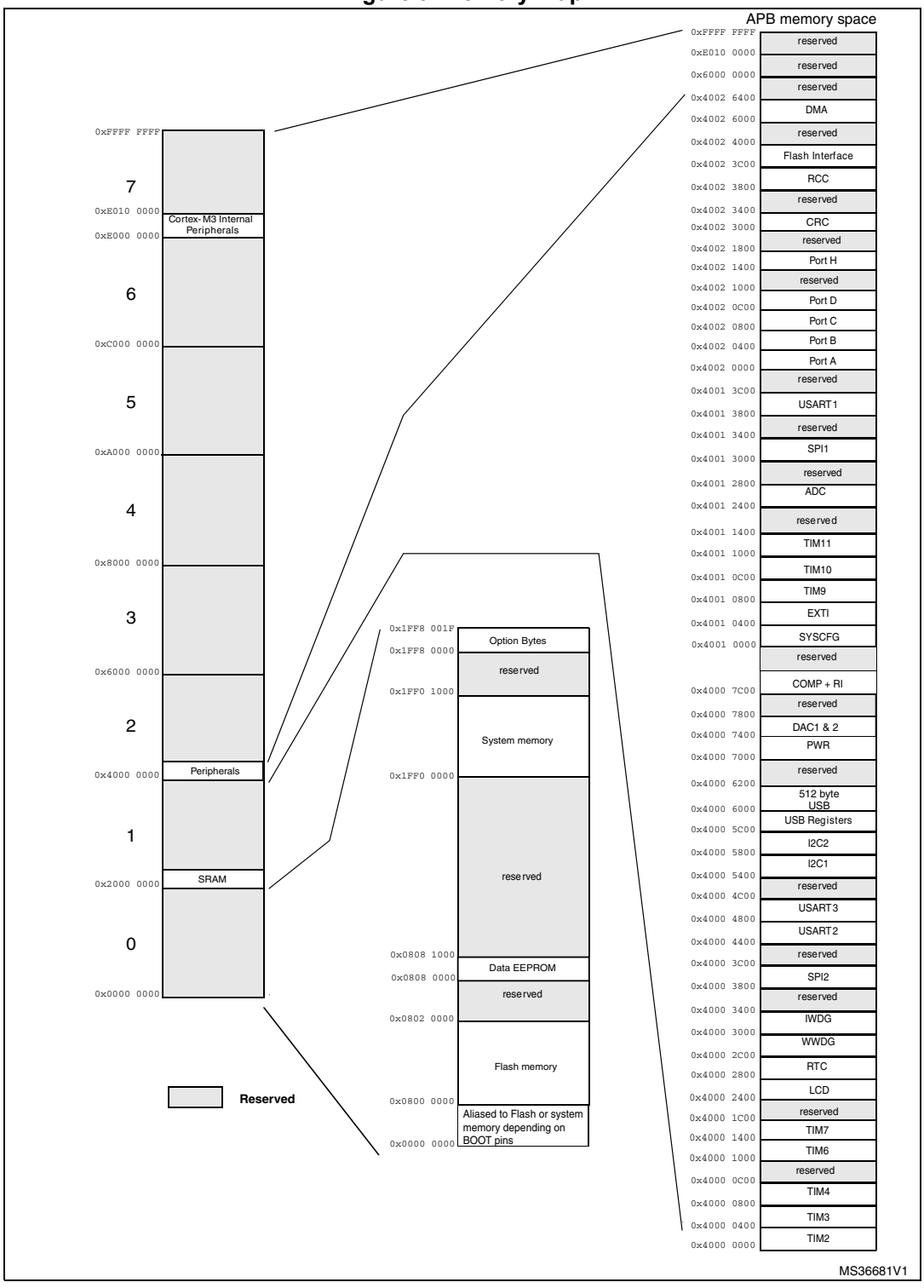
Table 10. Alternate function input/output (continued)

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART 1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
PD10	-	-	-	-	-	-	-	USART3_CK	-	-	-	-	-	TIMx_IC3	EVENTOUT
PD11	-	-	-	-	-	-	-	USART3_CTS	-	-	-	-	-	TIMx_IC4	EVENTOUT
PD12	-	-	TIM4_CH1	-	-	-	-	USART3_RTS	-	-	-	-	-	TIMx_IC1	EVENTOUT
PD13	-	-	TIM4_CH2	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PD14	-	-	TIM4_CH3	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PD15	-	-	TIM4_CH4	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PE0	-	-	TIM4_ETR	TIM10_CH1	-	-	-	-	-	-	-	-	-	TIMx_IC1	EVENTOUT
PE1	-	-		TIM11_CH1	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PE2	TRACECK	-	TIM3_ETR	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PE3	TRACED0	-	TIM3_CH1	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PE4	TRACED1	-	TIM3_CH2	-	-	-	-	-	-	-	-	-	-	TIMx_IC1	EVENTOUT
PE5	TRACED2	-	-	TIM9_CH1*	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PE6	TRACED3	-	-	TIM9_CH2*	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PE7	-	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PE8	-	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC1	EVENTOUT
PE9	-	TIM2_CH1_ETR	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PE10	-	TIM2_CH2	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PE11	-	TIM2_CH3	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PE12	-	TIM2_CH4	-	-	-	SPI1_NSS	-	-	-	-	-	-	-	TIMx_IC1	EVENTOUT
PE13	-	-	-	-	-	SPI1_SCK	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PE14	-	-	-	-	-	SPI1_MISO	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PE15	-	-	-	-	-	SPI1_MOSI	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PH0-OSC_IN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

5 Memory mapping

The memory map is shown in the following figure.

Figure 9. Memory map



6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in *Figure 14: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code, unless otherwise specified.

The current consumption values are derived from the tests performed under ambient temperature T_A=25°C and V_{DD} supply voltage conditions summarized in *Table 14: General operating conditions*, unless otherwise specified.

The MCU is placed under the following conditions:

- All I/O pins are configured in analog input mode.
- All peripherals are disabled except when explicitly mentioned.
- The Flash memory access time, 64-bit access and prefetch is adjusted depending on f_{HCLK} frequency and voltage range to provide the best CPU performance.
- When the peripherals are enabled $f_{APB1} = f_{APB2} = f_{AHB}$.
- When PLL is ON, the PLL inputs are equal to HSI = 16 MHz (if internal clock is used) or HSE = 16 MHz (if HSE bypass mode is used).
- The HSE user clock applied to OSC_IN input follows the characteristics specified in *Table 27: High-speed external user clock characteristics*.
- For maximum current consumption $V_{DD} = V_{DDA}$ = 3.6 V is applied to all supply pins.
- For typical current consumption $V_{DD} = V_{DDA}$ = 3.0 V is applied to all supply pins if not specified otherwise.

Table 24. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions		Typ(1)	Max (1)(2)	Unit
I_{DD} (Standby with RTC)	Supply current in Standby mode with RTC enabled	RTC clocked by LSI (no independent watchdog)	T_A = -40 °C to 25 °C V_{DD} = 1.8 V	0.865	-	µA
			T_A = -40 °C to 25 °C	1.11	1.9	
			T_A = 55 °C	1.15	2.2	
			T_A= 85 °C	1.35	4	
			T_A = 105 °C	1.93	8.3(3)	
		RTC clocked by LSE (no independent watchdog)(4)	T_A = -40 °C to 25 °C V_{DD} = 1.8 V	0.97	-	
			T_A = -40 °C to 25 °C	1.28	-	
			T_A = 55 °C	1.4	-	
			T_A= 85 °C	1.7	-	
			T_A = 105 °C	2.34	-	
I_{DD} (Standby)	Supply current in Standby mode with RTC disabled	Independent watchdog and LSI enabled	T_A = -40 °C to 25 °C	1.0	1.7	
		Independent watchdog and LSI OFF	T_A = -40 °C to 25 °C	0.277	0.6	
			T_A = 55 °C	0.31	0.9	
			T_A = 85 °C	0.52	2.75	
			T_A = 105 °C	1.09	7(3)	
I_{DD} (WU from Standby)	RMS supply current during wakeup time when exiting from Standby mode	-	V_{DD} = 3.0 V T_A = -40 °C to 25 °C	1	-	mA

1. The typical values are given for V_{DD} = 3.0 V and max values are given for V_{DD} = 3.6 V, unless otherwise specified.
2. Guaranteed by characterization results, unless otherwise specified.
3. Guaranteed by test in production.
4. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8pF loading capacitors.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on

Table 25. Peripheral current consumption(1)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}= 1.8 V VOS[1:0] = 01	Range 2, V_{CORE}= 1.5 V VOS[1:0] = 10	Range 3, V_{CORE}= 1.2 V VOS[1:0] = 11	Low-power sleep and run	
APB1	TIM2	11.3	9.0	7.3	9.0	µA/MHz (f_{HCLK})
	TIM3	11.4	9.1	7.1	9.1	
	TIM4	11.3	9.0	7.3	9.0	
	TIM6	3.9	3.1	2.5	3.1	
	TIM7	4.2	3.3	2.6	3.3	
	LCD	4.7	3.6	2.9	3.6	
	WWDG	3.7	2.9	2.4	2.9	
	SPI2	5.9	4.8	3.9	4.8	
	USART2	8.1	6.6	5.1	6.6	
	USART3	7.9	6.4	5.0	6.4	
	I2C1	7.8	6.1	4.9	6.1	
	I2C2	7.2	5.7	4.6	5.7	
	USB	12.7	10.3	8.1	10.3	
	PWR	3.1	2.4	2.0	2.4	
	DAC	6.6	5.3	4.3	5.3	
	COMP	5.3	4.3	3.4	4.3	
APB2	SYSCFG & RI	2.2	1.9	1.6	1.9	µA/MHz (f_{HCLK})
	TIM9	9.1	7.3	5.9	7.3	
	TIM10	6.0	4.9	3.9	4.9	
	TIM11	5.8	4.6	3.8	4.6	
	ADC(2)	8.7	7.0	5.6	7.0	
	SPI1	4.4	3.4	2.8	3.4	
	USART1	8.1	6.5	5.2	6.5	
AHB	GPIOA	4.4	3.5	2.9	3.5	
	GPIOB	4.4	3.5	2.9	3.5	
	GPIOC	3.7	3.0	2.5	3.0	
	GPIOD	3.6	2.8	2.4	2.8	
	GPIOE	4.7	3.8	3.1	3.8	
	GPIOH	3.7	2.9	2.4	2.9	
	CRC	0.6	0.4	0.4	0.4	
	FLASH	12.2	10.2	7.8	-(3)	
	DMA1	12.4	10.1	8.2	10.1	
All enabled		160	135	103	124.8	

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.13*. However, the recommended clock input waveform is shown in *Figure 15*.

Table 27. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	CSS is on or PLL is used	1	8	32	MHz
		CSS is off, PLL not used	0			
V_{HSEH}	OSC_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time		12	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance	-	-	2.6	-	pF

1. Guaranteed by design.

Figure 15. High-speed external clock source AC timing diagram

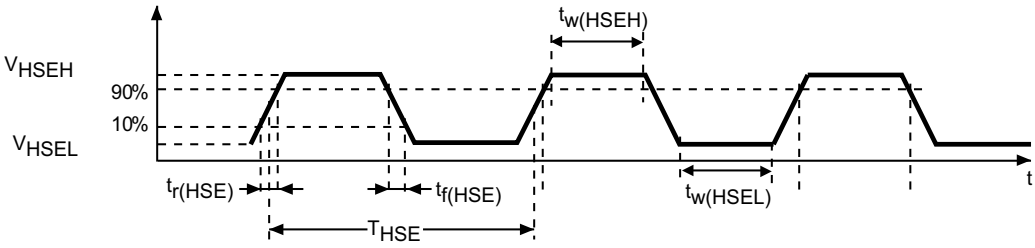


Table 29. HSE oscillator characteristics(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω	-	20	-	pF
I_{HSE}	HSE driving current	V_{DD}= 3.3 V, V_{IN} = V_{SS} with 30 pF load	-	-	3	mA
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.7 (stabilized)	mA
		C = 10 pF f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.46 (stabilized)	
g_m	Oscillator transconductance	Startup	3.5	-	-	mA /V
$t_{SU(HSE)}$ (4)	Startup time	V_{DD} is stabilized	-	1	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 17*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

6.3.13 I/O port characteristics

General input/output characteristics

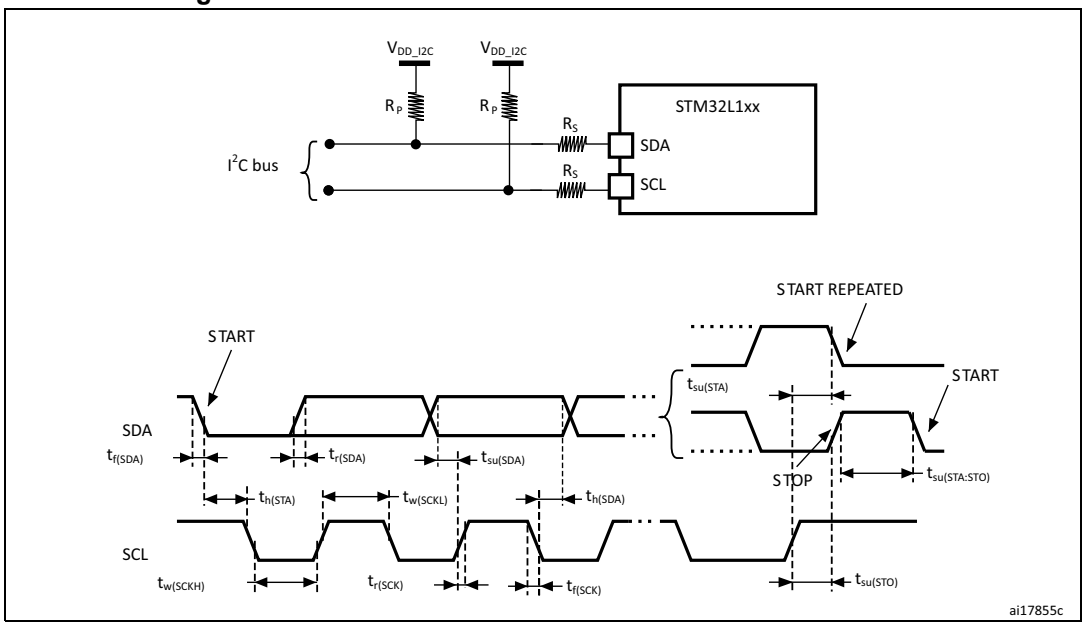
Unless otherwise specified, the parameters given in *Table 43* are derived from tests performed under conditions summarized in *Table 14*. All I/Os are CMOS and TTL compliant.

Table 43. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TC and FT I/O	-	-	0.3 V_{DD}(1)(2)	V
		BOOT0	-		0.14 V_{DD}(2)	
V_{IH}	Input high level voltage	TC I/O	0.45 V_{DD}+0.38(2)	-	-	
		FT I/O	0.39 V_{DD}+0.59(2)	-	-	
		BOOT0	0.15 V_{DD}+0.56(2)	-	-	
V_{hys}	I/O Schmitt trigger voltage hysteresis(2)	TC and FT I/O	-	10% V_{DD}(3)	-	
		BOOT0	-	0.01	-	
I_{lkg}	Input leakage current(4)	$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with LCD	-	-	±50	nA
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with analog switches	-	-	±50	
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with analog switches and LCD	-	-	±50	
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with USB	-	-	±250	
		$V_{SS} \le V_{IN} \le V_{DD}$ TC and FT I/O	-	-	±50	
		FT I/O $V_{DD} \le V_{IN} \le 5V$	-	-	±10	uA
R_{PU}	Weak pull-up equivalent resistor(5)(1)	$V_{IN} = V_{SS}$	30	45	60	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN} = V_{DD}$	30	45	60	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Guaranteed by test in production.
2. Guaranteed by design.
3. With a minimum of 200 mV.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

Figure 21. I²C bus AC waveforms and measurement circuit



1. R_S = series protection resistors
2. R_P = pull-up resistors
3. V_{DD_I2C} = I2C bus supply
4. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 49. SCL frequency (f_{PCLK1}= 32 MHz, V_{DD} = V_{DD_I2C} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801B
300	0x8024
200	0x8035
100	0x00A0
50	0x0140
20	0x0320

1. R_P = External pull-up resistance, f_{SCL} = I²C speed.
2. For speeds around 200 kHz, the tolerance on the achieved speed is ±5%. For other speed ranges, the tolerance on the achieved speed is ±2%. These variations depend on the accuracy of the external components used to design the application.

6.3.20 Comparator

Table 61. Comparator 1 characteristics

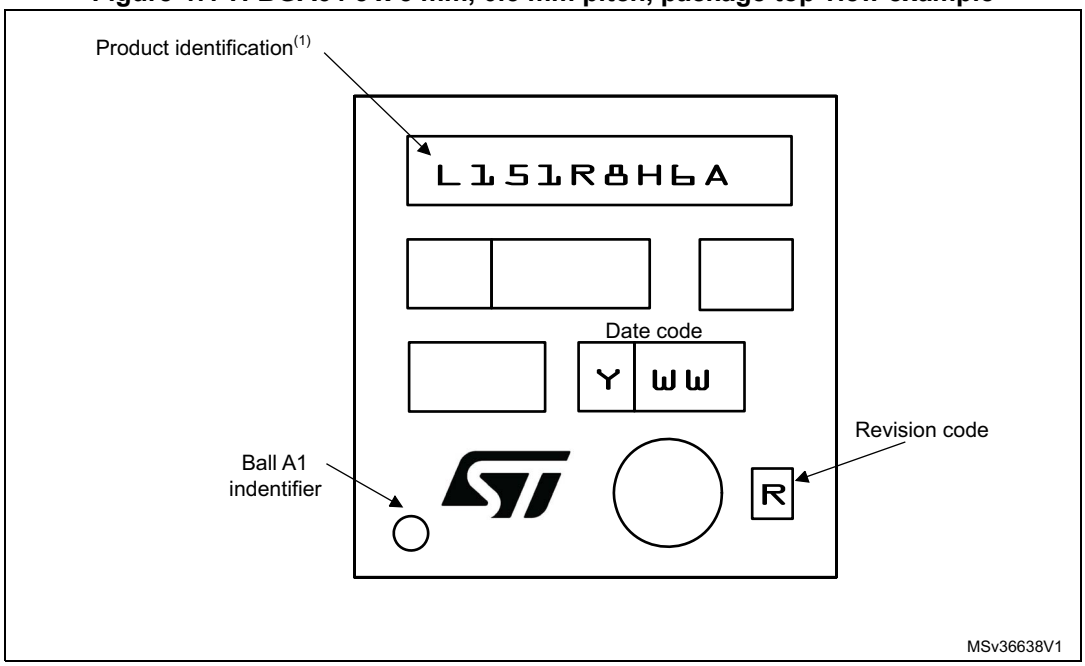
Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65		3.6	V
R_{400K}	R_{400K} value	-	-	400	-	kΩ
R_{10K}	R_{10K} value	-	-	10	-	
V_{IN}	Comparator 1 input voltage range	-	0.6	-	V_{DDA}	V
t_{START}	Comparator startup time	-	-	7	10	µs
td	Propagation delay(2)	-	-	3	10	
Voffset	Comparator offset	-	-	±3	±10	mV
$d_{Voffset}/dt$	Comparator offset variation in worst voltage stress conditions	V_{DDA} = 3.6 V V_{IN+} = 0 V V_{IN-} = V_{REFINT} T_A = 25 °C	0	1.5	10	mV/1000 h
I_{COMP1}	Current consumption(3)	-	-	160	260	nA

1. Guaranteed by characterization results.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

TFBGA64 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Figure 47. TFBGA64 5 x 5 mm, 0.5 mm pitch, package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.7 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max × Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ((V_{DD} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 72. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** UFBGA100 - 7 x 7 mm	59	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 x 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient TFBGA64 - 5 x 5 mm	65	
	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm / 0.5 mm pitch	45	
	Thermal resistance junction-ambient LQFP48 - 7 x 7 mm / 0.5 mm pitch	55	
	Thermal resistance junction-ambient UFQFPN48 - 7 x 7 mm / 0.5 mm pitch	33	

Table 74. Document revision history (continued)

Date	Revision	Changes
25-Apr-2016	4	Updated *Section 7: Package information* structure: Paragraph titles and paragraph heading level. Updated *Section 7: Package information* for all package device markings, adding text for device orientation versus pin 1/ ball A1 identifier. Updated *Figure 32: LQFP100 14 x 14 mm, 100-pin package top view example* removing gate mark. Updated *Table 65: LQFP64 10 x 10 mm, 64-pin low-profile quad flat package mechanical data*. Updated *Section 7.5: UFBGA100 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package information* adding *Table 69: UFBGA100 7 x 7 mm, 0.5 mm pitch, recommended PCB design rules* and *Figure 43: UFBGA100 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package recommended footprint*. Updated *Section 7.6: TFBGA64 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package information* adding *Table 71: TFBGA64 5 x 5 mm, 0.5 mm pitch, recommended PCB design rules* and changing *Figure 46: TFBGA64, 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package recommended footprint*. Updated *Table 17: Embedded internal reference voltage* temperature coefficient at 100ppm/°C and table note 3: “guaranteed by design” changed by “guaranteed by characterization results”. Updated *Table 62: Comparator 2 characteristics* new maximum threshold voltage temperature coefficient at 100ppm/°C. Updated *Table 40: ESD absolute maximum ratings* CDM class. Updated all the notes, removing ‘not tested in production’. Updated *Table 11: Voltage characteristics* adding note about V_{REF-} pin. Updated *Table 3: Functionalities depending on the operating power supply range* LSI and LSE functionalities putting “Y” in Standby mode. Removed note 1 below *Figure 2: Clock tree*. Updated *Table 58: DAC characteristics* resistive load.