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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I²S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 20x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151rbt6atr

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2 Description

The ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A devices incorporate the connectivity power of the universal serial bus (USB) with the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a frequency of 32 MHz (33.3 DMIPS), a memory protection unit (MPU), high-speed embedded memories (Flash memory up to 128 Kbytes and RAM up to 32 Kbytes) and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

All the devices offer a 12-bit ADC, 2 DACs and 2 ultra-low-power comparators, six general-purpose 16-bit timers and two basic timers, which can be used as time bases.

Moreover, the STM32L151x6/8/B-A and STM32L152x6/8/B-A devices contain standard and advanced communication interfaces: up to two I^2Cs and SPIs, three USARTs and a USB. The STM32L151x6/8/B-A and STM32L152x6/8/B-A devices offer up to 20 capacitive sensing channels to simply add touch sensing functionality to any application.

They also include a real-time clock with sub-second counting and a set of backup registers that remain powered in Standby mode.

Finally, the integrated LCD controller (except STM32L151x6/8/B-A devices) has a built-in LCD voltage generator that allows to drive up to 8 multiplexed LCDs with contrast independent of the supply voltage.

The ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. They are available in the -40 to +85 °C and -40 to +105°C temperature ranges. A comprehensive set of power-saving modes allows the design of low-power applications.

2.1 Device overview

Table 2. Ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A device features and peripheral counts

Peripheral		STM32L15xCxxxA			STM32L15xRxxxA			STM32L15xVxxxA	
Flash (Kbytes)		32	64	128	32	64	128	64	128
Data EEPROM (Kbytes)		4							
RAM (Kbytes)		16	32	32	16	32	32	32	32
Timers	General-purpose	6							
	Basic	2							
Communication interfaces	SPI	2							
	I^2C	2							
	USART	3							
	USB	1							
GPIOs		37			51/50(1)			83	
12-bit synchronized ADC Number of channels		1 14 channels			1 20/19 channels(1)			1 24 channels	
12-bit DAC Number of channels		2 2							
LCD (STM32L152xxxxA Only) COM x SEG		4x16			4x32/4x31(1) 8x28/8x27(1)			4x44 8x40	
Comparator		2							
Capacitive sensing channels		13			20				
Max. CPU frequency		32 MHz							
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 V to 3.6 V without BOR option							
Operating temperatures		Ambient operating temperatures: –40 to +85 °C / –40 to + 105 °C Junction temperature: -40 to +110°C							
Packages		LQFP48, UFQFPN48			LQFP64, TFBGA64			LQFP100, UFBGA100	

1. For TFBGA64 package (instead of PC3 pin there is V_{REF+} pin).

3.7 Memories

The STM32L151x6/8/B-A and STM32L152x6/8/B-A devices have the following features:

- Up to 32 Kbytes of embedded RAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 32, 64 or 128 Kbyte of embedded Flash program memory
  - 4 Kbytes of data EEPROM
  - Options bytes

  The options bytes are used to write-protect or read-out-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (Cortex-M3 JTAG and serial wire) and boot in RAM selection disabled (JTAG fuse)

  The whole non-volatile memory embeds the error correction code (ECC) feature.

  The user area of the Flash memory can be protected against Dbus read access by the PCROP feature (see RM0038 for details).

3.8 DMA (direct memory access)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose timers and ADC.

Table 8. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		TC	Standard 3.3 V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 9. STM32L151x6/8/B-A and STM32L152x6/8/B-A pin definitions (continued)

Pins					Pin name	Pin type(1)	I/O structure	Main function(2) (after reset)	Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48					Alternate functions	Additional functions
51	33	H8	L12	25	PB12	I/O	FT	PB12	SPI2_NSS/I2C2_SMBA/ USART3_CK/ LCD_SEG12/ TIM10_CH1	ADC_IN18/ COMP1_INP /VLCDRAIL2
52	34	G8	K12	26	PB13	I/O	FT	PB13	SPI2_SCK/ USART3_CTS/ LCD_SEG13/TIM9_CH1	ADC_IN19/ COMP1_INP
53	35	F8	K11	27	PB14	I/O	FT	PB14	SPI2_MISO/ USART3_RTS/ LCD_SEG14/TIM9_CH2	ADC_IN20/ COMP1_INP
54	36	F7	K10	28	PB15	I/O	FT	PB15	SPI2_MOSI/ LCD_SEG15/ TIM11_CH1	ADC_IN21/ COMP1_INP/ RTC_REFIN
55	-	-	K9	-	PD8	I/O	FT	PD8	USART3_TX/ LCD_SEG28	-
56	-	-	K8	-	PD9	I/O	FT	PD9	USART3_RX/ LCD_SEG29	-
57	-	-	J12	-	PD10	I/O	FT	PD10	USART3_CK/ LCD_SEG30	-
58	-	-	J11	-	PD11	I/O	FT	PD11	USART3_CTS/ LCD_SEG31	-
59	-	-	J10	-	PD12	I/O	FT	PD12	TIM4_CH1/ USART3_RTS/ LCD_SEG32	-
60	-	-	H12	-	PD13	I/O	FT	PD13	TIM4_CH2/LCD_SEG33	-
61	-	-	H11	-	PD14	I/O	FT	PD14	TIM4_CH3/LCD_SEG34	-
62	-	-	H10	-	PD15	I/O	FT	PD15	TIM4_CH4/LCD_SEG35	-
63	37	F6	E12	-	PC6	I/O	FT	PC6	TIM3_CH1/LCD_SEG24	-
64	38	E7	E11	-	PC7	I/O	FT	PC7	TIM3_CH2/LCD_SEG25	-
65	39	E8	E10	-	PC8	I/O	FT	PC8	TIM3_CH3/LCD_SEG26	-
66	40	D8	D12	-	PC9	I/O	FT	PC9	TIM3_CH4/LCD_SEG27	-

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

Please refer to device ErrataSheet for possible latest changes of electrical characteristics.

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.0 V (for the 1.65 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

Figure 10. Pin loading conditions

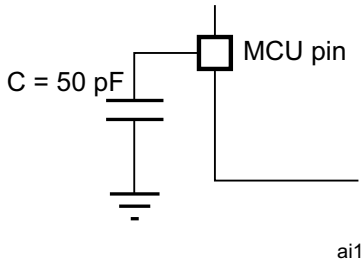
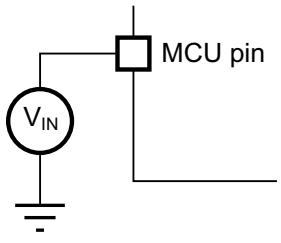


Figure 11. Pin input voltage



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 11: Voltage characteristics*, *Table 12: Current characteristics*, and *Table 13: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 11. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}(2)	Input voltage on five-volt tolerant pin	V_{SS} –0.3	V_{DD}+4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all different ground pins(3)	-	50	
V_{REF+} –V_{DDA}	Allowed voltage difference for V_{REF+} > V_{DDA}	-	0.4	V
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.11*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 12* for maximum allowed injected current values.
3. Include V_{REF-} pin.

Table 12. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all V_{DD_x} power lines (source)(1)	100	mA
ΣI_{VSS}(2)	Total current out of sum of all V_{SS_x} ground lines (sink)(1)	100	
$I_{VDD(PIN)}$	Maximum current into each V_{DD_x} power pin (source)(1)	70	
$I_{VSS(PIN)}$	Maximum current out of each V_{SS_x} ground pin (sink)(1)	-70	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	- 25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins(2)	60	
	Total output current sourced by sum of all IOs and control pins(2)	-60	
$I_{INJ(PIN)}$ (3)	Injected current on five-volt tolerant I/O(4) RST and B pins	-5/+0	
	Injected current on any other pin(5)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.

Table 19. Current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Run from RAM)	Supply current in Run mode, code executed from RAM, Flash switched off	$f_{HSE} = f_{HCLK}$ up to 16 MHz, included $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	185	255	µA
				2 MHz	345	435	
				4 MHz	645	930	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	0.755	1.5	mA
				8 MHz	1.5	2.2	
				16 MHz	3.0	3.6	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	1.8	2.9	
				16 MHz	3.6	4.3	
				32 MHz	7.15	8.5	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	2.95	3.7	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	7.15	8.7	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	65 kHz	39	115	µA
		MSI clock, 524 kHz		524 kHz	110	205	
		MSI clock, 4.2 MHz		4.2 MHz	690	870	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 24. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions		Typ(1)	Max (1)(2)	Unit
I_{DD} (Standby with RTC)	Supply current in Standby mode with RTC enabled	RTC clocked by LSI (no independent watchdog)	T_A = -40 °C to 25 °C V_{DD} = 1.8 V	0.865	-	µA
			T_A = -40 °C to 25 °C	1.11	1.9	
			T_A = 55 °C	1.15	2.2	
			T_A= 85 °C	1.35	4	
			T_A = 105 °C	1.93	8.3(3)	
		RTC clocked by LSE (no independent watchdog)(4)	T_A = -40 °C to 25 °C V_{DD} = 1.8 V	0.97	-	
			T_A = -40 °C to 25 °C	1.28	-	
			T_A = 55 °C	1.4	-	
			T_A= 85 °C	1.7	-	
			T_A = 105 °C	2.34	-	
I_{DD} (Standby)	Supply current in Standby mode with RTC disabled	Independent watchdog and LSI enabled	T_A = -40 °C to 25 °C	1.0	1.7	
		Independent watchdog and LSI OFF	T_A = -40 °C to 25 °C	0.277	0.6	
			T_A = 55 °C	0.31	0.9	
			T_A = 85 °C	0.52	2.75	
			T_A = 105 °C	1.09	7(3)	
I_{DD} (WU from Standby)	RMS supply current during wakeup time when exiting from Standby mode	-	V_{DD} = 3.0 V T_A = -40 °C to 25 °C	1	-	mA

1. The typical values are given for V_{DD} = 3.0 V and max values are given for V_{DD} = 3.6 V, unless otherwise specified.
2. Guaranteed by characterization results, unless otherwise specified.
3. Guaranteed by test in production.
4. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8pF loading capacitors.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.13*. However, the recommended clock input waveform is shown in *Figure 15*.

Table 27. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	CSS is on or PLL is used	1	8	32	MHz
		CSS is off, PLL not used	0			
V_{HSEH}	OSC_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time		12	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance	-	-	2.6	-	pF

1. Guaranteed by design.

Figure 15. High-speed external clock source AC timing diagram

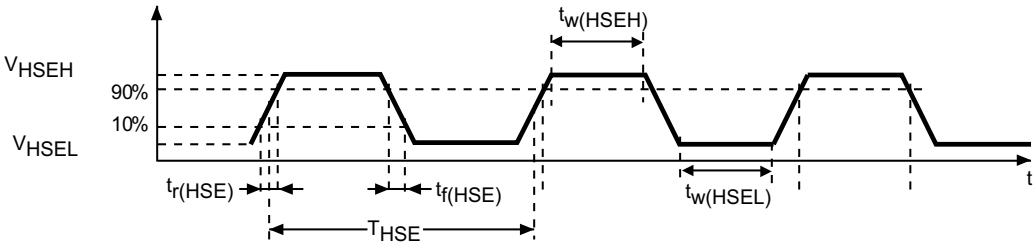


Table 29. HSE oscillator characteristics(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω	-	20	-	pF
I_{HSE}	HSE driving current	V_{DD}= 3.3 V, V_{IN} = V_{SS} with 30 pF load	-	-	3	mA
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.7 (stabilized)	mA
		C = 10 pF f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.46 (stabilized)	
g_m	Oscillator transconductance	Startup	3.5	-	-	mA /V
$t_{SU(HSE)}$ (4)	Startup time	V_{DD} is stabilized	-	1	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 17*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 39. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. frequency range			Unit
				4 MHz voltage Range 3	16 MHz voltage Range 2	32 MHz voltage Range 1	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 to 30 MHz	-16	-7	-3	dBµV
			30 to 130 MHz	-12	2	12	
			130 MHz to 1GHz	-11	0	8	
			SAE EMI Level	1	1.5	2	-

6.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

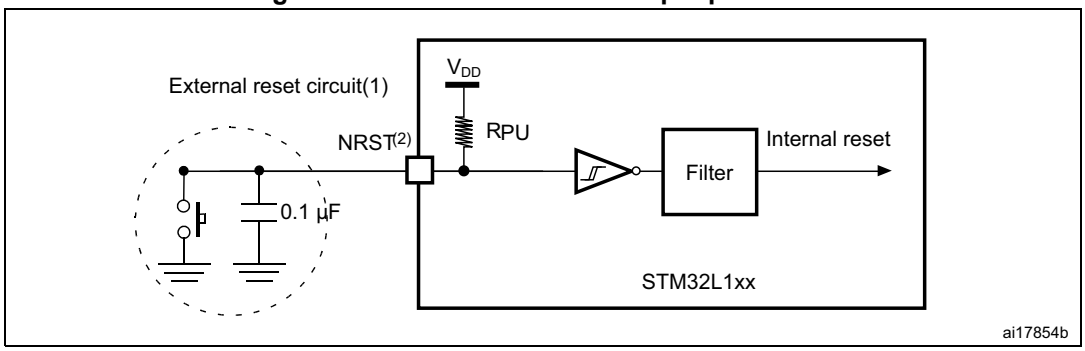
Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114, ANSI/ESD STM5.3.1 standard.

Table 40. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Packages	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	All	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	All	C4	500	V

1. Guaranteed by characterization results.

Figure 20. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 46*. Otherwise the reset will not be taken into account by the device.

6.3.15 TIM timer characteristics

The parameters given in *Table 47* are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 47. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	31.25	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 32 MHz	0	16	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected (timer's prescaler disabled)	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	0.0312	2048	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	-	134.2	s

1. TIMx is used as a general term to refer to the TIM2, TIM3 and TIM4 timers.

Figure 22. SPI timing diagram - slave mode and CPHA = 0

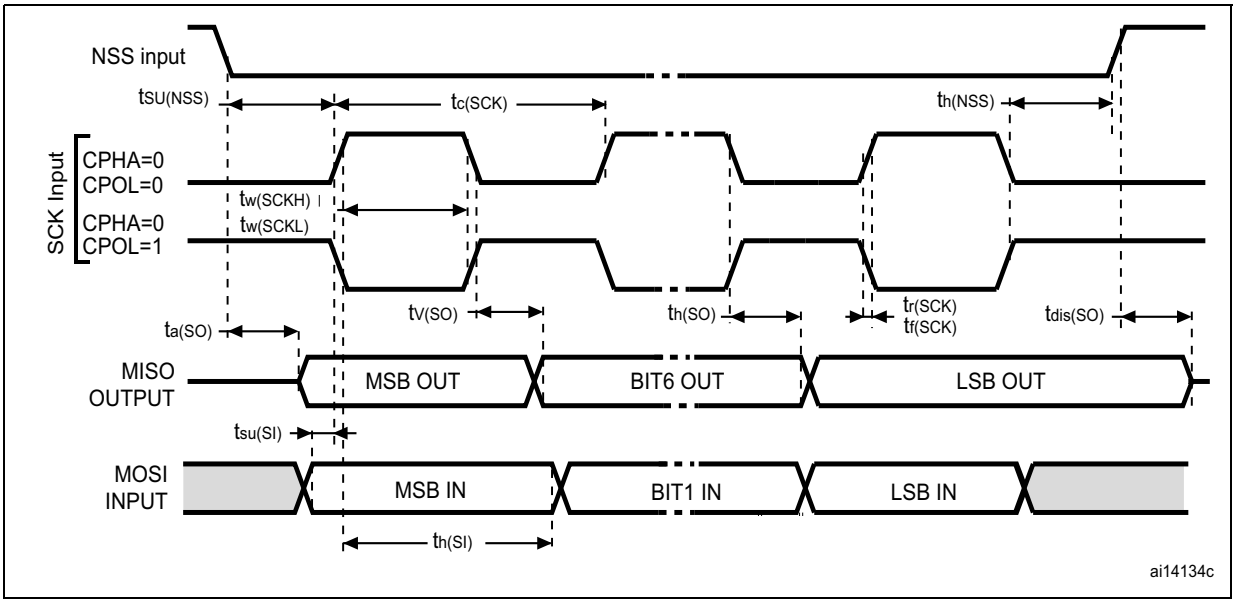
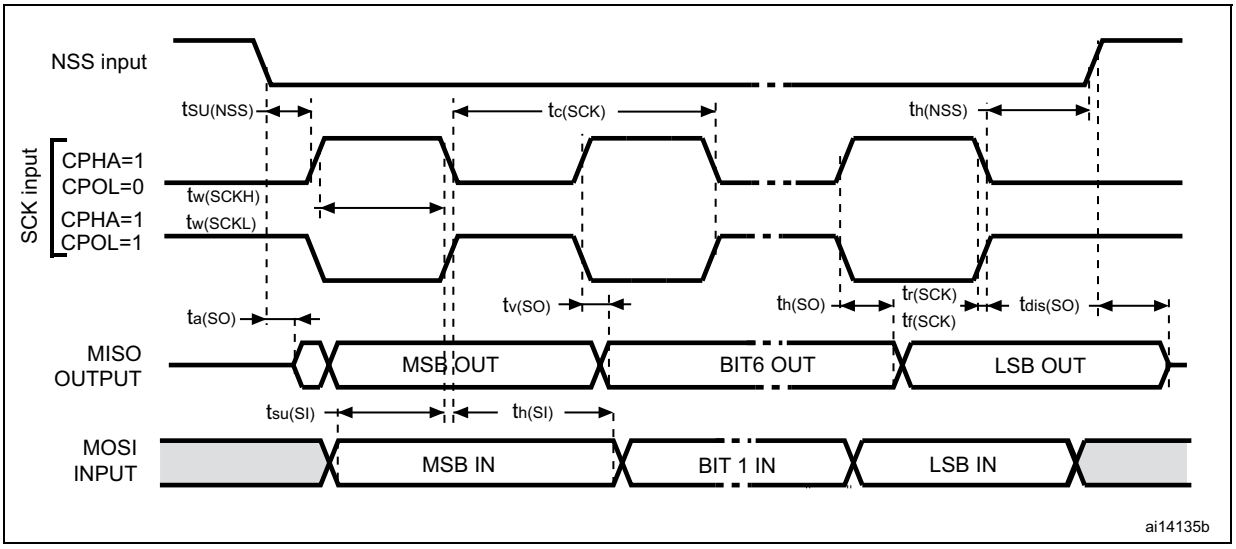


Figure 23. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

6.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 55* are guaranteed by design.

Table 54. ADC clock frequency

Symbol	Parameter	Conditions			Min	Max	Unit
f_{ADC}	ADC clock frequency	Voltage Range 1 & 2	2.4 V ≤V_{DDA} ≤3.6 V	V_{REF+} = V_{DDA}	0.480	16	MHz
				V_{REF+} < V_{DDA} V_{REF+} > 2.4 V		8	
				V_{REF+} < V_{DDA} V_{REF+} ≤2.4 V		4	
			1.8 V ≤V_{DDA} ≤2.4 V	V_{REF+} = V_{DDA}		8	
				V_{REF+} < V_{DDA}		4	
		Voltage Range 3				4	

Table 55. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	1.8	-	3.6	V
V_{REF+}	Positive reference voltage	2.4 V ≤V_{DDA} ≤3.6 V V_{REF+} must be below or equal to V_{DDA}	1.8(1)	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	-	V_{SSA}	-	V
I_{VDDA}	Current on the V_{DDA} input pin	-	-	1000	1450	µA
I_{VREF}(2)	Current on the V_{REF} input pin	Peak	-	400	700	µA
		Average	-		450	µA
V_{AIN}	Conversion voltage range(3)	-	0(4)	-	V_{REF+}	V
f_S	12-bit sampling rate	Direct channels	-	-	1	Msps
		Multiplexed channels	-	-	0.76	
	10-bit sampling rate	Direct channels	-	-	1.07	Msps
		Multiplexed channels	-	-	0.8	
	8-bit sampling rate	Direct channels	-	-	1.23	Msps
		Multiplexed channels	-	-	0.89	
	6-bit sampling rate	Direct channels	-	-	1.45	Msps
		Multiplexed channels	-	-	1	

6.3.18 DAC electrical specifications

Data guaranteed by design, unless otherwise specified.

Table 58. DAC characteristics

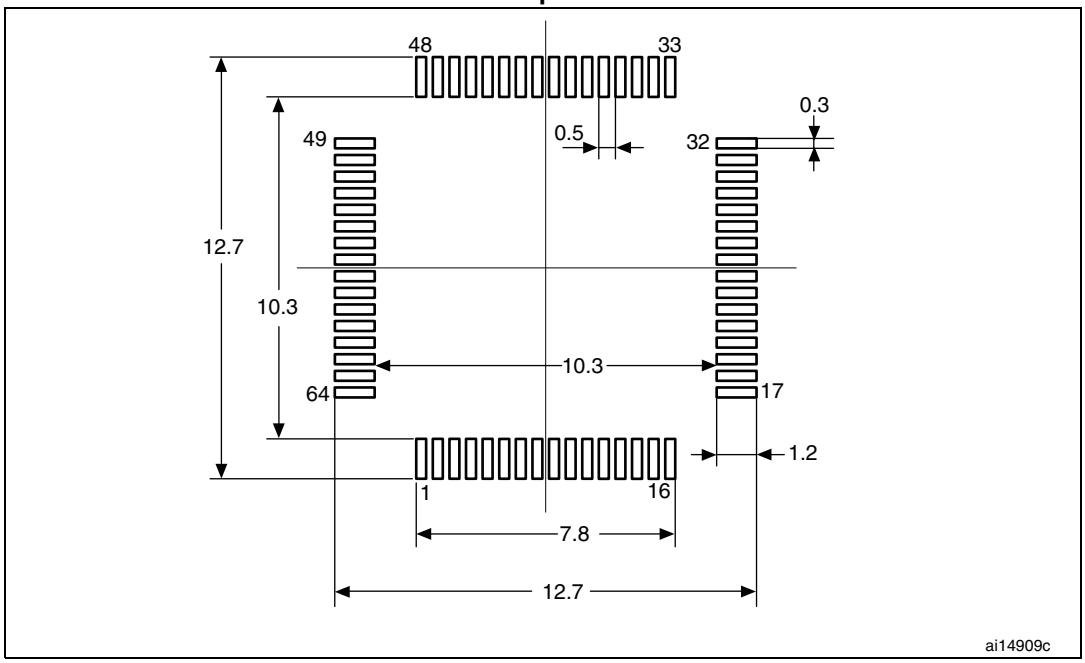
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.8	-	3.6	V
V_{REF+}	Reference supply voltage	V_{REF+} must always be below V_{DDA}		1.8	-	3.6	V
V_{REF-}	Lower reference voltage	-		V_{SSA}			V
$I_{DDVREF+}$(1)	Current consumption on V_{REF+} supply V_{REF+} = 3.3 V	No load, middle code (0x800)		-	130	220	µA
		No load, worst code (0x000)		-	220	350	µA
I_{DDA}(1)	Current consumption on V_{DDA} supply V_{DDA} = 3.3 V	No load, middle code (0x800)		-	210	320	µA
		No load, worst code (0xF1C)		-	320	520	µA
R_L	Resistive load	DAC output buffer ON	Connected to V_{SSA}	5	-	-	kΩ
			Connected to V_{DDA}	25	-	-	
C_L	Capacitive load	DAC output buffer ON		-	-	50	pF
R_O	Output impedance	DAC output buffer OFF		12	16	20	kΩ
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{DDA} – 0.2	V
		DAC output buffer OFF		0.5	-	V_{REF+}– 1LSB	mV
DNL(1)	Differential non linearity(2)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON		-	1.5	3	LSB
		No R_L, $C_L \leq 50$ pF DAC output buffer OFF		-	1.5	3	
INL(1)	Integral non linearity(3)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON		-	2	4	
		No R_L, $C_L \leq 50$ pF DAC output buffer OFF		-	2	4	
Offset(1)	Offset error at code 0x800 (4)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON		-	±10	±25	
		No R_L, $C_L \leq 50$ pF DAC output buffer OFF		-	±5	±8	
Offset1(1)	Offset error at code 0x001(5)	No R_L, $C_L \leq 50$ pF DAC output buffer OFF		-	±1.5	±5	

Table 65. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Typ	Min	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 34. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package recommended footprint



1. Dimensions are in millimeters.

7.7 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max × Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ((V_{DD} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 72. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** UFBGA100 - 7 x 7 mm	59	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 x 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient TFBGA64 - 5 x 5 mm	65	
	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm / 0.5 mm pitch	45	
	Thermal resistance junction-ambient LQFP48 - 7 x 7 mm / 0.5 mm pitch	55	
	Thermal resistance junction-ambient UFQFPN48 - 7 x 7 mm / 0.5 mm pitch	33	

8 Ordering information

Table 73. Ordering information scheme

Example: STM32 L 152 R B T 6 A D TR

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

L = Low-power

Device subfamily

151: Devices without LCD

152: Devices with LCD

Pin count

C = 48 pins

R = 64 pins

V = 100 pins

Flash memory size

6 = 32 Kbytes of Flash memory

8 = 64 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

Package

H = BGA

T = LQFP

U = UFQFPN

Temperature range

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

Options

A = device generation A

No character = VDD range: 1.8 to 3.6 V and BOR enabled

D = VDD range: 1.65 to 3.6 V and BOR disabled

Packing

TR = tape and reel

No character = tray or tube

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.