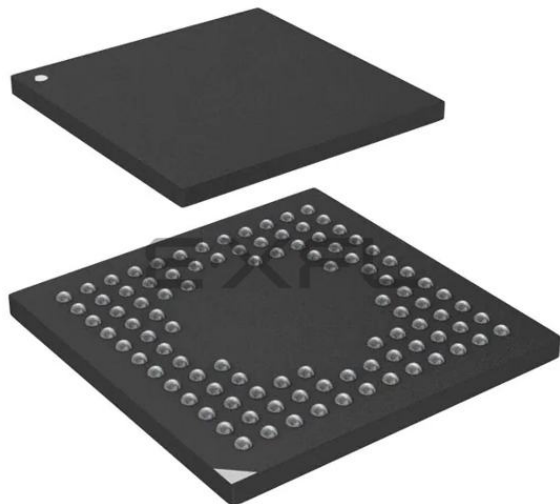




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I ² S, POR, PWM, WDT
Number of I/O	83
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA
Supplier Device Package	100-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151v8h6a

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L151x6/8/B-A and STM32L152x6/8/B-A ultra-low-power ARM® Cortex®-M3 based microcontrollers product line.

The ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A microcontroller family includes devices in 3 different package types: from 48 to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A microcontroller family suitable for a wide range of applications:

- Medical and handheld equipment
- Application control and user interface
- PC peripherals, gaming, GPS and sport equipment
- Alarm systems, Wired and wireless sensors, Video intercom
- Utility metering

This STM32L151x6/8/B-A and STM32L152x6/8/B-A datasheet should be read in conjunction with the STM32L1xxxx reference manual (RM0038). The document "Getting started with STM32L1xxxx hardware development" AN3216 gives a hardware implementation overview.

Both documents are available from the STMicroelectronics website www.st.com.

For information on the ARM® Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the ARM website.

Figure 1 shows the general block diagram of the device family.

Caution: This datasheet does not apply to:
– STM32L15xx6/8/B
covered by a separate datasheet.

line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB wakeup.

Stop mode consumption: refer to [Table 23](#).

- **Standby mode with RTC**

Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI RC and HSE crystal oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

The device exits Standby mode in 60 μ s when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby mode without RTC**

Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI, RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

The device exits Standby mode in 60 μ s when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Standby mode consumption: refer to [Table 24](#).

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering the Stop or Standby mode.

Table 3. Functionalities depending on the operating power supply range

Operating power supply range	Functionalities depending on the operating power supply range			
	DAC and ADC operation	USB	Dynamic voltage scaling range	I/O operation
$V_{DD} = 1.65$ to 1.71 V	Not functional	Not functional	Range 2 or Range 3	Degraded speed performance
$V_{DD} = 1.71$ to 1.8 V ⁽¹⁾	Not functional	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance
$V_{DD} = 1.8$ to 2.0 V ⁽¹⁾	Conversion time up to 500 Ksps	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance

Figure 2. Clock tree

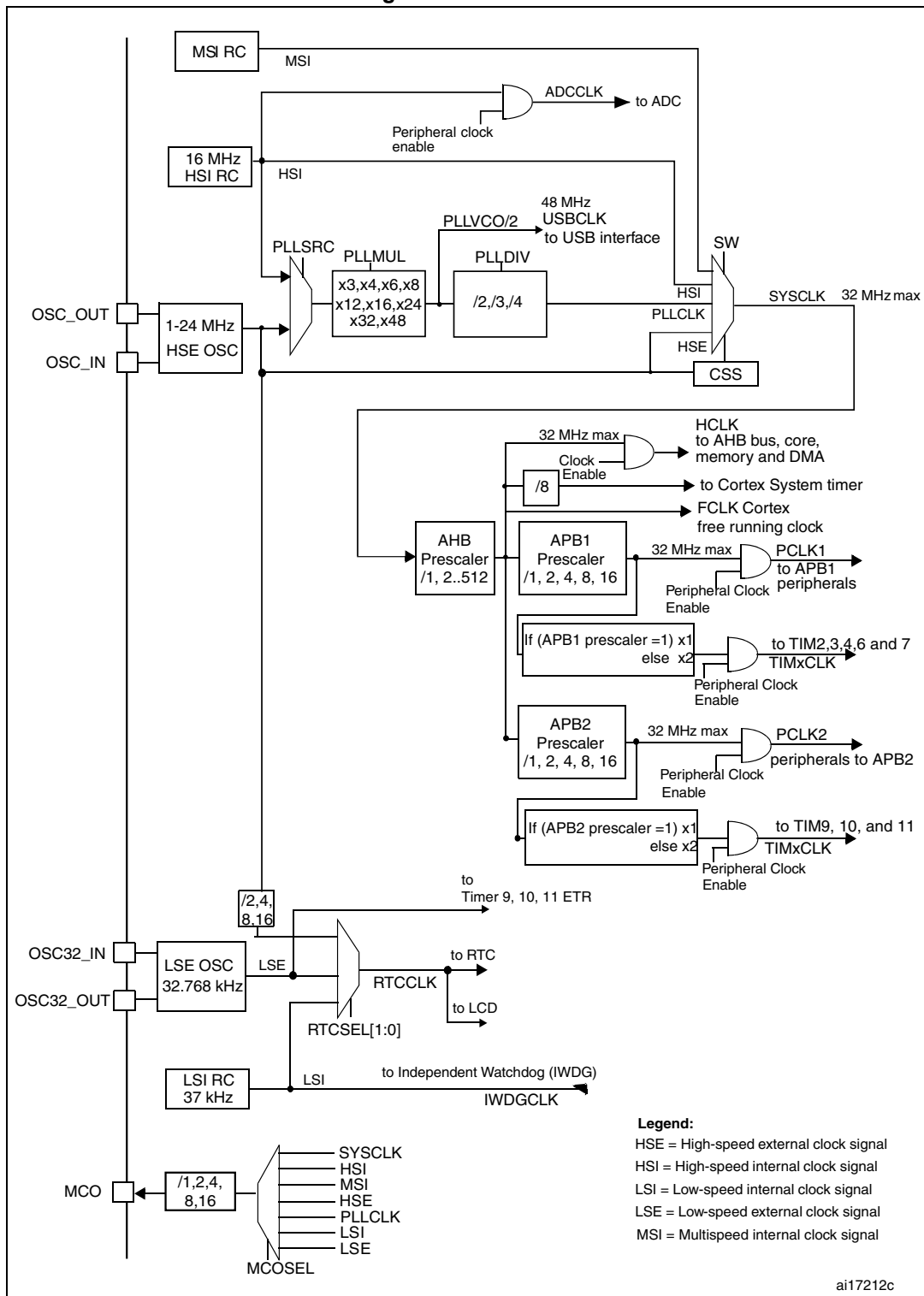




Table 10. Alternate function input/output (continued)

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8	AFIO9	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
PC10	-	-	-	-	-	-	-	USART3_TX	-	-	COM4 / SEG28 / SEG40	-	-	TIMx_IC3	EVENTOUT
PC11	-	-	-	-	-	-	-	USART3_RX	-	-	COM5 / SEG29 / SEG41	-	-	TIMx_IC4	EVENTOUT
PC12	-	-	-	-	-	-	-	USART3_CK	-	-	COM6 / SEG30 / SEG42	-	-	TIMx_IC1	EVENTOUT
PC13-WKUP2	-	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PC14-OSC32_IN	-	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PC15-OSC32_OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PD0	-	-	-	TIM9_CH1	-	SPI2_NSS	-	-	-	-	-	-	-	TIMx_IC1	EVENTOUT
PD1	-	-	-	-	-	SPI2_SCK	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PD2	-	-	TIM3_ETR	-	-	-	-	-	-	-	COM7 / SEG31 / SEG43	-	-	TIMx_IC3	EVENTOUT
PD3	-	-	-	-	-	SPI2_MISO	-	USART2_CTS	-	-	-	-	-	TIMx_IC4	EVENTOUT
PD4	-	-	-	-	-	SPI2_MOSI	-	USART2_RTS	-	-	-	-	-	TIMx_IC1	EVENTOUT
PD5	-	-	-	-	-	-	-	USART2_TX	-	-	-	-	-	TIMx_IC2	EVENTOUT
PD6	-	-	-	-	-	-	-	USART2_RX	-	-	-	-	-	TIMx_IC3	EVENTOUT
PD7	-	-	-	TIM9_CH2	-	-	-	USART2_CK	-	-	-	-	-	TIMx_IC4	EVENTOUT
PD8	-	-	-	-	-	-	-	USART3_TX	-	-	-	-	-	TIMx_IC1	EVENTOUT
PD9	-	-	-	-	-	-	-	USART3_RX	-	-	-	-	-	TIMx_IC2	EVENTOUT

Table 10. Alternate function input/output (continued)

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8	AFIO9	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
PD10	-	-	-	-	-	-	-	USART3_CK	-	-	-	-	-	TIMx_IC3	EVENTOUT
PD11	-	-	-	-	-	-	-	USART3_CTS	-	-	-	-	-	TIMx_IC4	EVENTOUT
PD12	-	-	TIM4_CH1	-	-	-	-	USART3_RTS	-	-	-	-	-	TIMx_IC1	EVENTOUT
PD13	-	-	TIM4_CH2	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PD14	-	-	TIM4_CH3	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PD15	-	-	TIM4_CH4	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PE0	-	-	TIM4_ETR	TIM10_CH1	-	-	-	-	-	-	-	-	-	TIMx_IC1	EVENTOUT
PE1	-	-	-	TIM11_CH1	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PE2	TRACECK	-	TIM3_ETR	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PE3	TRACED0	-	TIM3_CH1	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PE4	TRACED1	-	TIM3_CH2	-	-	-	-	-	-	-	-	-	-	TIMx_IC1	EVENTOUT
PE5	TRACED2	-	-	TIM9_CH1*	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PE6	TRACED3	-	-	TIM9_CH2*	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PE7	-	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PE8	-	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC1	EVENTOUT
PE9	-	TIM2_CH1_ETR	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PE10	-	TIM2_CH2	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PE11	-	TIM2_CH3	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PE12	-	TIM2_CH4	-	-	-	SPI1_NSS	-	-	-	-	-	-	-	TIMx_IC1	EVENTOUT
PE13	-	-	-	-	-	SPI1_SCK	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PE14	-	-	-	-	-	SPI1_MISO	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PE15	-	-	-	-	-	SPI1_MOSI	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PH0-OSC_IN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS} .

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25\text{ }^{\circ}\text{C}$ and $T_A = T_{A\text{max}}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation ($\text{mean} \pm 3\sigma$).

Please refer to device ErrataSheet for possible latest changes of electrical characteristics.

6.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 3.0\text{ V}$ (for the $1.65\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated ($\text{mean} \pm 2\sigma$).

6.1.3 Typical curves

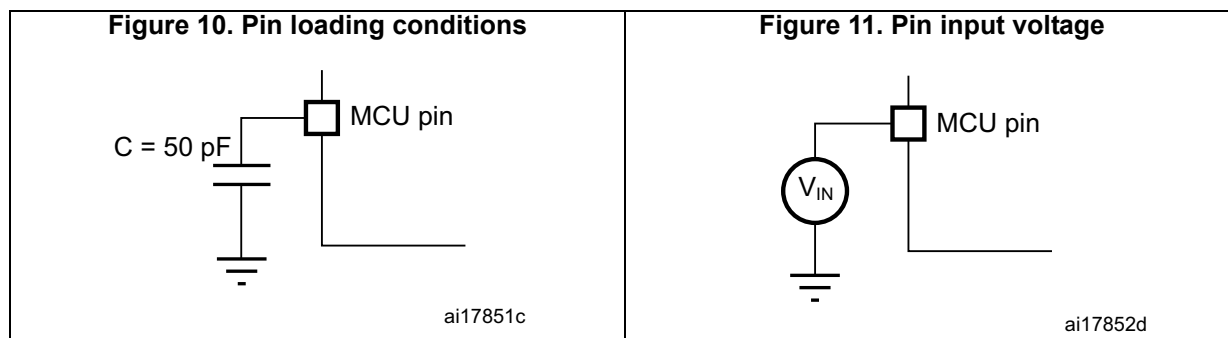
Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 10](#).

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 11](#).



6.1.6 Power supply scheme

Figure 12. Power supply scheme

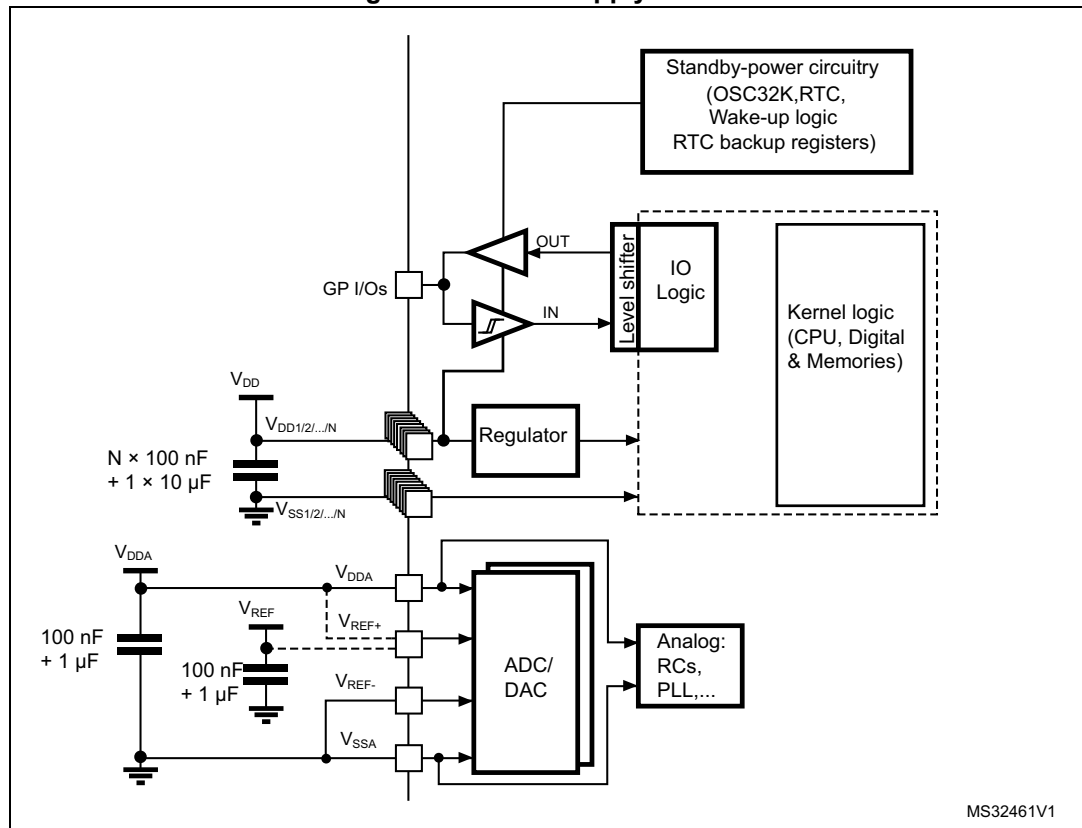


Table 19. Current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions		f _{HCLK}	Typ	Max ⁽¹⁾	Unit
I _{DD} (Run from RAM)	Supply current in Run mode, code executed from RAM, Flash switched off	f _{HSE} = f _{HCLK} up to 16 MHz, included f _{HSE} = f _{HCLK} /2 above 16 MHz (PLL ON) ⁽²⁾	Range 3, V _{CORE} =1.2 V VOS[1:0] = 11	1 MHz	185	255	μA
				2 MHz	345	435	
				4 MHz	645	930	
			Range 2, V _{CORE} =1.5 V VOS[1:0] = 10	4 MHz	0.755	1.5	mA
				8 MHz	1.5	2.2	
				16 MHz	3.0	3.6	
			Range 1, V _{CORE} =1.8 V VOS[1:0] = 01	8 MHz	1.8	2.9	
				16 MHz	3.6	4.3	
				32 MHz	7.15	8.5	
		HSI clock source (16 MHz)	Range 2, V _{CORE} =1.5 V VOS[1:0] = 10	16 MHz	2.95	3.7	
			Range 1, V _{CORE} =1.8 V VOS[1:0] = 01	32 MHz	7.15	8.7	
		MSI clock, 65 kHz	Range 3, V _{CORE} =1.2 V VOS[1:0] = 11	65 kHz	39	115	μA
		MSI clock, 524 kHz		524 kHz	110	205	
		MSI clock, 4.2 MHz		4.2 MHz	690	870	

1. Guaranteed by characterization results, unless otherwise specified.

2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 23. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions			Typ ⁽¹⁾	Max ⁽¹⁾⁽²⁾	Unit
I_{DD} (Stop with RTC)	Supply current in Stop mode with RTC enabled	RTC clocked by LSI, regulator in LP mode, HSI and HSE OFF (no independent watchdog)	LCD OFF	$T_A = -40^{\circ}\text{C}$ to 25°C $V_{DD} = 1.8\text{ V}$	1.13	-	μA
				$T_A = -40^{\circ}\text{C}$ to 25°C	1.38	4	
				$T_A = 55^{\circ}\text{C}$	1.70	6	
				$T_A = 85^{\circ}\text{C}$	3.30	10	
				$T_A = 105^{\circ}\text{C}$	7.80	23	
			LCD ON (static duty) ⁽³⁾	$T_A = -40^{\circ}\text{C}$ to 25°C	1.50	6	
				$T_A = 55^{\circ}\text{C}$	1.80	7	
				$T_A = 85^{\circ}\text{C}$	3.45	12	
				$T_A = 105^{\circ}\text{C}$	8.02	27	
		LCD ON (1/8 duty) ⁽⁴⁾		$T_A = -40^{\circ}\text{C}$ to 25°C	3.80	10	
				$T_A = 55^{\circ}\text{C}$	4.30	11	
				$T_A = 85^{\circ}\text{C}$	6.10	16	
				$T_A = 105^{\circ}\text{C}$	10.8	44	
		RTC clocked by LSE external clock (32.768 kHz), regulator in LP mode, HSI and HSE OFF (no independent watchdog)	LCD OFF	$T_A = -40^{\circ}\text{C}$ to 25°C	1.50	-	
				$T_A = 55^{\circ}\text{C}$	1.90	-	
				$T_A = 85^{\circ}\text{C}$	3.65	-	
				$T_A = 105^{\circ}\text{C}$	8.25	-	
			LCD ON (static duty) ⁽³⁾	$T_A = -40^{\circ}\text{C}$ to 25°C	1.60	-	
				$T_A = 55^{\circ}\text{C}$	2.05	-	
				$T_A = 85^{\circ}\text{C}$	3.75	-	
				$T_A = 105^{\circ}\text{C}$	8.40	-	
			LCD ON (1/8 duty) ⁽⁴⁾	$T_A = -40^{\circ}\text{C}$ to 25°C	3.90	-	
				$T_A = 55^{\circ}\text{C}$	4.55	-	
				$T_A = 85^{\circ}\text{C}$	6.35	-	
				$T_A = 105^{\circ}\text{C}$	11.10	-	
	RTC clocked by LSE (no independent watchdog) ⁽⁵⁾	LCD OFF		$T_A = -40^{\circ}\text{C}$ to 25°C $V_{DD} = 1.8\text{ V}$	1.23	-	
				$T_A = -40^{\circ}\text{C}$ to 25°C $V_{DD} = 3.0\text{ V}$	1.50	-	
				$T_A = -40^{\circ}\text{C}$ to 25°C $V_{DD} = 3.6\text{ V}$	1.75	-	

Table 26. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ	Max ⁽¹⁾	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	$f_{HCLK} = 32 \text{ MHz}$	0.4	-	μs
$t_{WUSLEEP_LP}$	Wakeup from Low-power sleep mode $f_{HCLK} = 262 \text{ kHz}$	$f_{HCLK} = 262 \text{ kHz}$ Flash enabled	46	-	
		$f_{HCLK} = 262 \text{ kHz}$ Flash switched OFF	46	-	
t_{WUSTOP}	Wakeup from Stop mode, regulator in Run mode	$f_{HCLK} = f_{MSI} = 4.2 \text{ MHz}$	8.2	-	
		$f_{HCLK} = f_{MSI} = 4.2 \text{ MHz}$ Voltage Range 1 and 2	7.7	8.9	
	Wakeup from Stop mode, regulator in low-power mode	$f_{HCLK} = f_{MSI} = 4.2 \text{ MHz}$ Voltage Range 3	8.2	13.1	
		$f_{HCLK} = f_{MSI} = 2.1 \text{ MHz}$	10.2	13.4	
		$f_{HCLK} = f_{MSI} = 1.05 \text{ MHz}$	16	20	
		$f_{HCLK} = f_{MSI} = 524 \text{ kHz}$	31	37	
		$f_{HCLK} = f_{MSI} = 262 \text{ kHz}$	57	66	
		$f_{HCLK} = f_{MSI} = 131 \text{ kHz}$	112	123	
		$f_{HCLK} = f_{MSI} = 65 \text{ kHz}$	221	236	
$t_{WUSTDBY}$	Wakeup from Standby mode FWU bit = 1	$f_{HCLK} = f_{MSI} = 2.1 \text{ MHz}$	58	104	ms
	Wakeup from Standby mode FWU bit = 0	$f_{HCLK} = f_{MSI} = 2.1 \text{ MHz}$	2.6	3.25	

1. Guaranteed by characterization results, unless otherwise specified

Low-speed external user clock generated from an external source

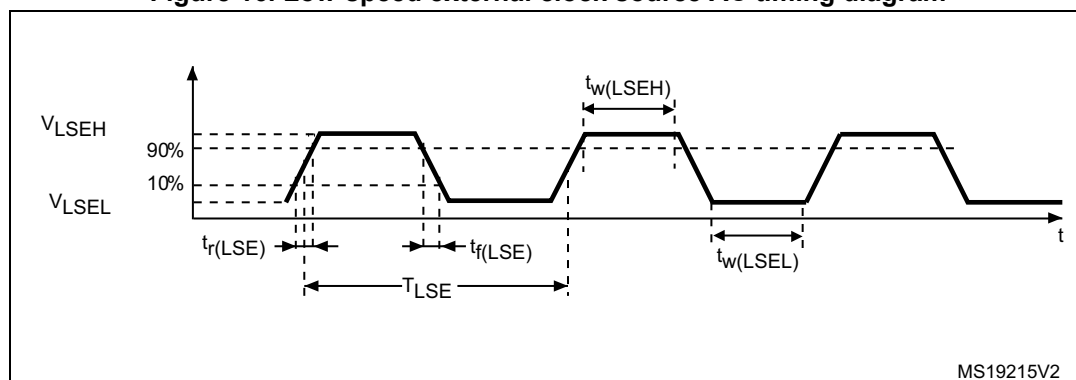
The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 14](#).

Table 28. Low-speed external user clock characteristics⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	1	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	$0.7V_{DD}$	-	V_{DD}	-
V_{LSEL}	OSC32_IN input pin low level voltage	V_{SS}	-	$0.3V_{DD}$	-
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	465	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time	-	-	10	
$C_{IN(LSE)}$	OSC32_IN input capacitance	-	0.6	-	pF

1. Guaranteed by design.

Figure 16. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 1 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 29](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 29. HSE oscillator characteristics⁽¹⁾⁽²⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	1		24	MHz
R_F	Feedback resistor	-		200	-	k Ω

Table 29. HSE oscillator characteristics⁽¹⁾⁽²⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S) ⁽³⁾	$R_S = 30 \Omega$	-	20	-	pF
I_{HSE}	HSE driving current	$V_{DD} = 3.3 \text{ V}$, $V_{IN} = V_{SS}$ with 30 pF load	-	-	3	mA
$I_{DD(HSE)}$	HSE oscillator power consumption	$C = 20 \text{ pF}$ $f_{OSC} = 16 \text{ MHz}$	-	-	2.5 (startup) 0.7 (stabilized)	mA
		$C = 10 \text{ pF}$ $f_{OSC} = 16 \text{ MHz}$	-	-	2.5 (startup) 0.46 (stabilized)	
g_m	Oscillator transconductance	Startup	3.5	-	-	mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized	-	1	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2} , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see [Figure 17](#)). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2} . Refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Note: For CL1 and CL2, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see [Figure 18](#)). CL1 and CL2, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of CL1 and CL2.

Load capacitance CL has the following formula: $CL = CL1 \times CL2 / (CL1 + CL2) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: To avoid exceeding the maximum value of CL1 and CL2 (15 pF) it is strongly recommended to use a resonator with a load capacitance $CL \leq 7$ pF. Never use a resonator with a load capacitance of 12.5 pF.

Example: if you choose a resonator with a load capacitance of $CL = 6$ pF and $C_{stray} = 2$ pF, then $CL1 = CL2 = 8$ pF.

Figure 18. Typical application with a 32.768 kHz crystal

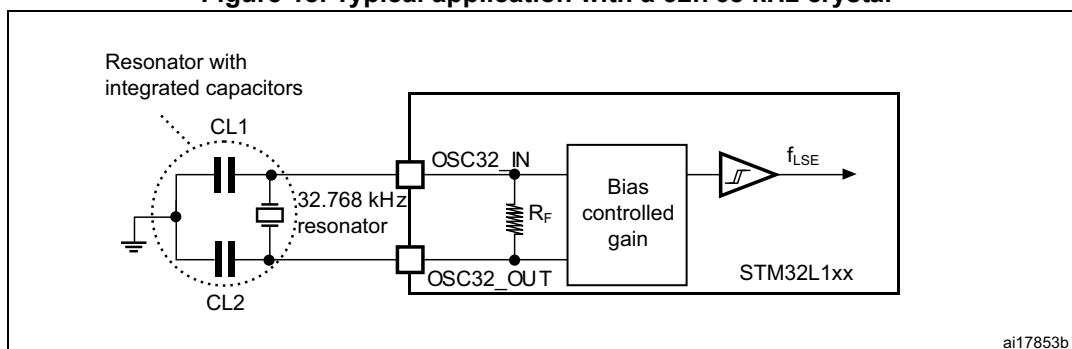
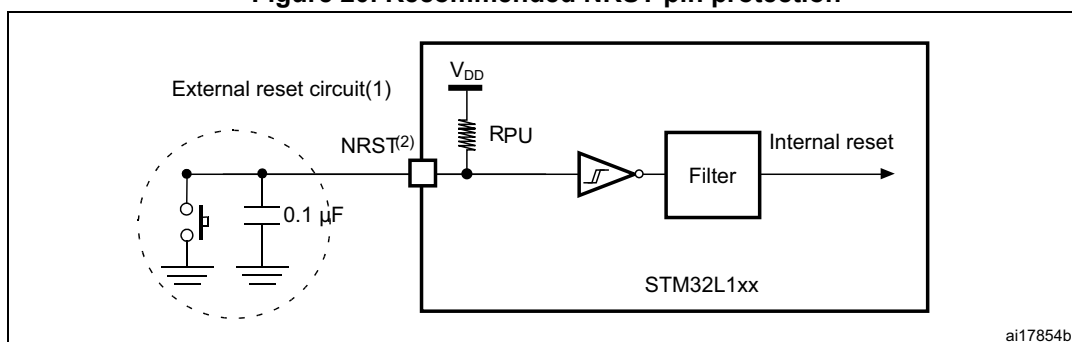


Figure 20. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in [Table 46](#). Otherwise the reset will not be taken into account by the device.

6.3.15 TIM timer characteristics

The parameters given in [Table 47](#) are guaranteed by design.

Refer to [Section 6.3.13: I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 47. TIMx⁽¹⁾ characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 32 \text{ MHz}$	31.25	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK} = 32 \text{ MHz}$	0	16	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected (timer's prescaler disabled)	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 32 \text{ MHz}$	0.0312	2048	μs
t_{MAX_COUNT}	Maximum possible count	-	-	65536×65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 32 \text{ MHz}$	-	134.2	s

1. TIMx is used as a general term to refer to the TIM2, TIM3 and TIM4 timers.

6.3.21 LCD controller (STM32L152x6/8/B-A devices only)

The STM32L152xx-A devices embed a built-in step-up converter to provide a constant LCD reference voltage independently from the V_{DD} voltage. An external capacitor C_{ext} must be connected to the V_{LCD} pin to decouple this converter.

Table 63. LCD controller characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{LCD}	LCD external voltage	-	-	3.6	V
V_{LCD0}	LCD internal reference voltage 0	-	2.6	-	
V_{LCD1}	LCD internal reference voltage 1	-	2.73	-	
V_{LCD2}	LCD internal reference voltage 2	-	2.86	-	
V_{LCD3}	LCD internal reference voltage 3	-	2.98	-	
V_{LCD4}	LCD internal reference voltage 4	-	3.12	-	
V_{LCD5}	LCD internal reference voltage 5	-	3.26	-	
V_{LCD6}	LCD internal reference voltage 6	-	3.4	-	
V_{LCD7}	LCD internal reference voltage 7	-	3.55	-	
C_{ext}	V_{LCD} external capacitance	0.1	-	2	μF
$I_{LCD}^{(1)}$	Supply current at $V_{DD} = 2.2 V$	-	3.3	-	μA
	Supply current at $V_{DD} = 3.0 V$	-	3.1	-	
$R_{Htot}^{(2)}$	Low drive resistive network overall value	5.28	6.6	7.92	$M\Omega$
$R_L^{(2)}$	High drive resistive network total value	192	240	288	$k\Omega$
V_{44}	Segment/Common highest level voltage	-	-	V_{LCD}	V
V_{34}	Segment/Common 3/4 level voltage	-	$3/4 V_{LCD}$	-	V
V_{23}	Segment/Common 2/3 level voltage	-	$2/3 V_{LCD}$	-	
V_{12}	Segment/Common 1/2 level voltage	-	$1/2 V_{LCD}$	-	
V_{13}	Segment/Common 1/3 level voltage	-	$1/3 V_{LCD}$	-	
V_{14}	Segment/Common 1/4 level voltage	-	$1/4 V_{LCD}$	-	
V_0	Segment/Common lowest level voltage	0	-	-	
$\Delta V_{xx}^{(2)}$	Segment/Common level voltage error $T_A = -40$ to $105^\circ C$	-	-	± 50	mV

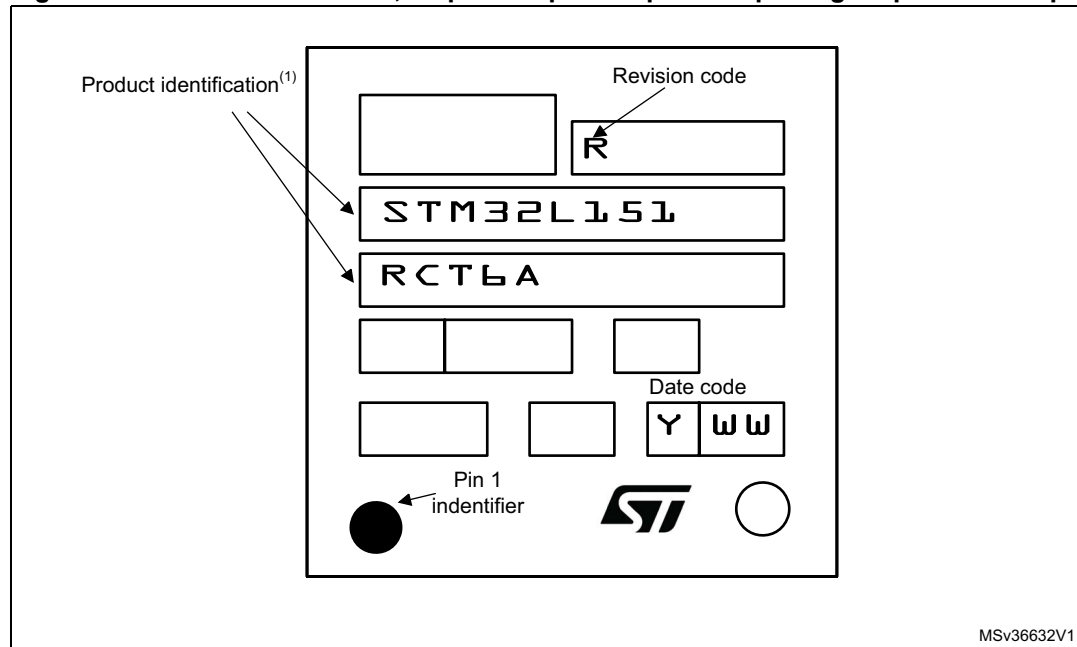
1. LCD enabled with 3 V internal step-up active, 1/8 duty, 1/4 bias, division ratio= 64, all pixels active, no LCD connected

2. Guaranteed by characterization results.

LQFP64 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

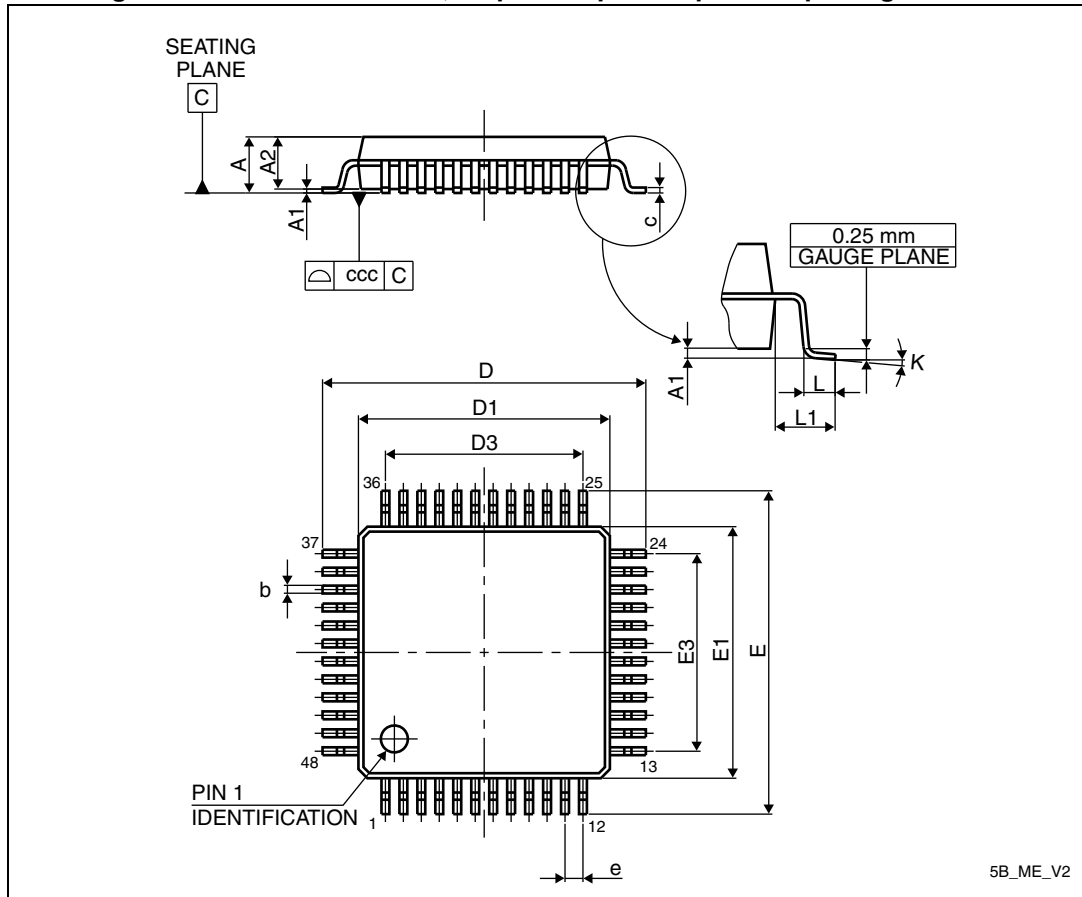
Figure 35. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package top view example



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.3 LQFP48 7 x 7 mm, 48-pin low-profile quad flat package information

Figure 36. LQFP48 7 x 7 mm, 48-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 66. LQFP48 7 x 7 mm, 48-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.