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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, Cap Sense, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 83 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 24x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151v8t6a |

## 2.1 Device overview

**Table 2. Ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A device features and peripheral counts**

| Peripheral | | STM32L15xCxxxA | | | STM32L15xRxxxA | | | STM32L15xVxxxA | |
|---|---|---|---|---|---|---|---|---|---|
| Flash (Kbytes) | | 32 | 64 | 128 | 32 | 64 | 128 | 64 | 128 |
| Data EEPROM (Kbytes) | | 4 | | | | | | | |
| RAM (Kbytes) | | 16 | 32 | 32 | 16 | 32 | 32 | 32 | 32 |
| Timers | General-purpose | 6 | | | | | | | |
| | Basic | 2 | | | | | | | |
| Communication interfaces | SPI | 2 | | | | | | | |
| | $I^2C$ | 2 | | | | | | | |
| | USART | 3 | | | | | | | |
| | USB | 1 | | | | | | | |
| GPIOs | | 37 | | | 51/50(1) | | | 83 | |
| 12-bit synchronized ADC Number of channels | | 1<br>14 channels | | | 1<br>20/19 channels(1) | | | 1<br>24 channels | |
| 12-bit DAC Number of channels | | 2<br>2 | | | | | | | |
| LCD (STM32L152xxxxA Only) COM x SEG | | 4x16 | | | 4x32/4x31(1)<br>8x28/8x27(1) | | | 4x44<br>8x40 | |
| Comparator | | 2 | | | | | | | |
| Capacitive sensing channels | | 13 | | | 20 | | | | |
| Max. CPU frequency | | 32 MHz | | | | | | | |
| Operating voltage | | 1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option<br>1.65 V to 3.6 V without BOR option | | | | | | | |
| Operating temperatures | | Ambient operating temperatures: –40 to +85 °C / –40 to + 105 °C<br>Junction temperature: -40 to +110°C | | | | | | | |
| Packages | | LQFP48, UFQFPN48 | | | LQFP64, TFBGA64 | | | LQFP100, UFBGA100 | |

1. For TFBGA64 package (instead of PC3 pin there is $V_{REF+}$ pin).

## 2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of cores and features. From a proprietary 8-bit core up to the Cortex-M3, including the Cortex-M0+, the STM8Lx and STM32Lx series offer the best range of choices to meet your requirements in terms of ultra-low-power features. The STM32 Ultra-low-power series is an ideal fit for applications like gas/water meters, keyboard/mouse, or wearable devices for fitness and healthcare. Numerous built-in features like LCD drivers, dual-bank memory, low-power Run mode, op-amp, AES-128bit, DAC, crystal-less USB and many others, allow to build highly cost-optimized applications by reducing the BOM.

*Note: STMicroelectronics as a reliable and long-term manufacturer ensures as much as possible the pin-to-pin compatibility between any STM8Lx and STM32Lx devices and between any of the STM32Lx and STM32Fx series. Thanks to this unprecedented scalability, your existing applications can be upgraded to respond to the latest market features and efficiency demand.*

### 2.2.1 Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM Cortex-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra-Low-power performance to range from 5 up to 33.3 DMIPs.

### 2.2.2 Shared peripherals

STM8L15xxx and STM32L1xxxx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC, DAC and comparators
- Digital peripherals: RTC and some communication interfaces

### 2.2.3 Common system strategy

To offer flexibility and optimize performance, the STM8L15xxx and STM32L1xxxx families use a common architecture:

- Common power supply range from 1.65 V to 3.6 V, (1.65 V at power down only for STM8L15xxx devices)
- Architecture optimized to reach ultra-low consumption both in low-power modes and Run mode
- Fast startup strategy from low-power modes
- Flexible system clock
- Ultra-safe reset: same reset strategy including power-on reset, power-down reset, brownout reset and programmable voltage detector.

### 2.2.4 Features

ST ultra-low-power continuum also lies in feature compatibility:

- More than 10 packages with pin count from 20 to 144 pins and size down to 3 x 3 mm
- Memory density ranging from 4 to 512 Kbytes

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage ($V_{REFINT}$) in Stop mode. The device remains in reset mode when $V_{DD}$ is below a specified threshold, $V_{POR/PDR}$ or $V_{BOR}$, without the need for any external reset circuit.

*Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.*

The device features an embedded programmable voltage detector (PVD) that monitors the $V_{DD}/V_{DDA}$ power supply and compares it to the $V_{PVD}$ threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when $V_{DD}/V_{DDA}$ drops below the $V_{PVD}$ threshold and/or when $V_{DD}/V_{DDA}$ is higher than the $V_{PVD}$ threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

### 3.3.3 Voltage regulator

The regulator has three operation modes: main (MR), low-power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32K osc, RCC_CSR).

### 3.3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from Flash memory
- Boot from System Memory
- Boot from embedded RAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1 or USART2. See the application note “STM32 microcontroller system memory boot mode” (AN2606) for details.

## 3.12 Ultra-low-power comparators and reference voltage

The STM32L151x6/8/B-A and STM32L152x6/8/B-A devices embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- one comparator with fixed threshold
- one comparator with rail-to-rail inputs, fast or slow mode. The threshold can be one of the following:
  - DAC output
  - External I/O
  - Internal reference voltage ($V_{REFINT}$) or $V_{REFINT}$ submultiple (1/4, 1/2, 3/4)

Both comparators can wake up from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 µA typical).

## 3.13 Routing interface

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM3 and TIM4 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1 and COMP2 and the internal reference voltage $V_{REFINT}$.

## 3.14 Touch sensing

The STM32L151x6/8/B-A and STM32L152x6/8/B-A devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 20 capacitive sensing channels distributed over 10 analog I/O groups. Both software and timer capacitive sensing acquisition modes are supported.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. The capacitive sensing acquisition only requires few external components to operate. This acquisition is managed directly by the GPIOs, timers and analog I/O groups (see *Section 3.13: Routing interface*).

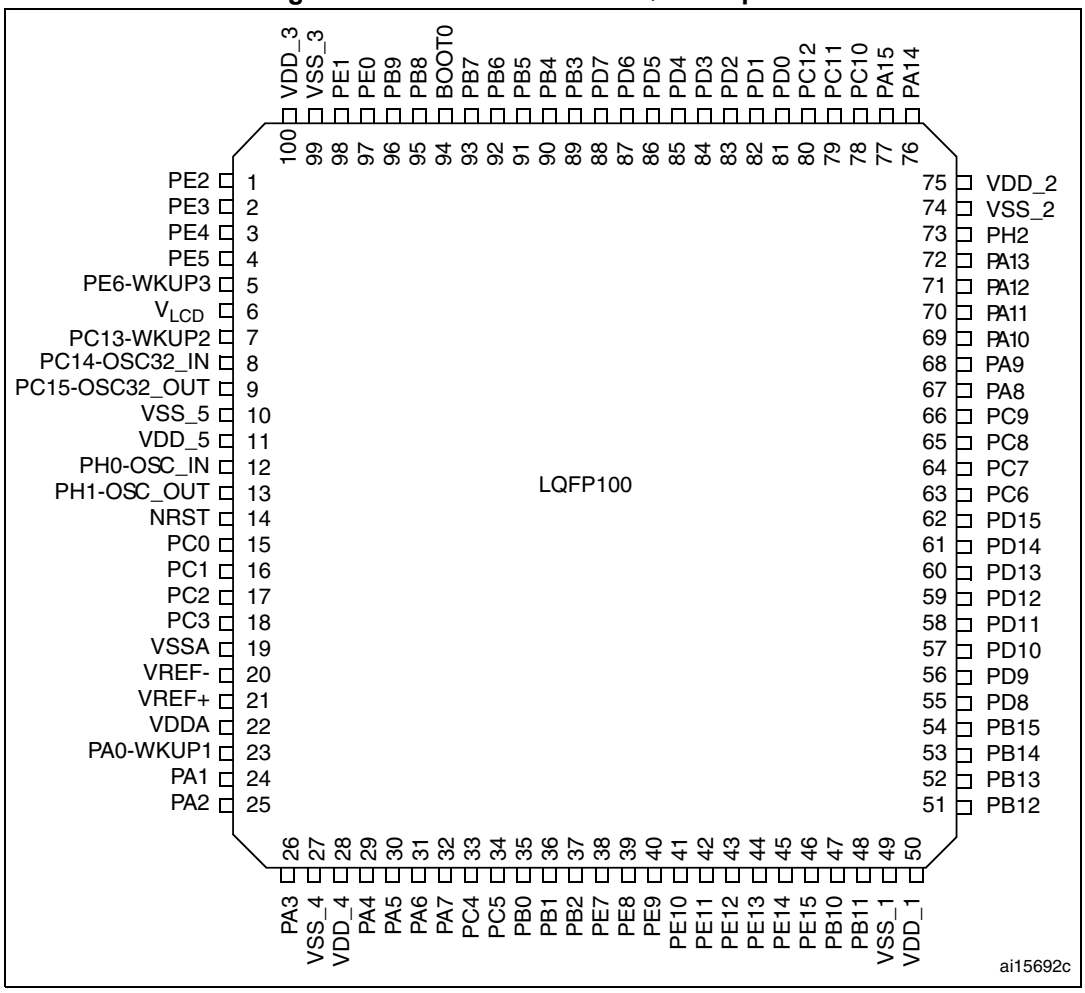
Reliable touch sensing functionality can be quickly and easily implemented using the free STM32L1xx STMTouch touch sensing firmware library.

## 3.15 Timers and watchdogs

The ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A devices include six general-purpose timers, two basic timers and two watchdog timers.

*Table 7* compares the features of the general-purpose and basic timers.

**Figure 4. STM32L15xVxxxA LQFP100 pinout**




1. This figure shows the package top view.

Table 9. STM32L151x6/8/B-A and STM32L152x6/8/B-A pin definitions (continued)

| Pins | | | | | Pin name | Pin type(1) | I/O structure | Main function(2) (after reset) | Pins functions | |
|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | LQFP64 | TFBGA64 | UFBGA100 | LQFP48 or UFQFPN48 | | | | | Alternate functions | Additional functions |
| 67 | 41 | D7 | D11 | 29 | PA8 | I/O | FT | PA8 | USART1_CK/MCO/ LCD_COM0 | - |
| 68 | 42 | C7 | D10 | 30 | PA9 | I/O | FT | PA9 | USART1_TX/ LCD_COM1 | - |
| 69 | 43 | C6 | C12 | 31 | PA10 | I/O | FT | PA10 | USART1_RX/ LCD_COM2 | - |
| 70 | 44 | C8 | B12 | 32 | PA11 | I/O | FT | PA11 | USART1_CTS/ SPI1_MISO | USB_DM |
| 71 | 45 | B8 | A12 | 33 | PA12 | I/O | FT | PA12 | USART1_RTS/ SPI1_MOSI | USB_DP |
| 72 | 46 | A8 | A11 | 34 | PA13 | I/O | FT | JTMS-SWDIO | JTMS-SWDIO | - |
| 73 | - | - | C11 | - | PH2 | I/O | FT | PH2 | - | - |
| 74 | 47 | D5 | F11 | 35 | $V_{SS\_2}$ | S | - | $V_{SS\_2}$ | - | - |
| 75 | 48 | E5 | G11 | 36 | $V_{DD\_2}$ | S | - | $V_{DD\_2}$ | - | - |
| 76 | 49 | A7 | A10 | 37 | PA14 | I/O | FT | JTCK-SWCLK | JCTK-SWCLK | - |
| 77 | 50 | A6 | A9 | 38 | PA15 | I/O | FT | JTDI | TIM2_CH1_ETR/PA15/ SPI1_NSS/ LCD_SEG17 | - |
| 78 | 51 | B7 | B11 | - | PC10 | I/O | FT | PC10 | USART3_TX/ LCD_SEG28/ LCD_SEG40/ LCD_COM4 | - |
| 79 | 52 | B6 | C10 | - | PC11 | I/O | FT | PC11 | USART3_RX/ LCD_SEG29/ LCD_SEG41/ LCD_COM5 | - |
| 80 | 53 | C5 | B10 | - | PC12 | I/O | FT | PC12 | USART3_CK/ LCD_SEG30/ LCD_SEG42/ LCD_COM6 | - |
| 81 | - | - | C9 | - | PD0 | I/O | FT | PD0 | SPI2_NSS/TIM9_CH1 | - |

**Table 9. STM32L151x6/8/B-A and STM32L152x6/8/B-A pin definitions (continued)**

| Pins | | | | | Pin name | Pin type[1] | I/O structure | Main function[2] (after reset) | Pins functions | |
|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | LQFP64 | TFBGA64 | UFBGA100 | LQFP48 or UFQFPN48 | | | | | Alternate functions | Additional functions |
| 98 | - | - | A2 | - | PE1 | I/O | FT | PE1 | LCD_SEG37/ TIM11_CH1 | - |
| 99 | 63 | D4 | D3 | 47 | $V_{SS\_3}$ | S | - | $V_{SS\_3}$ | - | - |
| 100 | 64 | E4 | C4 | 48 | $V_{DD\_3}$ | S | - | $V_{DD\_3}$ | - | - |

1. I = input, O = output, S = supply.
2. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripheral that is included. For example, if a device has only one SPI and two USARTs, they will be called SPI1 and USART1 & USART2, respectively. Refer to *Table 2 on page 11*.
3. Applicable to STM32L152xxxxA devices only. In STM32L151xxxxA devices, this pin should be connected to $V_{DD}$.
4. The PC14 and PC15 I/Os are only configured as OSC32_IN/OSC32_OUT when the LSE oscillator is on (by setting the LSEON bit in the RCC_CSR register). The LSE oscillator pins OSC32_IN/OSC32_OUT can be used as general-purpose PC14/PC15 I/Os, respectively, when the LSE oscillator is off (after reset, the LSE oscillator is off). The LSE has priority over the GPIO function. For more details, refer to Using the OSC32_IN/OSC32_OUT pins as GPIO PC14/PC15 port pins section in the STM32L1xxxx reference manual (RM0038).
5. The PH0 and PH1 I/Os are only configured as OSC_IN/OSC_OUT when the HSE oscillator is on (by setting the HSEON bit in the RCC_CR register). The HSE oscillator pins OSC_IN/OSC_OUT can be used as general-purpose PH0/PH1 I/Os, respectively, when the HSE oscillator is off (after reset, the HSE oscillator is off). The HSE has priority over the GPIO function.
6. Unlike in the LQFP64 package, there is no PC3 in the TFBGA64 package. The $V_{REF+}$ functionality is provided instead.

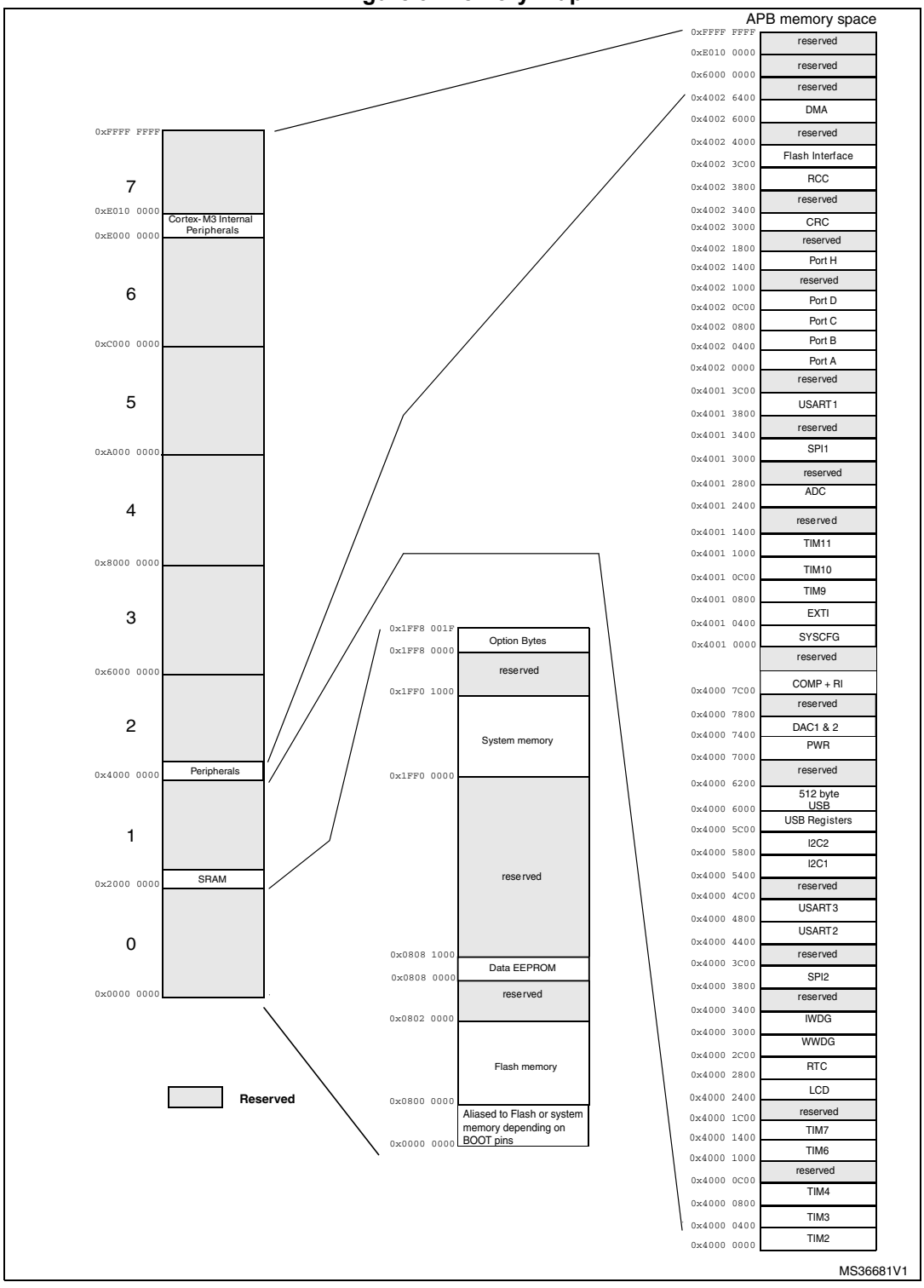
**Table 10. Alternate function input/output (continued)**

| Port name | Digital alternate function number | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | AFIO0 | AFIO1 | AFIO2 | AFIO3 | AFIO4 | AFIO5 | AFOI6 | AFIO7 | AFIO8 | AFIO9 | AFIO11 | AFIO12 | AFIO13 | AFIO14 | AFIO15 |
| | Alternate function | | | | | | | | | | | | | | |
| | SYSTEM | TIM2 | TIM3/4 | TIM9/10/11 | I2C1/2 | SPI1/2 | N/A | USART 1/2/3 | N/A | N/A | LCD | N/A | N/A | RI | SYSTEM |
| PC10 | - | - | - | - | - | - | - | USART3_TX | - | - | COM4 / SEG28 / SEG40 | - | - | TIMx_IC3 | EVENTOUT |
| PC11 | - | - | - | - | - | - | - | USART3_RX | - | - | COM5 / SEG29 / SEG41 | - | - | TIMx_IC4 | EVENTOUT |
| PC12 | - | - | - | - | - | - | - | USART3_CK | - | - | COM6 / SEG30 / SEG42 | - | - | TIMx_IC1 | EVENTOUT |
| PC13-WKUP2 | - | - | - | - | - | - | - | - | - | - | - | - | - | TIMx_IC2 | EVENTOUT |
| PC14-OSC32_IN | - | - | - | - | - | - | - | - | - | - | - | - | - | TIMx_IC3 | EVENTOUT |
| PC15-OSC32_OUT | - | - | - | - | - | - | - | - | - | - | - | - | - | TIMx_IC4 | EVENTOUT |
| PD0 | - | - | - | TIM9_CH1 | - | SPI2_NSS | - | - | - | - | - | - | - | TIMx_IC1 | EVENTOUT |
| PD1 | - | - | - | - | - | SPI2_SCK | - | - | - | - | - | - | - | TIMx_IC2 | EVENTOUT |
| PD2 | - | - | TIM3_ETR | - | - | - | - | - | - | - | COM7 / SEG31 / SEG43 | - | - | TIMx_IC3 | EVENTOUT |
| PD3 | - | - | - | - | - | SPI2_MISO | - | USART2_CTS | - | - | - | - | - | TIMx_IC4 | EVENTOUT |
| PD4 | - | - | - | - | - | SPI2_MOSI | - | USART2_RTS | - | - | - | - | - | TIMx_IC1 | EVENTOUT |
| PD5 | - | - | - | - | - | - | - | USART2_TX | - | - | - | - | - | TIMx_IC2 | EVENTOUT |
| PD6 | - | - | - | - | - | - | - | USART2_RX | - | - | - | - | - | TIMx_IC3 | EVENTOUT |
| PD7 | - | - | - | TIM9_CH2 | - | - | - | USART2_CK | - | - | - | - | - | TIMx_IC4 | EVENTOUT |
| PD8 | - | - | - | - | - | - | - | USART3_TX | - | - | - | - | - | TIMx_IC1 | EVENTOUT |
| PD9 | - | - | - | - | - | - | - | USART3_RX | - | - | - | - | - | TIMx_IC2 | EVENTOUT |

# 5 Memory mapping

The memory map is shown in the following figure.

**Figure 9. Memory map**



3. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.17*.
4. Positive current injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 11* for maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 11: Voltage characteristics* for the maximum allowed input voltage values.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

**Table 13. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $T_J$ | Maximum junction temperature | 150 | °C |
| $T_{LEAD}$ | Maximum lead temperature during soldering | see note (1) | °C |

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (ROHS directive 2011/65/EU, July 2011).

# 6.3 Operating conditions

## 6.3.1 General operating conditions

**Table 14. General operating conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{HCLK}$ | Internal AHB clock frequency | - | 0 | 32 | MHz |
| $f_{PCLK1}$ | Internal APB1 clock frequency | - | 0 | 32 | |
| $f_{PCLK2}$ | Internal APB2 clock frequency | - | 0 | 32 | |
| $V_{DD}$ | Standard operating voltage | BOR detector disabled | 1.65 | 3.6 | V |
| | | BOR detector enabled, at power on | 1.8 | 3.6 | |
| | | BOR detector disabled, after power on | 1.65 | 3.6 | |
| $V_{DDA}$ (1) | Analog operating voltage (ADC and DAC not used) | Must be the same voltage as $V_{DD}$ (2) | 1.65 | 3.6 | V |
| | Analog operating voltage (ADC or DAC used) | | 1.8 | 3.6 | |
| $V_{IN}$ | I/O input voltage | FT pins: 2.0 V ≤$V_{DD}$ | –0.3 | 5.5 (3) | V |
| | | FT pins: $V_{DD}$ < 2.0 V | –0.3 | 5.25 (3) | |
| | | BOOT0 | 0 | 5.5 | |
| | | Any other pin | –0.3 | $V_{DD}$+0.3 | |

**Table 14. General operating conditions (continued)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $P_D$ | Power dissipation at TA = 85 °C for suffix 6 or TA = 105 °C for suffix 7(4) | UFBGA100 package | - | 339 | mW |
| | | LQFP100 package | - | 435 | |
| | | TFBGA64 package | - | 308 | |
| | | LQFP64 package | - | 444 | |
| | | LQFP48 package | - | 364 | |
| | | UFQFPN48 package | - | 606 | |
| $T_A$ | Ambient temperature for 6 suffix version | Maximum power dissipation(5) | –40 | 85 | °C |
| | Ambient temperature for 7 suffix version | Maximum power dissipation | –40 | 105 | |
| $T_J$ | Junction temperature range | 6 suffix version | –40 | 105 | °C |
| | Junction temperature range | 7 suffix version | –40 | 110 | |

1. When the ADC is used, refer to *Table 55: ADC characteristics*.
2. It is recommended to power $V_{DD}$ and $V_{DDA}$ from the same source. A maximum difference of 300 mV between $V_{DD}$ and $V_{DDA}$ can be tolerated during power-up and operation.
3. To sustain a voltage higher than $V_{DD}$+0.3 V, the internal pull-up/pull-down resistors must be disabled.
4. If $T_A$ is lower, higher $P_D$ values are allowed as long as $T_J$ does not exceed $T_J$ max (see *Table 13: Thermal characteristics on page 56*).
5. In low-power dissipation state, $T_A$ can be extended to -40°C to 105°C temperature range as long as $T_J$ does not exceed $T_J$ max (see *Table 13: Thermal characteristics on page 56*).

### 6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the ambient temperature condition summarized in the following table.

**Table 15. Embedded reset and power control block characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{VDD}$(1) | $V_{DD}$ rise time rate | BOR detector enabled | 0 | - | ∞ | µs/V |
| | | BOR detector disabled | 0 | - | 1000 | |
| | $V_{DD}$ fall time rate | BOR detector enabled | 20 | - | ∞ | |
| | | BOR detector disabled | 0 | - | 1000 | |
| $T_{RSTTEMPO}$(1) | Reset temporization | $V_{DD}$ rising, BOR enabled | - | 2 | 3.3 | ms |
| | | $V_{DD}$ rising, BOR disabled(2) | 0.4 | 0.7 | 1.6 | |
| $V_{POR/PDR}$ | Power on/power down reset threshold | Falling edge | 1 | 1.5 | 1.65 | V |
| | | Rising edge | 1.3 | 1.5 | 1.65 | |

**Table 18. Current consumption in Run mode, code with data processing running from Flash**

| Symbol | Parameter | Conditions | | $f_{HCLK}$ | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ (Run from Flash) | Supply current in Run mode, code executed from Flash | $f_{HSE} = f_{HCLK}$ up to 16 MHz, included $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2) | Range 3, $V_{CORE}$=1.2 V VOS[1:0] = 11 | 1 MHz | 215 | 285 | µA |
| | | | | 2 MHz | 400 | 490 | |
| | | | | 4 MHz | 725 | 1000 | |
| | | | Range 2, $V_{CORE}$=1.5 V VOS[1:0] = 10 | 4 MHz | 0.915 | 1.3 | mA |
| | | | | 8 MHz | 1.75 | 2.15 | |
| | | | | 16 MHz | 3.4 | 4 | |
| | | | Range 1, $V_{CORE}$=1.8 V VOS[1:0] = 01 | 8 MHz | 2.1 | 2.9 | |
| | | | | 16 MHz | 4.2 | 5.2 | |
| | | | | 32 MHz | 8.25 | 9.6 | |
| | | HSI clock source (16 MHz) | Range 2, $V_{CORE}$=1.5 V VOS[1:0] = 10 | 16 MHz | 3.5 | 4.4 | |
| | | | Range 1, $V_{CORE}$=1.8 V VOS[1:0] = 01 | 32 MHz | 8.2 | 10.2 | |
| | | MSI clock, 65 kHz | Range 3, $V_{CORE}$=1.2 V VOS[1:0] = 11 | 65 kHz | 0.041 | 0.085 | |
| | | MSI clock, 524 kHz | | 524 kHz | 0.125 | 0.180 | |
| | | MSI clock, 4.2 MHz | | 4.2 MHz | 0.775 | 0.935 | |

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

**Table 20. Current consumption in Sleep mode**

| Symbol | Parameter | Conditions | | $f_{HCLK}$ | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ (Sleep) | Supply current in Sleep mode, Flash OFF | $f_{HSE}$ = $f_{HCLK}$ up to 16 MHz included, $f_{HSE}$ = $f_{HCLK}$/2 above 16 MHz (PLL ON)(2) | Range 3, $V_{CORE}$=1.2 V VOS[1:0] = 11 | 1 MHz | 50 | 155 | µA |
| | | | | 2 MHz | 78.5 | 235 | |
| | | | | 4 MHz | 140 | 370(3) | |
| | | | Range 2, $V_{CORE}$=1.5 V VOS[1:0] = 10 | 4 MHz | 165 | 375 | |
| | | | | 8 MHz | 310 | 530 | |
| | | | | 16 MHz | 590 | 1000 | |
| | | | Range 1, $V_{CORE}$=1.8 V VOS[1:0] = 01 | 8 MHz | 350 | 615 | |
| | | | | 16 MHz | 680 | 1200 | |
| | | | | 32 MHz | 1600 | 2350 | |
| | | HSI clock source (16 MHz) | Range 2, $V_{CORE}$=1.5 V VOS[1:0] = 10 | 16 MHz | 640 | 970 | |
| | | | Range 1, $V_{CORE}$=1.8 V VOS[1:0] = 01 | 32 MHz | 1600 | 2350 | |
| | | MSI clock, 65 kHz | Range 3, $V_{CORE}$=1.2 V VOS[1:0] = 11 | 65 kHz | 19 | 60 | |
| | | MSI clock, 524 kHz | | 524 kHz | 33 | 90 | |
| | | MSI clock, 4.2 MHz | | 4.2 MHz | 145 | 210 | |
| | Supply current in Sleep mode, Flash ON | $f_{HSE}$ = $f_{HCLK}$ up to 16 MHz included, $f_{HSE}$ = $f_{HCLK}$/2 above 16 MHz (PLL ON)(2) | Range 3, $V_{CORE}$=1.2 V VOS[1:0] = 11 | 1 MHz | 60.5 | 145 | µA |
| | | | | 2 MHz | 89.5 | 225 | |
| | | | | 4 MHz | 150 | 360 | |
| | | | Range 2, $V_{CORE}$=1.5 V VOS[1:0] = 10 | 4 MHz | 180 | 370 | |
| | | | | 8 MHz | 320 | 490 | |
| | | | | 16 MHz | 605 | 895 | |
| | | | Range 1, $V_{CORE}$=1.8 V VOS[1:0] = 01 | 8 MHz | 380 | 565 | |
| | | | | 16 MHz | 695 | 1070 | |
| | | | | 32 MHz | 1600 | 2200 | |
| | | HSI clock source (16 MHz) | Range 2, $V_{CORE}$=1.5 V VOS[1:0] = 10 | 16 MHz | 650 | 970 | |
| | | | Range 1, $V_{CORE}$=1.8 V VOS[1:0] = 01 | 32 MHz | 1600 | 2320 | |
| | | MSI clock, 65 kHz | Range 3, $V_{CORE}$=1.2V VOS[1:0] = 11 | 65 kHz | 29.5 | 65 | |
| | | MSI clock, 524 kHz | | 524 kHz | 44 | 80 | |
| | | MSI clock, 4.2 MHz | | 4.2 MHz | 155 | 220 | |

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register)
3. Guaranteed by test in production.

**Table 52. USB DC electrical characteristics**

| Symbol | Parameter | Conditions | Min.(1) | Max.(1) | Unit |
|---|---|---|---|---|---|
| **Input levels** | | | | | |
| $V_{DD}$ | USB operating voltage(2) | - | 3.0 | 3.6 | V |
| $V_{DI}$(3) | Differential input sensitivity | I(USB_DP, USB_DM) | 0.2 | - | V |
| $V_{CM}$(3) | Differential common mode range | Includes $V_{DI}$ range | 0.8 | 2.5 | |
| $V_{SE}$(3) | Single ended receiver threshold | - | 1.3 | 2.0 | |
| **Output levels** | | | | | |
| $V_{OL}$(4) | Static output level low | $R_L$ of 1.5 kΩ to 3.6 V(5) | - | 0.3 | V |
| $V_{OH}$(4) | Static output level high | $R_L$ of 15 kΩ to $V_{SS}$(5) | 2.8 | 3.6 | |

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. Guaranteed by characterization results.
4. Guaranteed by test in production.
5. $R_L$ is the load connected on the USB drivers.

**Figure 25. USB timings: definition of data signal rise and fall time**

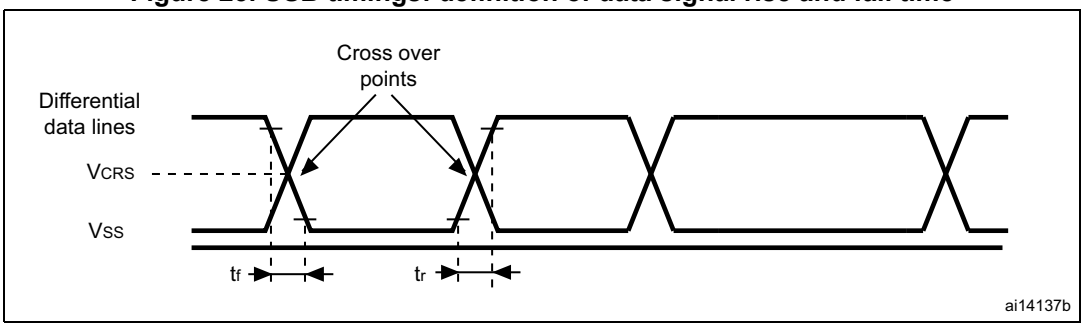



**Table 53. USB: full speed electrical characteristics**

| Driver characteristics(1) | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Unit** |
| $t_r$ | Rise time(2) | $C_L$ = 50 pF | 4 | 20 | ns |
| $t_f$ | Fall Time(2) | $C_L$ = 50 pF | 4 | 20 | ns |
| $t_{rfm}$ | Rise/ fall time matching | $t_r/t_f$ | 90 | 110 | % |
| $V_{CRS}$ | Output signal crossover voltage | - | 1.3 | 2.0 | V |

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification section 7 (version 2.0).

### 6.3.18 DAC electrical specifications

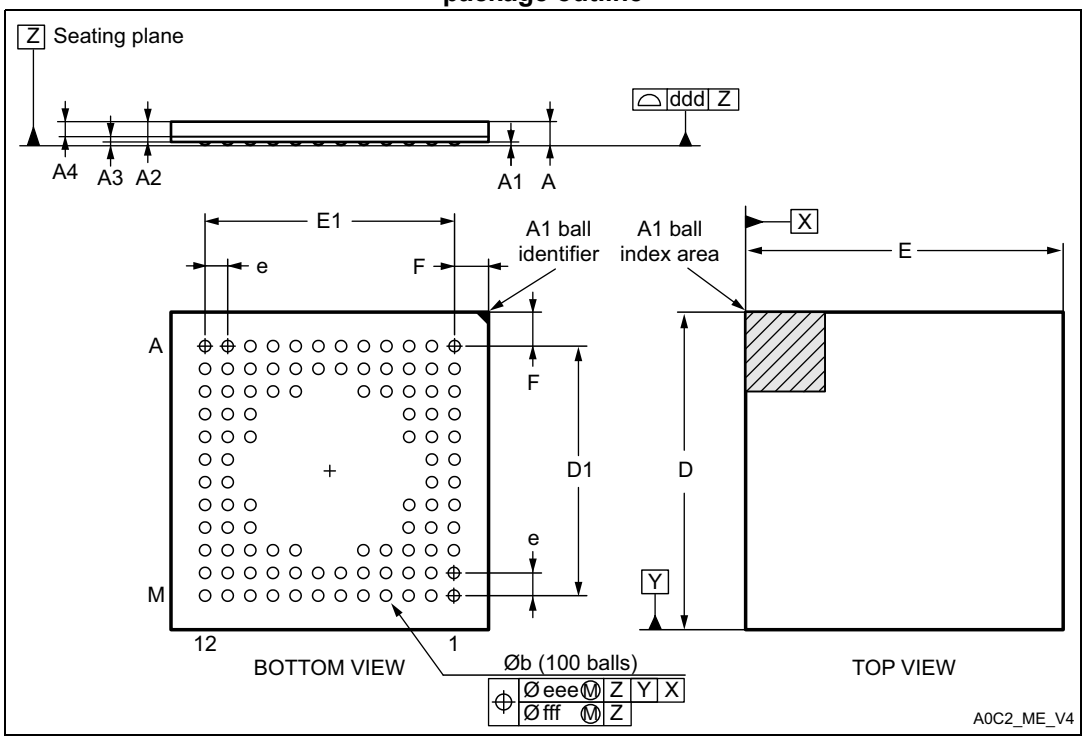
Data guaranteed by design, unless otherwise specified.

**Table 58. DAC characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | | 1.8 | - | 3.6 | V |
| $V_{REF+}$ | Reference supply voltage | $V_{REF+}$ must always be below $V_{DDA}$ | | 1.8 | - | 3.6 | V |
| $V_{REF-}$ | Lower reference voltage | - | | $V_{SSA}$ | | | V |
| $I_{DDVREF+}$(1) | Current consumption on $V_{REF+}$ supply $V_{REF+}$ = 3.3 V | No load, middle code (0x800) | | - | 130 | 220 | µA |
| | | No load, worst code (0x000) | | - | 220 | 350 | µA |
| $I_{DDA}$(1) | Current consumption on $V_{DDA}$ supply $V_{DDA}$ = 3.3 V | No load, middle code (0x800) | | - | 210 | 320 | µA |
| | | No load, worst code (0xF1C) | | - | 320 | 520 | µA |
| $R_L$ | Resistive load | DAC output buffer ON | Connected to $V_{SSA}$ | 5 | - | - | kΩ |
| | | | Connected to $V_{DDA}$ | 25 | - | - | |
| $C_L$ | Capacitive load | DAC output buffer ON | | - | - | 50 | pF |
| $R_O$ | Output impedance | DAC output buffer OFF | | 12 | 16 | 20 | kΩ |
| $V_{DAC\_OUT}$ | Voltage on DAC_OUT output | DAC output buffer ON | | 0.2 | - | $V_{DDA}$ – 0.2 | V |
| | | DAC output buffer OFF | | 0.5 | - | $V_{REF+}$– 1LSB | mV |
| DNL(1) | Differential non linearity(2) | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON | | - | 1.5 | 3 | LSB |
| | | No $R_L$, $C_L \leq 50$ pF DAC output buffer OFF | | - | 1.5 | 3 | |
| INL(1) | Integral non linearity(3) | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON | | - | 2 | 4 | |
| | | No $R_L$, $C_L \leq 50$ pF DAC output buffer OFF | | - | 2 | 4 | |
| Offset(1) | Offset error at code 0x800 (4) | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON | | - | ±10 | ±25 | |
| | | No $R_L$, $C_L \leq 50$ pF DAC output buffer OFF | | - | ±5 | ±8 | |
| Offset1(1) | Offset error at code 0x001(5) | No $R_L$, $C_L \leq 50$ pF DAC output buffer OFF | | - | ±1.5 | ±5 | |

## 7.5 UFBGA100 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package information

**Figure 42. UFBGA100, 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package outline**




1. Drawing is not to scale.

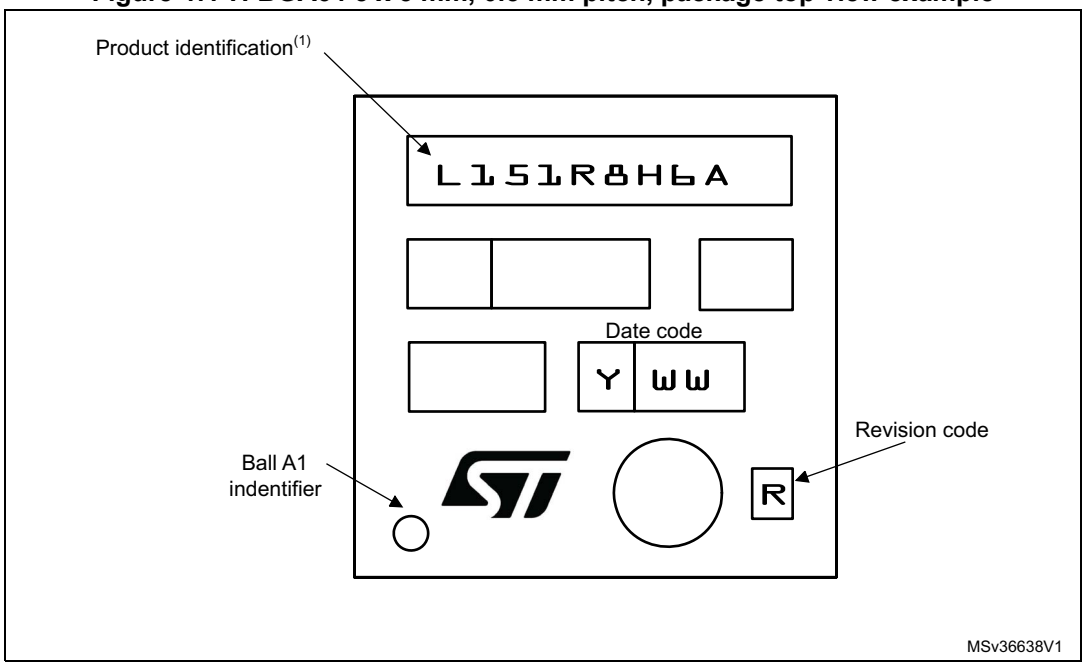
**Table 68. UFBGA100 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 0.6 | - | - | 0.0236 |
| A1 | 0.05 | 0.08 | 0.11 | 0.002 | 0.0031 | 0.0043 |
| A2 | 0.4 | 0.45 | 0.5 | 0.0157 | 0.0177 | 0.0197 |
| A3 | 0.08 | 0.13 | 0.18 | 0.0031 | 0.0051 | 0.0071 |
| A4 | 0.27 | 0.32 | 0.37 | 0.0106 | 0.0126 | 0.0146 |
| b | 0.2 | 0.25 | 0.3 | 0.0079 | 0.0098 | 0.0118 |
| D | 6.95 | 7 | 7.05 | 0.2736 | 0.2756 | 0.2776 |
| D1 | 5.45 | 5.5 | 5.55 | 0.2146 | 0.2165 | 0.2185 |
| E | 6.95 | 7 | 7.05 | 0.2736 | 0.2756 | 0.2776 |
| E1 | 5.45 | 5.5 | 5.55 | 0.2146 | 0.2165 | 0.2185 |
| e | - | 0.5 | - | - | 0.0197 | - |

### TFBGA64 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

**Figure 47. TFBGA64 5 x 5 mm, 0.5 mm pitch, package top view example**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

# 8 Ordering information

**Table 73. Ordering information scheme**

Example: STM32 L 152 R B T 6 A D TR

**Device family**

STM32 = ARM-based 32-bit microcontroller

**Product type**

L = Low-power

Device subfamily

151: Devices without LCD

152: Devices with LCD

Pin count

C = 48 pins

R = 64 pins

V = 100 pins

**Flash memory size**

6 = 32 Kbytes of Flash memory

8 = 64 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

**Package**

H = BGA

T = LQFP

U = UFQFPN

**Temperature range**

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

Options

A = device generation A

No character = VDD range: 1.8 to 3.6 V and BOR enabled

D = VDD range: 1.65 to 3.6 V and BOR disabled

Packing

TR = tape and reel

No character = tray or tube

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.