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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152cbt6a">https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152cbt6a</a>

## 2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of cores and features. From a proprietary 8-bit core up to the Cortex-M3, including the Cortex-M0+, the STM8Lx and STM32Lx series offer the best range of choices to meet your requirements in terms of ultra-low-power features. The STM32 Ultra-low-power series is an ideal fit for applications like gas/water meters, keyboard/mouse, or wearable devices for fitness and healthcare. Numerous built-in features like LCD drivers, dual-bank memory, low-power Run mode, op-amp, AES-128bit, DAC, crystal-less USB and many others, allow to build highly cost-optimized applications by reducing the BOM.

*Note: STMicroelectronics as a reliable and long-term manufacturer ensures as much as possible the pin-to-pin compatibility between any STM8Lx and STM32Lx devices and between any of the STM32Lx and STM32Fx series. Thanks to this unprecedented scalability, your existing applications can be upgraded to respond to the latest market features and efficiency demand.*

### 2.2.1 Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM Cortex-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra-Low-power performance to range from 5 up to 33.3 DMIPs.

### 2.2.2 Shared peripherals

STM8L15xxx and STM32L1xxxx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC, DAC and comparators
- Digital peripherals: RTC and some communication interfaces

### 2.2.3 Common system strategy

To offer flexibility and optimize performance, the STM8L15xxx and STM32L1xxxx families use a common architecture:

- Common power supply range from 1.65 V to 3.6 V, (1.65 V at power down only for STM8L15xxx devices)
- Architecture optimized to reach ultra-low consumption both in low-power modes and Run mode
- Fast startup strategy from low-power modes
- Flexible system clock
- Ultra-safe reset: same reset strategy including power-on reset, power-down reset, brownout reset and programmable voltage detector.

### 2.2.4 Features

ST ultra-low-power continuum also lies in feature compatibility:

- More than 10 packages with pin count from 20 to 144 pins and size down to 3 x 3 mm
- Memory density ranging from 4 to 512 Kbytes

### 3.1 Low-power modes

The ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A devices support dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply:

- In Range 1 ( $V_{DD}$  range limited to 1.71-3.6 V), the CPU runs at up to 32 MHz (refer to [Table 18](#) for consumption).
- In Range 2 (full  $V_{DD}$  range), the CPU runs at up to 16 MHz (refer to [Table 18](#) for consumption)
- In Range 3 (full  $V_{DD}$  range), the CPU runs at up to 4 MHz (generated only with the multispeed internal RC oscillator clock source). Refer to [Table 18](#) for consumption.

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep mode**  
In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.  
Sleep mode power consumption: refer to [Table 20](#).
- **Low-power Run mode**  
This mode is achieved with the multispeed internal (MSI) RC oscillator set to the minimum clock (less than 131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In the low-power Run mode, the clock frequency and the number of enabled peripherals are both limited.  
Low-power Run mode consumption: refer to [Table 21](#).
- **Low-power Sleep mode**  
This mode is achieved by entering the Sleep mode with the internal voltage regulator in low-power mode to minimize the regulator's operating current. In the low-power Sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.  
When wakeup is triggered by an event or an interrupt, the system reverts to the run mode with the regulator on.  
Low-power Sleep mode consumption: refer to [Table 22](#).
- **Stop mode with RTC**  
Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the  $V_{CORE}$  domain are stopped, the PLL, MSI RC, HSI RC and HSE crystal oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.  
The device can be woken up from Stop mode by any of the EXTI line, in 8  $\mu$ s. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on), it can be the RTC alarm(s), the USB wakeup, the RTC tamper events, the RTC timestamp event or the RTC wakeup.
- **Stop mode without RTC**  
Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, LSE and HSE crystal oscillators are disabled. The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 8  $\mu$ s. The EXTI

line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB wakeup.

Stop mode consumption: refer to [Table 23](#).

- **Standby mode with RTC**

Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire  $V_{\text{CORE}}$  domain is powered off. The PLL, MSI RC, HSI RC and HSE crystal oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC\_CSR).

The device exits Standby mode in 60  $\mu\text{s}$  when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby mode without RTC**

Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire  $V_{\text{CORE}}$  domain is powered off. The PLL, MSI, RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC\_CSR).

The device exits Standby mode in 60  $\mu\text{s}$  when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Standby mode consumption: refer to [Table 24](#).

*Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering the Stop or Standby mode.*

**Table 3. Functionalities depending on the operating power supply range**

Operating power supply range	Functionalities depending on the operating power supply range			
	DAC and ADC operation	USB	Dynamic voltage scaling range	I/O operation
$V_{\text{DD}} = 1.65$ to $1.71$ V	Not functional	Not functional	Range 2 or Range 3	Degraded speed performance
$V_{\text{DD}} = 1.71$ to $1.8$ V <sup>(1)</sup>	Not functional	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance
$V_{\text{DD}} = 1.8$ to $2.0$ V <sup>(1)</sup>	Conversion time up to 500 Ksps	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance

### 3.15.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit down-counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

## 3.16 Communication interfaces

### 3.16.1 I<sup>2</sup>C bus

Up to two I<sup>2</sup>C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7- and 10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

### 3.16.2 Universal synchronous/asynchronous receiver transmitter (USART)

All USART interfaces are able to communicate at speeds of up to 4 Mbit/s. They provide hardware management of the CTS and RTS signals and are ISO 7816 compliant. They support IrDA SIR ENDEC and have LIN Master/Slave capability.

All USART interfaces can be served by the DMA controller.

### 3.16.3 Serial peripheral interface (SPI)

Up to two SPIs are able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

Both SPIs can be served by the DMA controller.

### 3.16.4 Universal serial bus (USB)

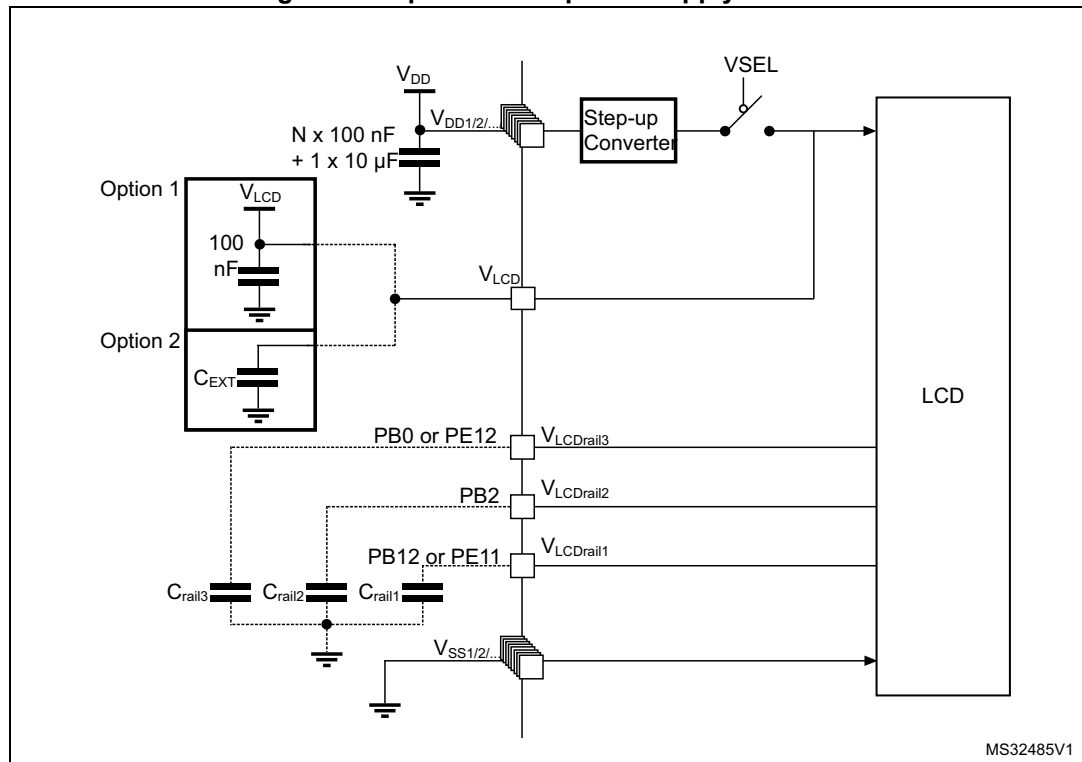
The STM32L151x6/8/B-A and STM32L152x6/8/B-A devices embed a USB device peripheral compatible with the USB full speed 12 Mbit/s. The USB interface implements a full speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and supports suspend/resume. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

Table 9. STM32L151x6/8/B-A and STM32L152x6/8/B-A pin definitions (continued)

Pins					Pin name	Pin type <sup>(1)</sup>	I/O structure	Main function <sup>(2)</sup> (after reset)	Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UQFPN48					Alternate functions	Additional functions
67	41	D7	D11	29	PA8	I/O	FT	PA8	USART1_CK/MCO/ LCD_COM0	-
68	42	C7	D10	30	PA9	I/O	FT	PA9	USART1_TX/ LCD_COM1	-
69	43	C6	C12	31	PA10	I/O	FT	PA10	USART1_RX/ LCD_COM2	-
70	44	C8	B12	32	PA11	I/O	FT	PA11	USART1_CTS/ SPI1_MISO	USB_DM
71	45	B8	A12	33	PA12	I/O	FT	PA12	USART1_RTS/ SPI1_MOSI	USB_DP
72	46	A8	A11	34	PA13	I/O	FT	JTMS-SWDIO	JTMS-SWDIO	-
73	-	-	C11	-	PH2	I/O	FT	PH2	-	-
74	47	D5	F11	35	V <sub>SS_2</sub>	S	-	V <sub>SS_2</sub>	-	-
75	48	E5	G11	36	V <sub>DD_2</sub>	S	-	V <sub>DD_2</sub>	-	-
76	49	A7	A10	37	PA14	I/O	FT	JTCK-SWCLK	JCTK-SWCLK	-
77	50	A6	A9	38	PA15	I/O	FT	JTDI	TIM2_CH1_ETR/PA15/ SPI1_NSS/ LCD_SEG17	-
78	51	B7	B11	-	PC10	I/O	FT	PC10	USART3_TX/ LCD_SEG28/ LCD_SEG40/ LCD_COM4	-
79	52	B6	C10	-	PC11	I/O	FT	PC11	USART3_RX/ LCD_SEG29/ LCD_SEG41/ LCD_COM5	-
80	53	C5	B10	-	PC12	I/O	FT	PC12	USART3_CK/ LCD_SEG30/ LCD_SEG42/ LCD_COM6	-
81	-	-	C9	-	PD0	I/O	FT	PD0	SPI2_NSS/TIM9_CH1	-

### 6.1.7 Optional LCD power supply scheme

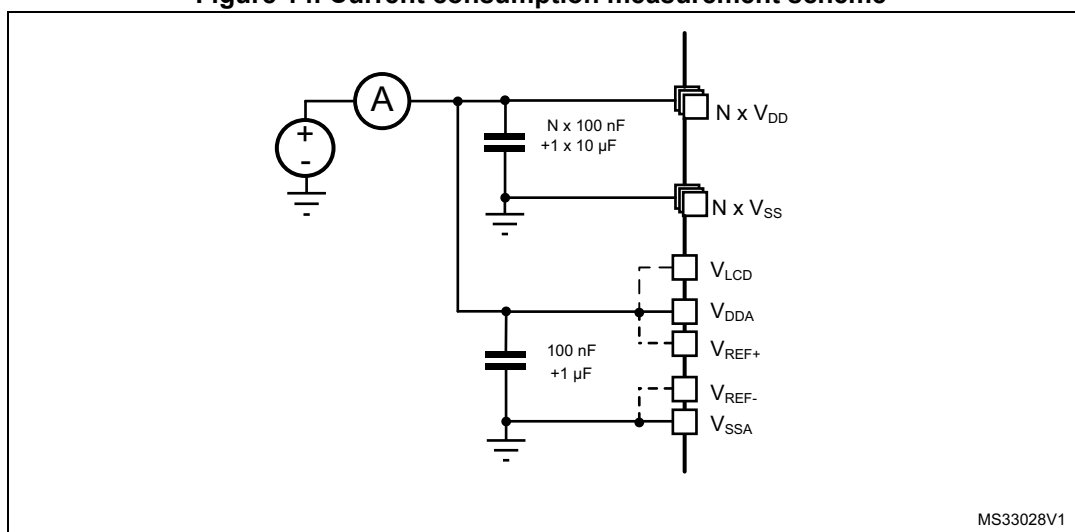
Figure 13. Optional LCD power supply scheme



1. Option 1: LCD power supply is provided by a dedicated V<sub>LCD</sub> supply source, V<sub>SEL</sub> switch is open.
2. Option 2: LCD power supply is provided by the internal step-up converter, V<sub>SEL</sub> switch is closed, an external capacitance is needed for correct behavior of this converter.

### 6.1.8 Current consumption measurement

Figure 14. Current consumption measurement scheme



## 6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 11: Voltage characteristics](#), [Table 12: Current characteristics](#), and [Table 13: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 11. Voltage characteristics**

Symbol	Ratings	Min	Max	Unit
$V_{DD}-V_{SS}$	External main supply voltage (including $V_{DDA}$ and $V_{DD}$ ) <sup>(1)</sup>	-0.3	4.0	V
$V_{IN}$ <sup>(2)</sup>	Input voltage on five-volt tolerant pin	$V_{SS}-0.3$	$V_{DD}+4.0$	
	Input voltage on any other pin	$V_{SS}-0.3$	4.0	
$ \Delta V_{DDX} $	Variations between different $V_{DD}$ power pins	-	50	mV
$ V_{SSX}-V_{SS} $	Variations between all different ground pins <sup>(3)</sup>	-	50	
$V_{REF+}-V_{DDA}$	Allowed voltage difference for $V_{REF+} > V_{DDA}$	-	0.4	V
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see <a href="#">Section 6.3.11</a>		-

1. All main power ( $V_{DD}$ ,  $V_{DDA}$ ) and ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the external power supply, in the permitted range.
2.  $V_{IN}$  maximum must always be respected. Refer to [Table 12](#) for maximum allowed injected current values.
3. Include  $V_{REF-}$  pin.

**Table 12. Current characteristics**

Symbol	Ratings	Max.	Unit
$\Sigma I_{VDD}$	Total current into sum of all $V_{DD\_x}$ power lines (source) <sup>(1)</sup>	100	mA
$\Sigma I_{VSS}$ <sup>(2)</sup>	Total current out of sum of all $V_{SS\_x}$ ground lines (sink) <sup>(1)</sup>	100	
$I_{VDD(PIN)}$	Maximum current into each $V_{DD\_x}$ power pin (source) <sup>(1)</sup>	70	
$I_{VSS(PIN)}$	Maximum current out of each $V_{SS\_x}$ ground pin (sink) <sup>(1)</sup>	-70	
$I_{IO}$	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	- 25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins <sup>(2)</sup>	60	
	Total output current sourced by sum of all IOs and control pins <sup>(2)</sup>	-60	
$I_{INJ(PIN)}$ <sup>(3)</sup>	Injected current on five-volt tolerant I/O <sup>(4)</sup> RST and B pins	-5/+0	
	Injected current on any other pin <sup>(5)</sup>	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) <sup>(6)</sup>	± 25	

1. All main power ( $V_{DD}$ ,  $V_{DDA}$ ) and ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.



Table 15. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{BOR0}$	Brown-out reset threshold 0	Falling edge	1.67	1.7	1.74	V
		Rising edge	1.69	1.76	1.8	
$V_{BOR1}$	Brown-out reset threshold 1	Falling edge	1.87	1.93	1.97	
		Rising edge	1.96	2.03	2.07	
$V_{BOR2}$	Brown-out reset threshold 2	Falling edge	2.22	2.30	2.35	
		Rising edge	2.31	2.41	2.44	
$V_{BOR3}$	Brown-out reset threshold 3	Falling edge	2.45	2.55	2.60	
		Rising edge	2.54	2.66	2.7	
$V_{BOR4}$	Brown-out reset threshold 4	Falling edge	2.68	2.8	2.85	
		Rising edge	2.78	2.9	2.95	
$V_{PVD0}$	Programmable voltage detector threshold 0	Falling edge	1.8	1.85	1.88	V
		Rising edge	1.88	1.94	1.99	
$V_{PVD1}$	PVD threshold 1	Falling edge	1.98	2.04	2.09	
		Rising edge	2.08	2.14	2.18	
$V_{PVD2}$	PVD threshold 2	Falling edge	2.20	2.24	2.28	
		Rising edge	2.28	2.34	2.38	
$V_{PVD3}$	PVD threshold 3	Falling edge	2.39	2.44	2.48	
		Rising edge	2.47	2.54	2.58	
$V_{PVD4}$	PVD threshold 4	Falling edge	2.57	2.64	2.69	
		Rising edge	2.68	2.74	2.79	
$V_{PVD5}$	PVD threshold 5	Falling edge	2.77	2.83	2.88	
		Rising edge	2.87	2.94	2.99	
$V_{PVD6}$	PVD threshold 6	Falling edge	2.97	3.05	3.09	
		Rising edge	3.08	3.15	3.20	
$V_{hyst}$	Hysteresis voltage	BOR0 threshold	-	40	-	mV
		All BOR and PVD thresholds excepting BOR0	-	100	-	

1. Guaranteed by characterization.

2. Valid for device version without BOR at power up. Please see option "D" in Ordering information scheme for more details.

Table 23. Typical and maximum current consumptions in Stop mode (continued)

Symbol	Parameter	Conditions	Typ <sup>(1)</sup>	Max <sup>(1)(2)</sup>	Unit
$I_{DD (Stop)}$	Supply current in Stop mode (RTC disabled)	Regulator in LP mode, HSI and HSE OFF, independent watchdog and LSI enabled	$T_A = -40^{\circ}\text{C to } 25^{\circ}\text{C}$	1.80	2.2
		Regulator in LP mode, LSI, HSI and HSE OFF (no independent watchdog)	$T_A = -40^{\circ}\text{C to } 25^{\circ}\text{C}$	0.434	1
			$T_A = 55^{\circ}\text{C}$	0.735	3
			$T_A = 85^{\circ}\text{C}$	2.350	9
			$T_A = 105^{\circ}\text{C}$	6.84	22 <sup>(6)</sup>
$I_{DD (WU \text{ from Stop})}$	RMS (root mean square) supply current during wakeup time when exiting from Stop mode	MSI = 4.2 MHz	$V_{DD} = 3.0 \text{ V}$ $T_A = -40^{\circ}\text{C to } 25^{\circ}\text{C}$	2	-
		MSI = 1.05 MHz		1.45	-
		MSI = 65 kHz <sup>(7)</sup>		1.45	-

1. The typical values are given for  $V_{DD} = 3.0 \text{ V}$  and max values are given for  $V_{DD} = 3.6 \text{ V}$ , unless otherwise specified.
2. Guaranteed by characterization results, unless otherwise specified.
3. LCD enabled with external VLCD, static duty, division ratio = 256, all pixels active, no LCD connected.
4. LCD enabled with external VLCD, 1/8 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
5. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8pF loading capacitors.
6. Guaranteed by test in production.
7. When MSI = 64 kHz, the RMS current is measured over the first 15  $\mu\text{s}$  following the wakeup event. For the remaining time of the wakeup period, the current is similar to the Run mode current.

Table 25. Peripheral current consumption<sup>(1)</sup> (continued)

Peripheral		Typical consumption, V <sub>DD</sub> = 3.0 V, T <sub>A</sub> = 25 °C				Unit
		Range 1, V <sub>CORE</sub> = 1.8 V VOS[1:0] = 01	Range 2, V <sub>CORE</sub> = 1.5 V VOS[1:0] = 10	Range 3, V <sub>CORE</sub> = 1.2 V VOS[1:0] = 11	Low-power sleep and run	
I <sub>DD</sub> (RTC)		0.4				μA
I <sub>DD</sub> (LCD)		3.1				
I <sub>DD</sub> (ADC) <sup>(4)</sup>		1450				
I <sub>DD</sub> (DAC) <sup>(5)</sup>		340				
I <sub>DD</sub> (COMP1)		0.16				
I <sub>DD</sub> (COMP2)	Slow mode	2				
	Fast mode	5				
I <sub>DD</sub> (PVD / BOR) <sup>(6)</sup>		2.6				
I <sub>DD</sub> (IWDG)		0.25				

1. Data based on differential I<sub>DD</sub> measurement between all peripherals OFF and one peripheral with clock enabled, in the following conditions: f<sub>HCLK</sub> = 32 MHz (Range 1), f<sub>HCLK</sub> = 16 MHz (Range 2), f<sub>HCLK</sub> = 4 MHz (Range 3), f<sub>HCLK</sub> = 64kHz (Low-power run/sleep), f<sub>APB1</sub> = f<sub>HCLK</sub>, f<sub>APB2</sub> = f<sub>HCLK</sub>, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling.
2. HSI oscillator is OFF for this measure.
3. In low-power sleep and run mode, the Flash memory must always be in power-down mode.
4. Data based on a differential I<sub>DD</sub> measurement between ADC in reset configuration and continuous ADC conversion (HSI consumption not included).
5. Data based on a differential I<sub>DD</sub> measurement between DAC in reset configuration and continuous DAC conversion of V<sub>DD</sub>/2. DAC is in buffered mode, output is left floating.
6. Including supply current of internal reference voltage.

### 6.3.5 Wakeup time from Low-power mode

The wakeup times given in the following table are measured with the MSI RC oscillator. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: the clock source is the clock that was set before entering Sleep mode
- Stop mode: the clock source is the MSI oscillator in the range configured before entering Stop mode
- Standby mode: the clock source is the MSI oscillator running at 2.1 MHz

All timings are derived from tests performed under ambient temperature and V<sub>DD</sub> supply voltage conditions summarized in [Table 14](#).

Table 26. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ	Max <sup>(1)</sup>	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	$f_{HCLK} = 32 \text{ MHz}$	0.4	-	$\mu\text{s}$
$t_{WUSLEEP\_LP}$	Wakeup from Low-power sleep mode $f_{HCLK} = 262 \text{ kHz}$	$f_{HCLK} = 262 \text{ kHz}$ Flash enabled	46	-	
		$f_{HCLK} = 262 \text{ kHz}$ Flash switched OFF	46	-	
$t_{WUSTOP}$	Wakeup from Stop mode, regulator in Run mode	$f_{HCLK} = f_{MSI} = 4.2 \text{ MHz}$	8.2	-	
		$f_{HCLK} = f_{MSI} = 4.2 \text{ MHz}$ Voltage Range 1 and 2	7.7	8.9	
	Wakeup from Stop mode, regulator in low-power mode	$f_{HCLK} = f_{MSI} = 4.2 \text{ MHz}$ Voltage Range 3	8.2	13.1	
		$f_{HCLK} = f_{MSI} = 2.1 \text{ MHz}$	10.2	13.4	
		$f_{HCLK} = f_{MSI} = 1.05 \text{ MHz}$	16	20	
		$f_{HCLK} = f_{MSI} = 524 \text{ kHz}$	31	37	
		$f_{HCLK} = f_{MSI} = 262 \text{ kHz}$	57	66	
		$f_{HCLK} = f_{MSI} = 131 \text{ kHz}$	112	123	
		$f_{HCLK} = f_{MSI} = 65 \text{ kHz}$	221	236	
$t_{WUSTDBY}$	Wakeup from Standby mode FWU bit = 1	$f_{HCLK} = f_{MSI} = 2.1 \text{ MHz}$	58	104	ms
	Wakeup from Standby mode FWU bit = 0	$f_{HCLK} = f_{MSI} = 2.1 \text{ MHz}$	2.6	3.25	

1. Guaranteed by characterization results, unless otherwise specified

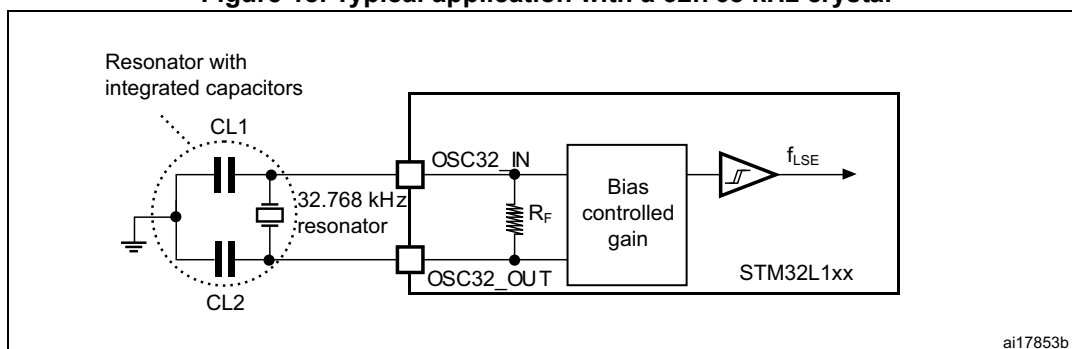
**Note:** For CL1 and CL2, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see [Figure 18](#)). CL1 and CL2, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of CL1 and CL2.

Load capacitance CL has the following formula:  $CL = CL1 \times CL2 / (CL1 + CL2) + C_{stray}$  where  $C_{stray}$  is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

**Caution:** To avoid exceeding the maximum value of CL1 and CL2 (15 pF) it is strongly recommended to use a resonator with a load capacitance  $CL \leq 7$  pF. Never use a resonator with a load capacitance of 12.5 pF.

Example: if you choose a resonator with a load capacitance of  $CL = 6$  pF and  $C_{stray} = 2$  pF, then  $CL1 = CL2 = 8$  pF.

**Figure 18. Typical application with a 32.768 kHz crystal**



### 6.3.7 Internal clock source characteristics

The parameters given in the following table are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 14](#).

#### High-speed internal (HSI) RC oscillator

**Table 31. HSI oscillator characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{HSI}$	Frequency	$V_{DD} = 3.0\text{ V}$	-	16	-	MHz
$TRIM^{(1)(2)}$	HSI user-trimmed resolution	Trimming code is not a multiple of 16	-	$\pm 0.4$	0.7	%
		Trimming code is a multiple of 16	-	-	$\pm 1.5$	%
$ACC_{HSI}^{(2)}$	Accuracy of the factory-calibrated HSI oscillator	$V_{DDA} = 3.0\text{ V}$ , $T_A = 25\text{ }^\circ\text{C}$	-1 <sup>(3)</sup>	-	1 <sup>(3)</sup>	%
		$V_{DDA} = 3.0\text{ V}$ , $T_A = 0\text{ to }55\text{ }^\circ\text{C}$	-1.5	-	1.5	%
		$V_{DDA} = 3.0\text{ V}$ , $T_A = -10\text{ to }70\text{ }^\circ\text{C}$	-2	-	2	%
		$V_{DDA} = 3.0\text{ V}$ , $T_A = -10\text{ to }85\text{ }^\circ\text{C}$	-2.5	-	2	%
		$V_{DDA} = 3.0\text{ V}$ , $T_A = -10\text{ to }105\text{ }^\circ\text{C}$	-4	-	2	%
		$V_{DDA} = 1.65\text{ V to }3.6\text{ V}$ $T_A = -40\text{ to }105\text{ }^\circ\text{C}$	-4	-	3	%
$t_{SU(HSI)}^{(2)}$	HSI oscillator startup time	-	-	3.7	6	$\mu\text{s}$
$I_{DD(HSI)}^{(2)}$	HSI oscillator power consumption	-	-	100	140	$\mu\text{A}$

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).
2. Guaranteed by characterization results.
3. Guaranteed by test in production.

#### Low-speed internal (LSI) RC oscillator

**Table 32. LSI oscillator characteristics**

Symbol	Parameter	Min	Typ	Max	Unit
$f_{LSI}^{(1)}$	LSI frequency	26	38	56	kHz
$D_{LSI}^{(2)}$	LSI oscillator frequency drift $0^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	-10	-	4	%
$t_{SU(LSI)}^{(3)}$	LSI oscillator startup time	-	-	200	$\mu\text{s}$
$I_{DD(LSI)}^{(3)}$	LSI oscillator power consumption	-	400	510	nA

1. Guaranteed by test in production.
2. This is a deviation for an individual part, once the initial frequency has been measured.
3. Guaranteed by design.

### 6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during the device characterization.

#### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB: A Burst of Fast Transient voltage** (positive and negative) is applied to  $V_{DD}$  and  $V_{SS}$  through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 38](#). They are based on the EMS levels and classes defined in application note AN1709.

**Table 38. EMS characteristics**

Symbol	Parameter	Conditions	Level/Class
$V_{FESD}$	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$ , LQFP100, $T_A = +25\text{ }^{\circ}\text{C}$ , $f_{HCLK} = 32\text{ MHz}$ conforms to IEC 61000-4-2	3B
$V_{EFTB}$	Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$ , LQFP100, $T_A = +25\text{ }^{\circ}\text{C}$ , $f_{HCLK} = 32\text{ MHz}$ conforms to IEC 61000-4-4	4A

#### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

##### Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

##### Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

### 6.3.13 I/O port characteristics

#### General input/output characteristics

Unless otherwise specified, the parameters given in [Table 43](#) are derived from tests performed under conditions summarized in [Table 14](#). All I/Os are CMOS and TTL compliant.

**Table 43. I/O static characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL}$	Input low level voltage	TC and FT I/O	-	-	$0.3 V_{DD}^{(1)(2)}$	V
		BOOT0	-	-	$0.14 V_{DD}^{(2)}$	
$V_{IH}$	Input high level voltage	TC I/O	$0.45 V_{DD} + 0.38^{(2)}$	-	-	
		FT I/O	$0.39 V_{DD} + 0.59^{(2)}$	-	-	
		BOOT0	$0.15 V_{DD} + 0.56^{(2)}$	-	-	
$V_{hys}$	I/O Schmitt trigger voltage hysteresis <sup>(2)</sup>	TC and FT I/O	-	$10\% V_{DD}^{(3)}$	-	nA
		BOOT0	-	0.01	-	
$I_{lkg}$	Input leakage current <sup>(4)</sup>	$V_{SS} \leq V_{IN} \leq V_{DD}$ I/Os with LCD	-	-	$\pm 50$	
		$V_{SS} \leq V_{IN} \leq V_{DD}$ I/Os with analog switches	-	-	$\pm 50$	
		$V_{SS} \leq V_{IN} \leq V_{DD}$ I/Os with analog switches and LCD	-	-	$\pm 50$	
		$V_{SS} \leq V_{IN} \leq V_{DD}$ I/Os with USB	-	-	$\pm 250$	
		$V_{SS} \leq V_{IN} \leq V_{DD}$ TC and FT I/O	-	-	$\pm 50$	
		FT I/O $V_{DD} \leq V_{IN} \leq 5V$	-	-	$\pm 10$	uA
$R_{PU}$	Weak pull-up equivalent resistor <sup>(5)(1)</sup>	$V_{IN} = V_{SS}$	30	45	60	k $\Omega$
$R_{PD}$	Weak pull-down equivalent resistor <sup>(5)</sup>	$V_{IN} = V_{DD}$	30	45	60	k $\Omega$
$C_{IO}$	I/O pin capacitance	-	-	5	-	pF

1. Guaranteed by test in production.

2. Guaranteed by design.

3. With a minimum of 200 mV.

4. The max. value may be exceeded if negative current is injected on adjacent pins.

5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).



### Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 19](#) and [Table 45](#), respectively.

Unless otherwise specified, the parameters given in [Table 45](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 14](#).

**Table 45. I/O AC characteristics<sup>(1)</sup>**

OSPEEDRx [1:0] bit value <sup>(1)</sup>	Symbol	Parameter	Conditions	Min	Max <sup>(2)</sup>	Unit
00	$f_{\max(\text{IO})\text{out}}$	Maximum frequency <sup>(3)</sup>	$C_L = 50 \text{ pF}$ , $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	400	kHz
			$C_L = 50 \text{ pF}$ , $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	400	
	$t_{f(\text{IO})\text{out}}$ $t_{r(\text{IO})\text{out}}$	Output rise and fall time	$C_L = 50 \text{ pF}$ , $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	625	ns
			$C_L = 50 \text{ pF}$ , $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	625	
01	$f_{\max(\text{IO})\text{out}}$	Maximum frequency <sup>(3)</sup>	$C_L = 50 \text{ pF}$ , $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	2	MHz
			$C_L = 50 \text{ pF}$ , $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	1	
	$t_{f(\text{IO})\text{out}}$ $t_{r(\text{IO})\text{out}}$	Output rise and fall time	$C_L = 50 \text{ pF}$ , $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	125	ns
			$C_L = 50 \text{ pF}$ , $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	250	
10	$F_{\max(\text{IO})\text{out}}$	Maximum frequency <sup>(3)</sup>	$C_L = 50 \text{ pF}$ , $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	10	MHz
			$C_L = 50 \text{ pF}$ , $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	2	
	$t_{f(\text{IO})\text{out}}$ $t_{r(\text{IO})\text{out}}$	Output rise and fall time	$C_L = 50 \text{ pF}$ , $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	25	ns
			$C_L = 50 \text{ pF}$ , $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	125	
11	$F_{\max(\text{IO})\text{out}}$	Maximum frequency <sup>(3)</sup>	$C_L = 50 \text{ pF}$ , $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	50	MHz
			$C_L = 50 \text{ pF}$ , $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	8	
	$t_{f(\text{IO})\text{out}}$ $t_{r(\text{IO})\text{out}}$	Output rise and fall time	$C_L = 30 \text{ pF}$ , $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	5	ns
			$C_L = 50 \text{ pF}$ , $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	30	
-	$t_{\text{EXTI}pw}$	Pulse width of external signals detected by the EXTI controller	-	8	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. The maximum frequency is defined in [Figure 19](#).

Table 52. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min. <sup>(1)</sup>	Max. <sup>(1)</sup>	Unit
Input levels					
V <sub>DD</sub>	USB operating voltage <sup>(2)</sup>	-	3.0	3.6	V
V <sub>DI</sub> <sup>(3)</sup>	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
V <sub>CM</sub> <sup>(3)</sup>	Differential common mode range	Includes V <sub>DI</sub> range	0.8	2.5	
V <sub>SE</sub> <sup>(3)</sup>	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V <sub>OL</sub> <sup>(4)</sup>	Static output level low	R <sub>L</sub> of 1.5 kΩ to 3.6 V <sup>(5)</sup>	-	0.3	V
V <sub>OH</sub> <sup>(4)</sup>	Static output level high	R <sub>L</sub> of 15 kΩ to V <sub>SS</sub> <sup>(5)</sup>	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full speed electrical specification, the USB\_DP (D+) pin should be pulled up with a 1.5 k $\Omega$  resistor to a 3.0-to-3.6 V voltage range.
3. Guaranteed by characterization results.
4. Guaranteed by test in production.
5.  $R_L$  is the load connected on the USB drivers.

Figure 25. USB timings: definition of data signal rise and fall time

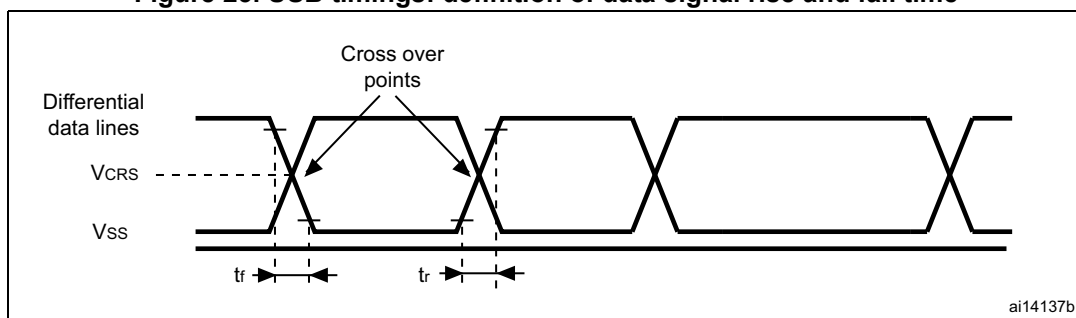


Table 53. USB: full speed electrical characteristics

Driver characteristics <sup>(1)</sup>					
Symbol	Parameter	Conditions	Min	Max	Unit
$t_r$	Rise time <sup>(2)</sup>	$C_L = 50$ pF	4	20	ns
$t_f$	Fall Time <sup>(2)</sup>	$C_L = 50$ pF	4	20	ns
$t_{rfm}$	Rise/ fall time matching	$t_r/t_f$	90	110	%
$V_{CRS}$	Output signal crossover voltage	-	1.3	2.0	V

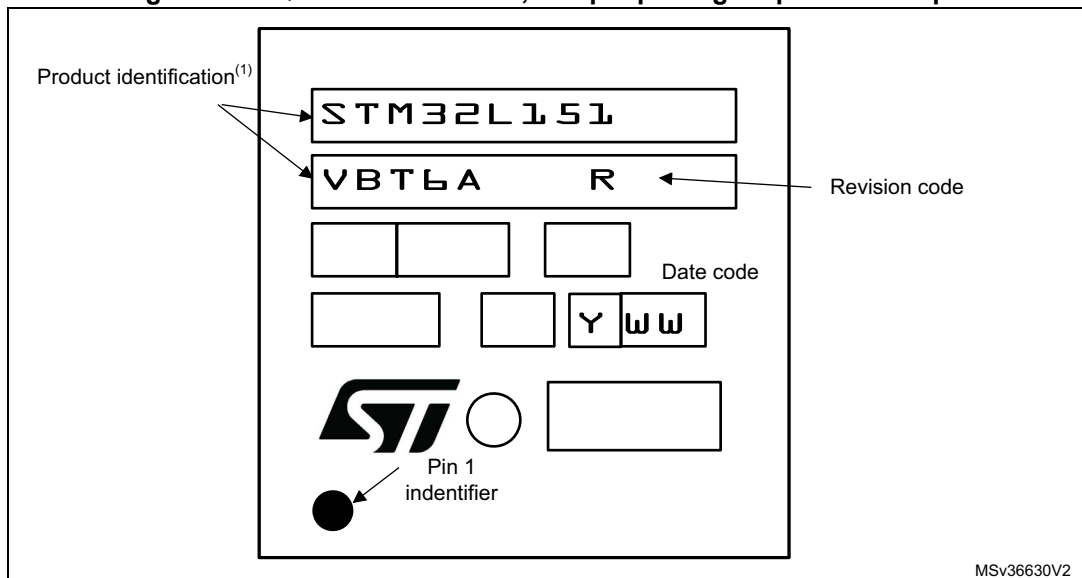
1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification section 7 (version 2.0).

Technical drawing of a square plate with dimensions and labels. The plate is square with a side length of 16.7. The drawing shows the plate from a top-down perspective, with a central vertical line and a central horizontal line intersecting at the center. The plate is divided into four quadrants by these lines. The labels and dimensions are as follows:

- Top-left quadrant:** A vertical stack of 75 small squares, labeled 75 at the top. A dimension of 14.3 is shown for the height of this stack.
- Top-right quadrant:** A horizontal stack of 51 small squares, labeled 51 at the right. A dimension of 0.5 is shown for the width of this stack.
- Bottom-left quadrant:** A horizontal stack of 100 small squares, labeled 100 at the bottom. A dimension of 12.3 is shown for the width of this stack.
- Bottom-right quadrant:** A vertical stack of 26 small squares, labeled 26 at the bottom. A dimension of 0.3 is shown for the height of this stack.
- Overall dimensions:** The total width and height of the plate are both 16.7.
- Other labels:** 76 is labeled at the top of the left edge, 50 at the top of the right edge, and 1 is labeled at the bottom of the left edge.

## LQFP100 device Marking

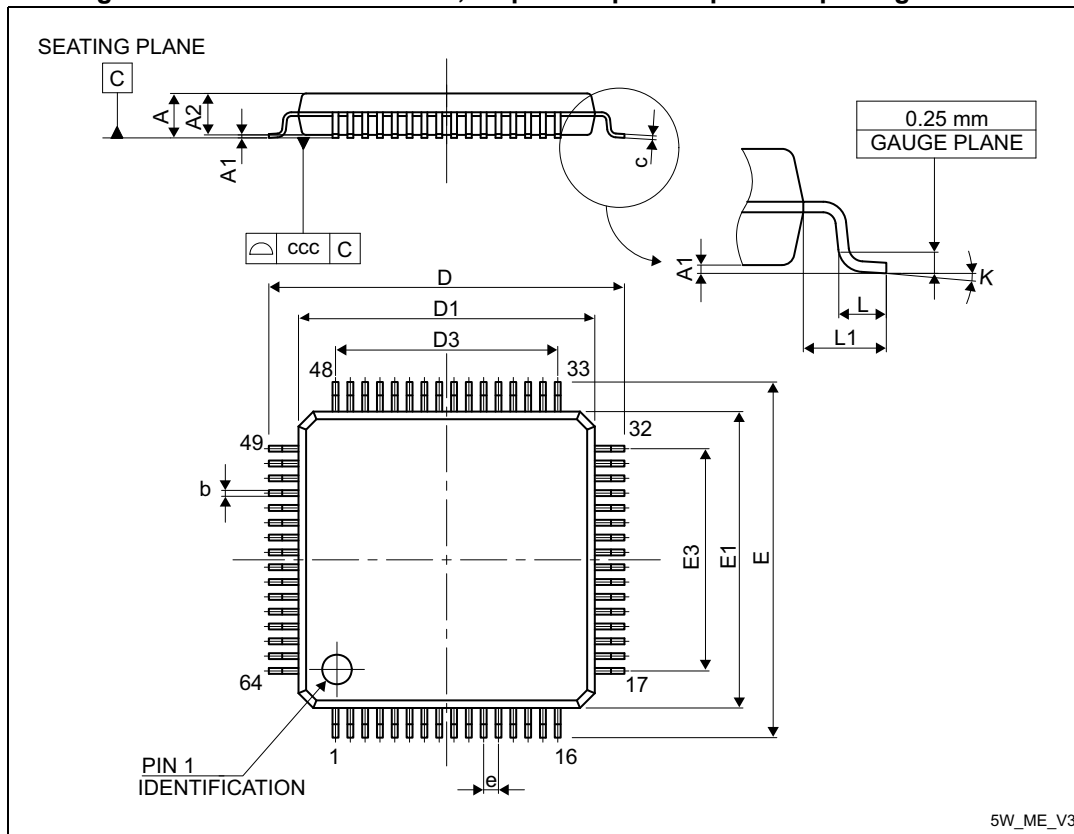
**Figure 32. LQFP100 14 x 14 mm, 100-pin package top view example**



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## 7.2 LQFP64 10 x 10 mm, 64-pin low-profile quad flat package information

Figure 33. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package outline



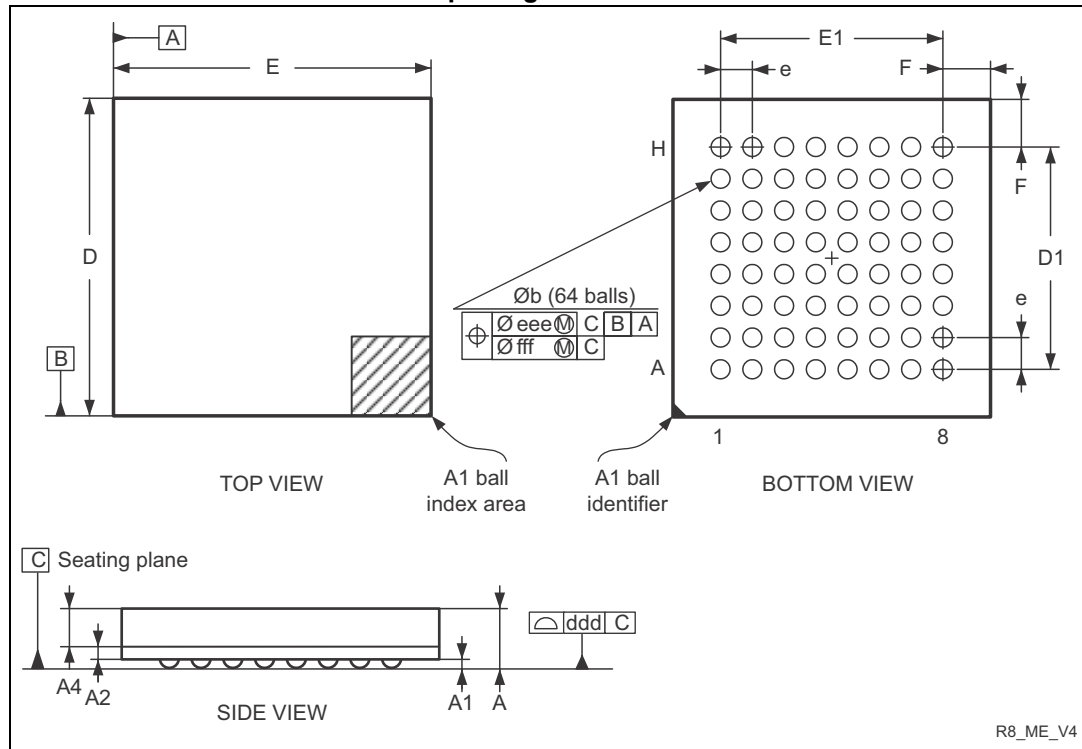
1. Drawing is not to scale.

Table 65. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Typ	Min	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

## 7.6 TFBGA64 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package information

Figure 45. TFBGA64 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package outline



1. Drawing is not to scale.

Table 70. TFBGA64 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package mechanical data

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.200	-	-	0.0472
A1	0.150	-	-	0.0059	-	-
A2	-	0.200	-	-	0.0079	-
A4	-	-	0.600	-	-	0.0236
b	0.250	0.300	0.350	0.0098	0.0118	0.0138
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	-	3.500	-	-	0.1378	-
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	-	3.500	-	-	0.1378	-
e	-	0.500	-	-	0.0197	-
F	-	0.750	-	-	0.0295	-