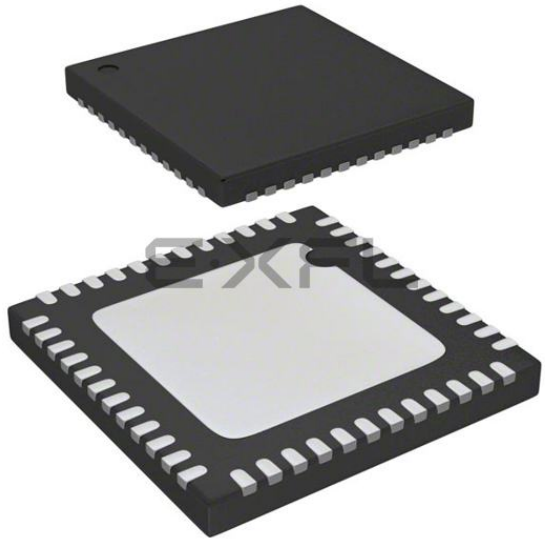


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152cbu6a

Contents

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A devices embed a nested vectored interrupt controller able to handle up to 45 maskable interrupt channels (not including the 16 interrupt lines of Cortex-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving*, higher-priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.3 Reset and supply management

3.3.1 Power supply schemes

- V_{DD} = 1.65 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

The device exists in two versions:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the V_{DD} threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the V_{DD} min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the power ramp-up should guarantee that 1.65 V is reached on V_{DD} at least 1 ms after it exits the POR area.

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The regulator has three operation modes: main (MR), low-power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32K osc, RCC_CSR).

3.3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from Flash memory
- Boot from System Memory
- Boot from embedded RAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1 or USART2. See the application note “STM32 microcontroller system memory boot mode” (AN2606) for details.

Table 10. Alternate function input/output

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART 1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
BOOT0	BOOT0	-	-	-	-	-	-	-	-	-	-	-	-	-	-
NRST	NRST	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PA0-WKUP1	-	TIM2_CH1_ETR	-	-	-	-	-	USART2_CTS	-	-	-	-	-	TIMx_IC1	EVENTOUT
PA1	-	TIM2_CH2	-	-	-	-	-	USART2_RTS	-	-	[SEG0]	-	-	TIMx_IC2	EVENTOUT
PA2	-	TIM2_CH3	-	TIM9_CH1	-	-	-	USART2_TX	-	-	[SEG1]	-	-	TIMx_IC3	EVENTOUT
PA3	-	TIM2_CH4	-	TIM9_CH2	-	-	-	USART2_RX	-	-	[SEG2]	-	-	TIMx_IC4	EVENTOUT
PA4	-	-	-	-	-	SPI1_NSS	-	USART2_CK	-	-	-	-	-	TIMx_IC1	EVENTOUT
PA5	-	TIM2_CH1_ETR	-	-	-	SPI1_SCK	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PA6	-	-	TIM3_CH1	TIM10_CH1	-	SPI1_MISO	-	-	-	-	[SEG3]	-	-	TIMx_IC3	EVENTOUT
PA7	-	-	TIM3_CH2	TIM11_CH1	-	SPI1_MOSI	-	-	-	-	[SEG4]	-	-	TIMx_IC4	EVENTOUT
PA8	MCO	-	-	-	-	-	-	USART1_CK	-	-	[COM0]	-	-	TIMx_IC1	EVENTOUT
PA9	-	-	-	-	-	-	-	USART1_TX	-	-	[COM1]	-	-	TIMx_IC2	EVENTOUT
PA10	-	-	-	-	-	-	-	USART1_RX	-	-	[COM2]	-	-	TIMx_IC3	EVENTOUT
PA11	-	-	-	-	-	SPI1_MISO	-	USART1_CTS	-	-	-	-	-	TIMx_IC4	EVENTOUT
PA12	-	-	-	-	-	SPI1_MOSI	-	USART1_RTS	-	-	-	-	-	TIMx_IC1	EVENTOUT
PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PA15	JTDI	TIM2_CH1_ETR	-	-	-	SPI1_NSS	-	-	-	-	SEG17	-	-	TIMx_IC4	EVENTOUT
PB0	-	-	TIM3_CH3	-	-	-	-	-	-	-	[SEG5]	-	-	-	EVENTOUT
PB1	-	-	TIM3_CH4	-	-	-	-	-	-	-	[SEG6]	-	-	-	EVENTOUT
PB2	BOOT1	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PB3	JTDO	TIM2_CH2	-	-	-	SPI1_SCK	-	-	-	-	[SEG7]	-	-	-	EVENTOUT

Table 10. Alternate function input/output (continued)

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART 1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
PB4	NJTRST	-	TIM3_CH1	-	-	SPI1_MISO	-	-	-	-	[SEG8]	-	-	-	EVENTOUT
PB5	-	-	TIM3_CH2	-	I2C1_ SMBA	SPI1_MOSI	-	-	-	-	[SEG9]	-	-	-	EVENTOUT
PB6	-	-	TIM4_CH1	-	I2C1_SCL	-	-	USART1_TX	-	-	-	-	-	-	EVENTOUT
PB7	-	-	TIM4_CH2	-	I2C1_SDA	-	-	USART1_RX	-	-	-	-	-	-	EVENTOUT
PB8	-	-	TIM4_CH3	TIM10_CH1*	I2C1_SCL	-	-	-	-	-	SEG16	-	-	-	EVENTOUT
PB9	-	-	TIM4_CH4	TIM11_CH1*	I2C1_SDA	-	-	-	-	-	[COM3]	-	-	-	EVENTOUT
PB10	-	TIM2_CH3	-	-	I2C2_SCL	-	-	USART3_TX	-	-	SEG10	-	-	-	EVENTOUT
PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	-	USART3_RX	-	-	SEG11	-	-	-	EVENTOUT
PB12	-	-	-	TIM10_CH1	I2C2_ SMBA	SPI2_NSS	-	USART3_CK	-	-	SEG12	-	-	-	EVENTOUT
PB13	-	-	-	TIM9_CH1	-	SPI2_SCK	-	USART3_CTS	-	-	SEG13	-	-	-	EVENTOUT
PB14	-	-	-	TIM9_CH2	-	SPI2_MISO	-	USART3_RTS	-	-	SEG14	-	-	-	EVENTOUT
PB15	-	-	-	TIM11_CH1	-	SPI2_MOSI	-	-	-	-	SEG15	-	-	-	EVENTOUT
PC0	-	-	-	-	-	-	-	-	-	-	SEG18	-	-	TIMx_IC1	EVENTOUT
PC1	-	-	-	-	-	-	-	-	-	-	SEG19	-	-	TIMx_IC2	EVENTOUT
PC2	-	-	-	-	-	-	-	-	-	-	SEG20	-	-	TIMx_IC3	EVENTOUT
PC3	-	-	-	-	-	-	-	-	-	-	SEG21	-	-	TIMx_IC4	EVENTOUT
PC4	-	-	-	-	-	-	-	-	-	-	SEG22	-	-	TIMx_IC1	EVENTOUT
PC5	-	-	-	-	-	-	-	-	-	-	SEG23	-	-	TIMx_IC2	EVENTOUT
PC6	-	-	TIM3_CH1	-	-	-	-	-	-	-	SEG24	-	-	TIMx_IC3	EVENTOUT
PC7	-	-	TIM3_CH2	-	-	-	-	-	-	-	SEG25	-	-	TIMx_IC4	EVENTOUT
PC8	-	-	TIM3_CH3	-	-	-	-	-	-	-	SEG26	-	-	TIMx_IC1	EVENTOUT
PC9	-	-	TIM3_CH4	-	-	-	-	-	-	-	SEG27	-	-	TIMx_IC2	EVENTOUT

Table 10. Alternate function input/output (continued)

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART 1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
PC10	-	-	-	-	-	-	-	USART3_TX	-	-	COM4 / SEG28 / SEG40	-	-	TIMx_IC3	EVENTOUT
PC11	-	-	-	-	-	-	-	USART3_RX	-	-	COM5 / SEG29 / SEG41	-	-	TIMx_IC4	EVENTOUT
PC12	-	-	-	-	-	-	-	USART3_CK	-	-	COM6 / SEG30 / SEG42	-	-	TIMx_IC1	EVENTOUT
PC13-WKUP2	-	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PC14-OSC32_IN	-	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PC15-OSC32_OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PD0	-	-	-	TIM9_CH1	-	SPI2_NSS	-	-	-	-	-	-	-	TIMx_IC1	EVENTOUT
PD1	-	-	-	-	-	SPI2_SCK	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PD2	-	-	TIM3_ETR	-	-	-	-	-	-	-	COM7 / SEG31 / SEG43	-	-	TIMx_IC3	EVENTOUT
PD3	-	-	-	-	-	SPI2_MISO	-	USART2_CTS	-	-	-	-	-	TIMx_IC4	EVENTOUT
PD4	-	-	-	-	-	SPI2_MOSI	-	USART2_RTS	-	-	-	-	-	TIMx_IC1	EVENTOUT
PD5	-	-	-	-	-	-	-	USART2_TX	-	-	-	-	-	TIMx_IC2	EVENTOUT
PD6	-	-	-	-	-	-	-	USART2_RX	-	-	-	-	-	TIMx_IC3	EVENTOUT
PD7	-	-	-	TIM9_CH2	-	-	-	USART2_CK	-	-	-	-	-	TIMx_IC4	EVENTOUT
PD8	-	-	-	-	-	-	-	USART3_TX	-	-	-	-	-	TIMx_IC1	EVENTOUT
PD9	-	-	-	-	-	-	-	USART3_RX	-	-	-	-	-	TIMx_IC2	EVENTOUT

6.1.6 Power supply scheme

Figure 12. Power supply scheme

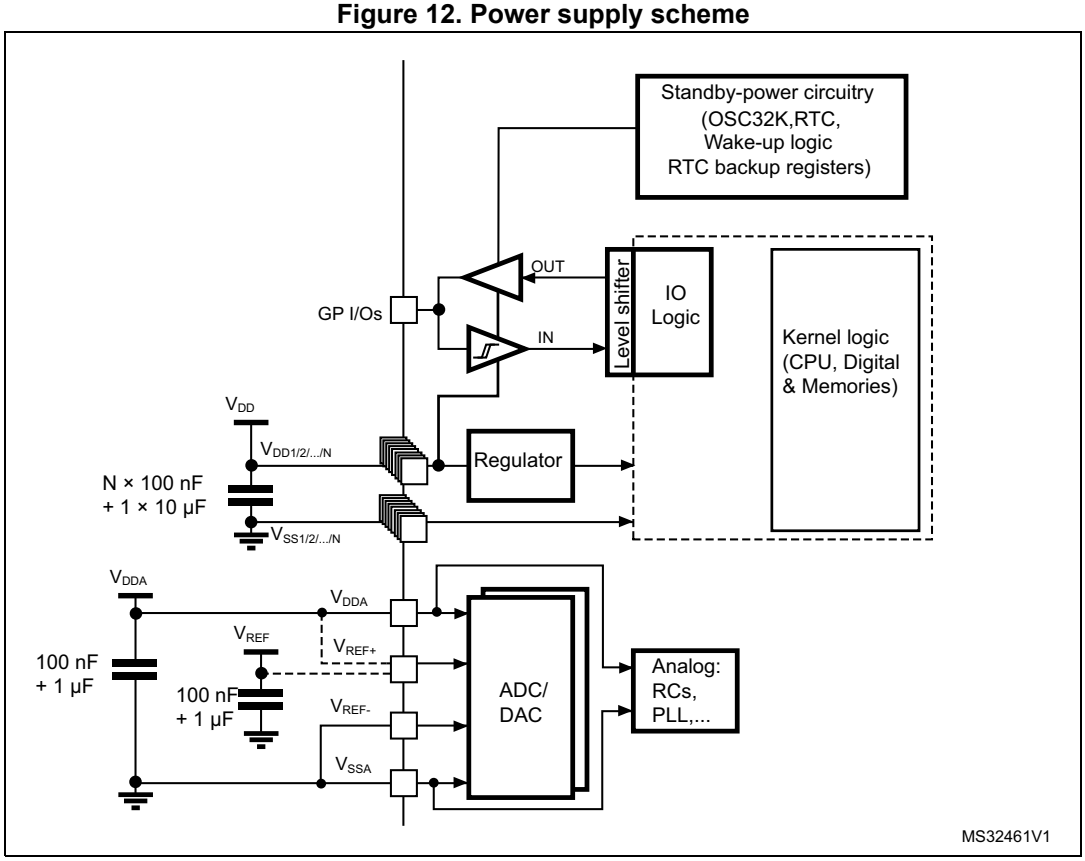


Table 22. Current consumption in Low-power sleep mode

Symbol	Parameter	Conditions			Typ	Max (1)	Unit
I_{DD} (LP Sleep)	Supply current in Low-power sleep mode	All peripherals OFF, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz Flash OFF	T_A = -40 °C to 25 °C	5.5	-	µA
			MSI clock, 65 kHz f_{HCLK} = 32 kHz Flash ON	T_A = -40 °C to 25 °C	15	16	
				T_A = 85 °C	20	23	
				T_A = 105 °C	24	26	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz, Flash ON	T_A = -40 °C to 25 °C	15	16	
				T_A = 85 °C	20.5	23	
				T_A = 105 °C	25.4	27	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz, Flash ON	T_A = -40 °C to 25 °C	18	20	
				T_A = 55 °C	21	22	
				T_A = 85 °C	23	27	
				T_A = 105 °C	28	31	
		TIM9 and USART1 enabled, Flash ON, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz	T_A = -40 °C to 25 °C	15	16	
				T_A = 85 °C	20	22	
				T_A = 105 °C	24	26	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz	T_A = -40 °C to 25 °C	15	16	
				T_A = 85 °C	20.5	23	
				T_A = 105 °C	25.4	27	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz	T_A = -40 °C to 25 °C	18	20	
				T_A = 55 °C	21	22	
				T_A = 85 °C	23	27	
				T_A = 105 °C	28	30	
I_{DD} Max (LP Sleep)	Max allowed current in Low-power Sleep mode	V_{DD} from 1.65 V to 3.6 V	-	-	-	200	

1. Guaranteed by characterization results, unless otherwise specified.

Table 23. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions			Typ(1)	Max (1)(2)	Unit
I_{DD} (Stop with RTC)	Supply current in Stop mode with RTC enabled	RTC clocked by LSI, regulator in LP mode, HSI and HSE OFF (no independent watchdog)	LCD OFF	T_A = -40°C to 25°C V_{DD} = 1.8 V	1.13	-	µA
				T_A = -40°C to 25°C	1.38	4	
				T_A = 55°C	1.70	6	
				T_A= 85°C	3.30	10	
				T_A = 105°C	7.80	23	
			LCD ON (static duty)(3)	T_A = -40°C to 25°C	1.50	6	
				T_A = 55°C	1.80	7	
				T_A= 85°C	3.45	12	
				T_A = 105°C	8.02	27	
			LCD ON (1/8 duty)(4)	T_A = -40°C to 25°C	3.80	10	
				T_A = 55°C	4.30	11	
				T_A= 85°C	6.10	16	
				T_A = 105°C	10.8	44	
		RTC clocked by LSE external clock (32.768 kHz), regulator in LP mode, HSI and HSE OFF (no independent watchdog)	LCD OFF	T_A = -40°C to 25°C	1.50	-	
				T_A = 55°C	1.90	-	
				T_A= 85°C	3.65	-	
				T_A = 105°C	8.25	-	
			LCD ON (static duty)(3)	T_A = -40°C to 25°C	1.60	-	
				T_A = 55°C	2.05	-	
				T_A= 85°C	3.75	-	
				T_A = 105°C	8.40	-	
			LCD ON (1/8 duty)(4)	T_A = -40°C to 25°C	3.90	-	
				T_A = 55°C	4.55	-	
				T_A= 85°C	6.35	-	
				T_A = 105°C	11.10	-	
		RTC clocked by LSE (no independent watchdog)(5)	LCD OFF	T_A = -40°C to 25°C V_{DD} = 1.8 V	1.23	-	
				T_A = -40°C to 25°C V_{DD} = 3.0 V	1.50	-	
				T_A = -40°C to 25°C V_{DD} = 3.6 V	1.75	-	

Table 26. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	f_{HCLK} = 32 MHz	0.4	-	µs
$t_{WUSLEEP\_LP}$	Wakeup from Low-power sleep mode f_{HCLK} = 262 kHz	f_{HCLK} = 262 kHz Flash enabled	46	-	
		f_{HCLK} = 262 kHz Flash switched OFF	46	-	
t_{WUSTOP}	Wakeup from Stop mode, regulator in Run mode	$f_{HCLK} = f_{MSI}$ = 4.2 MHz	8.2	-	
	Wakeup from Stop mode, regulator in low-power mode	$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage Range 1 and 2	7.7	8.9	
		$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage Range 3	8.2	13.1	
		$f_{HCLK} = f_{MSI}$ = 2.1 MHz	10.2	13.4	
		$f_{HCLK} = f_{MSI}$ = 1.05 MHz	16	20	
		$f_{HCLK} = f_{MSI}$ = 524 kHz	31	37	
		$f_{HCLK} = f_{MSI}$ = 262 kHz	57	66	
		$f_{HCLK} = f_{MSI}$ = 131 kHz	112	123	
		f_{HCLK} = MSI = 65 kHz	221	236	
$t_{WUSTDBY}$	Wakeup from Standby mode FWU bit = 1	f_{HCLK} = MSI = 2.1 MHz	58	104	
	Wakeup from Standby mode FWU bit = 0	f_{HCLK} = MSI = 2.1 MHz	2.6	3.25	ms

1. Guaranteed by characterization results, unless otherwise specified

Low-speed external user clock generated from an external source

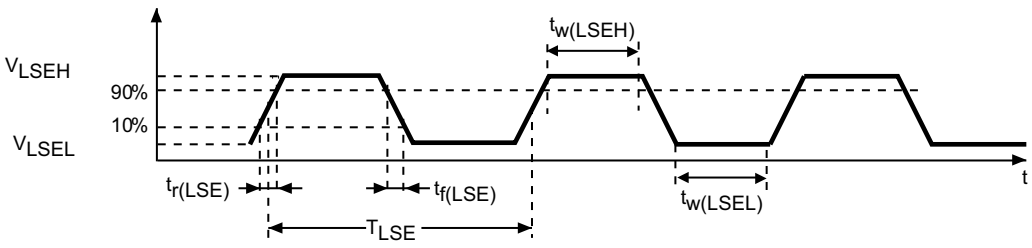
The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 14*.

Table 28. Low-speed external user clock characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	1	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	$0.7V_{DD}$	-	V_{DD}	-
V_{LSEL}	OSC32_IN input pin low level voltage	V_{SS}	-	$0.3V_{DD}$	-
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	465	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time	-	-	10	
$C_{IN(LSE)}$	OSC32_IN input capacitance	-	0.6	-	pF

1. Guaranteed by design.

Figure 16. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 1 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 29*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 29. HSE oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	1		24	MHz
R_F	Feedback resistor	-		200	-	kΩ

Table 29. HSE oscillator characteristics(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω	-	20	-	pF
I_{HSE}	HSE driving current	V_{DD}= 3.3 V, V_{IN} = V_{SS} with 30 pF load	-	-	3	mA
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.7 (stabilized)	mA
		C = 10 pF f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.46 (stabilized)	
g_m	Oscillator transconductance	Startup	3.5	-	-	mA /V
$t_{SU(HSE)}$ (4)	Startup time	V_{DD} is stabilized	-	1	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 17*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during the device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 38*. They are based on the EMS levels and classes defined in application note AN1709.

Table 38. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

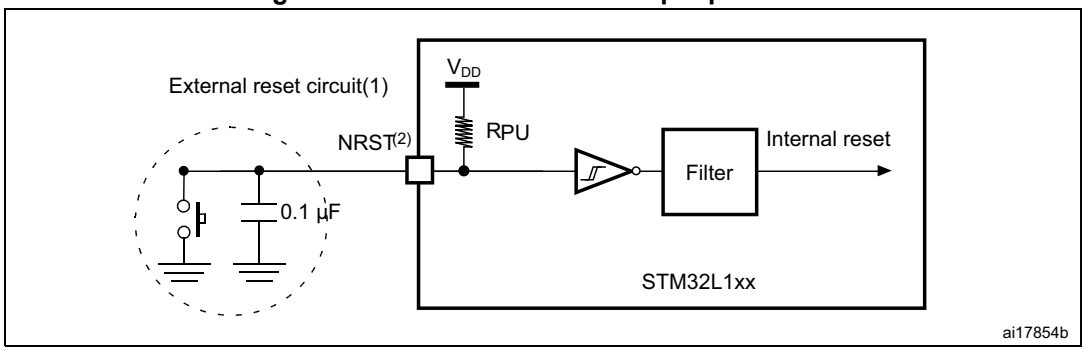
The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

Figure 20. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 46*. Otherwise the reset will not be taken into account by the device.

6.3.15 TIM timer characteristics

The parameters given in *Table 47* are guaranteed by design.

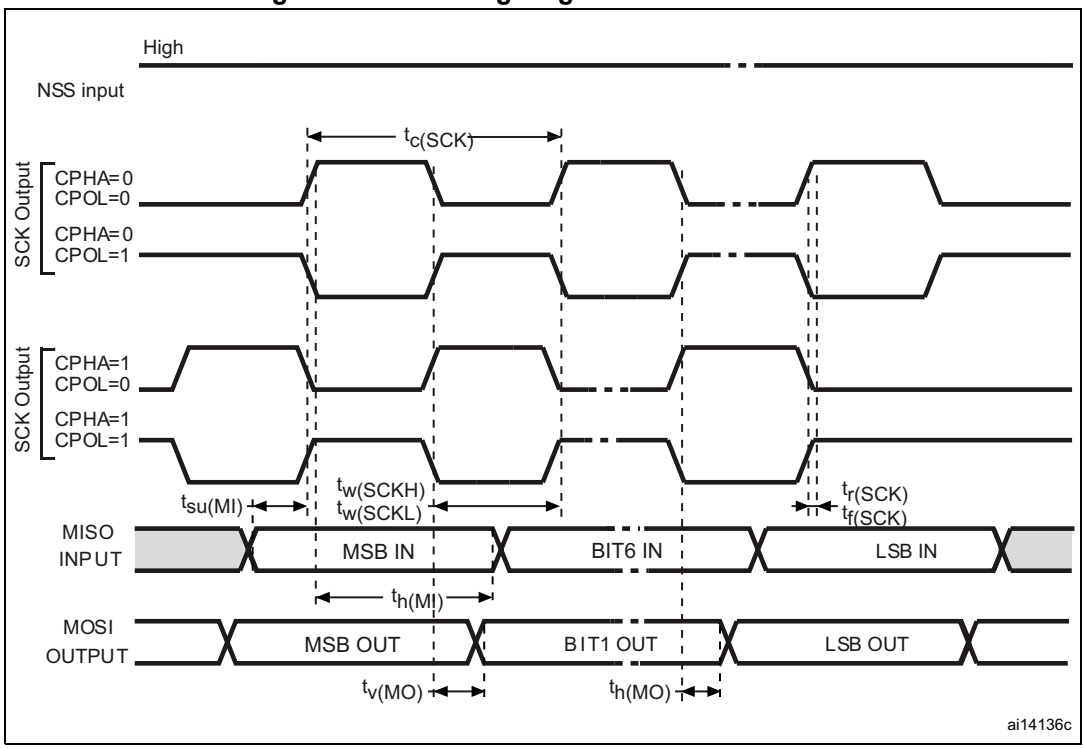
Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 47. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	31.25	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 32 MHz	0	16	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected (timer's prescaler disabled)	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	0.0312	2048	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	-	134.2	s

1. TIMx is used as a general term to refer to the TIM2, TIM3 and TIM4 timers.

Figure 24. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

USB characteristics

The USB interface is USB-IF certified (full speed).

Table 51. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design.

Table 52. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage(2)	-	3.0	3.6	V
V_{DI}(3)	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(3)	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V_{OL}(4)	Static output level low	R_L of 1.5 kΩ to 3.6 V(5)	-	0.3	V
V_{OH}(4)	Static output level high	R_L of 15 kΩ to V_{SS}(5)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. Guaranteed by characterization results.
4. Guaranteed by test in production.
5. R_L is the load connected on the USB drivers.

Figure 25. USB timings: definition of data signal rise and fall time

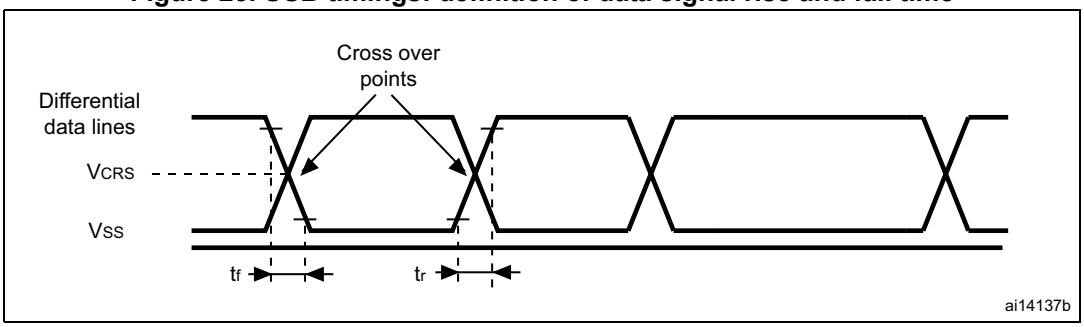


Table 53. USB: full speed electrical characteristics

Driver characteristics(1)					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall Time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification section 7 (version 2.0).

Figure 26. ADC accuracy characteristics

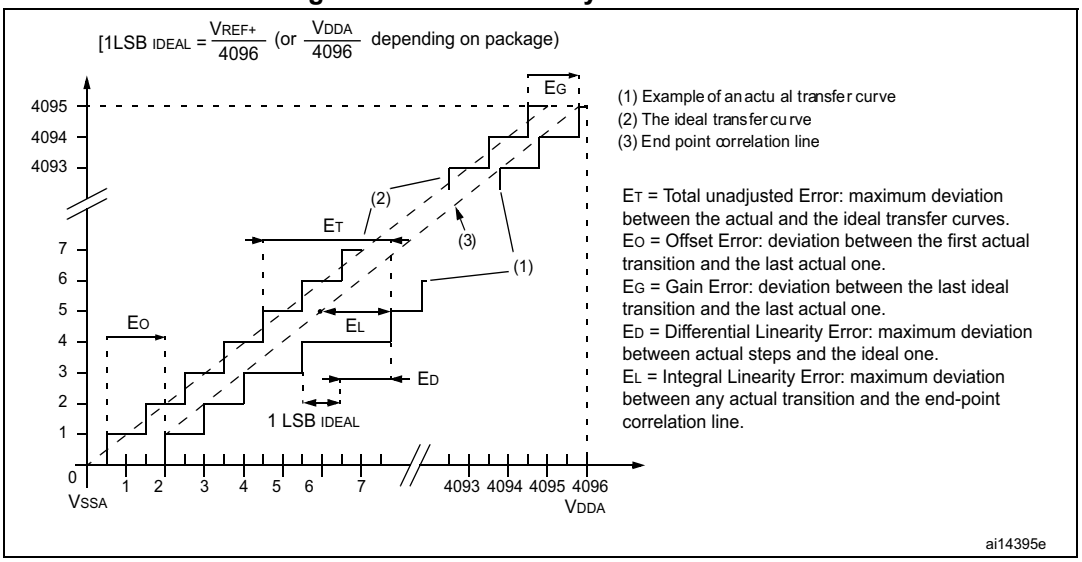
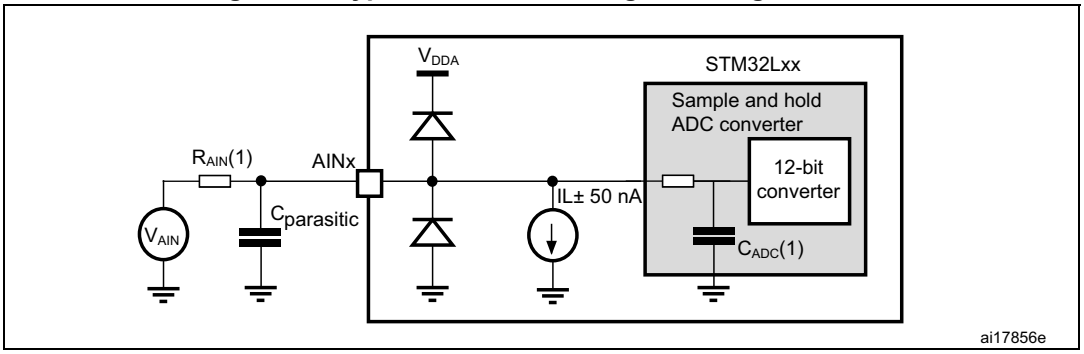


Figure 27. Typical connection diagram using the ADC



1. Refer to *Table 57: Maximum source impedance RAIN max* for the value of R_{AIN} and *Table 55: ADC characteristics* for the value of CADC
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

6.3.21 LCD controller (STM32L152x6/8/B-A devices only)

The STM32L152xx-A devices embed a built-in step-up converter to provide a constant LCD reference voltage independently from the V_{DD} voltage. An external capacitor C_{ext} must be connected to the V_{LCD} pin to decouple this converter.

Table 63. LCD controller characteristics

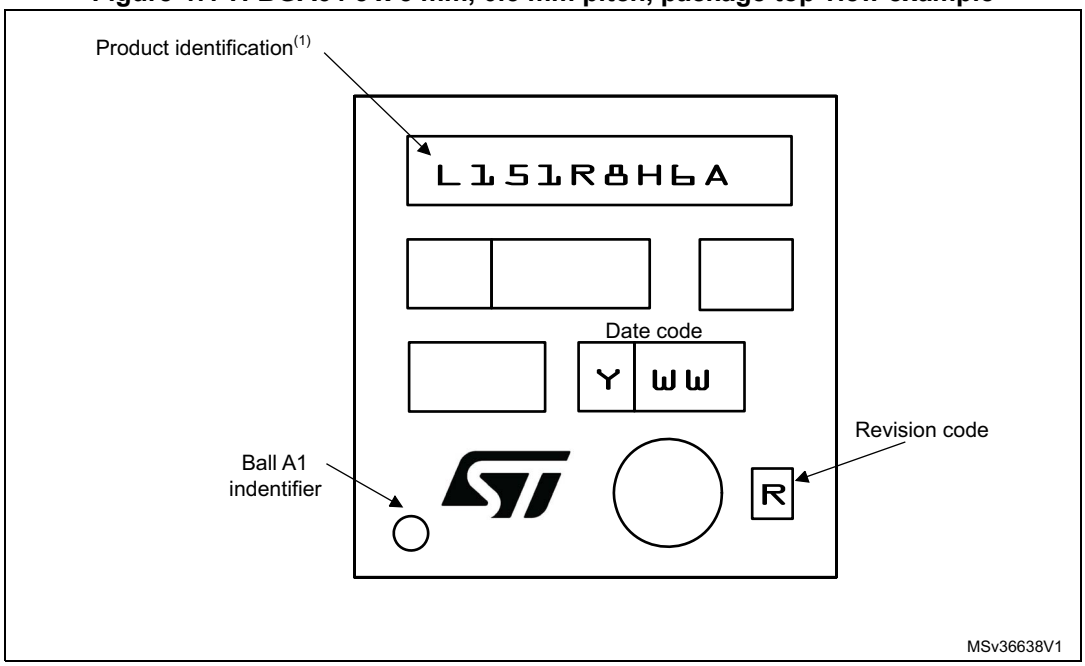
Symbol	Parameter	Min	Typ	Max	Unit
V_{LCD}	LCD external voltage	-	-	3.6	V
V_{LCD0}	LCD internal reference voltage 0	-	2.6	-	
V_{LCD1}	LCD internal reference voltage 1	-	2.73	-	
V_{LCD2}	LCD internal reference voltage 2	-	2.86	-	
V_{LCD3}	LCD internal reference voltage 3	-	2.98	-	
V_{LCD4}	LCD internal reference voltage 4	-	3.12	-	
V_{LCD5}	LCD internal reference voltage 5	-	3.26	-	
V_{LCD6}	LCD internal reference voltage 6	-	3.4	-	
V_{LCD7}	LCD internal reference voltage 7	-	3.55	-	
C_{ext}	V_{LCD} external capacitance	0.1	-	2	µF
I_{LCD}(1)	Supply current at V_{DD} = 2.2 V	-	3.3	-	µA
	Supply current at V_{DD} = 3.0 V	-	3.1	-	
R_{Htot}(2)	Low drive resistive network overall value	5.28	6.6	7.92	MΩ
R_L(2)	High drive resistive network total value	192	240	288	kΩ
V_{44}	Segment/Common highest level voltage	-	-	V_{LCD}	V
V_{34}	Segment/Common 3/4 level voltage	-	3/4 V_{LCD}	-	V
V_{23}	Segment/Common 2/3 level voltage	-	2/3 V_{LCD}	-	
V_{12}	Segment/Common 1/2 level voltage	-	1/2 V_{LCD}	-	
V_{13}	Segment/Common 1/3 level voltage	-	1/3 V_{LCD}	-	
V_{14}	Segment/Common 1/4 level voltage	-	1/4 V_{LCD}	-	
V_0	Segment/Common lowest level voltage	0	-	-	
ΔVxx(2)	Segment/Common level voltage error T_A = -40 to 105 °C	-	-	±50	mV

1. LCD enabled with 3 V internal step-up active, 1/8 duty, 1/4 bias, division ratio= 64, all pixels active, no LCD connected
2. Guaranteed by characterization results.

TFBGA64 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Figure 47. TFBGA64 5 x 5 mm, 0.5 mm pitch, package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.