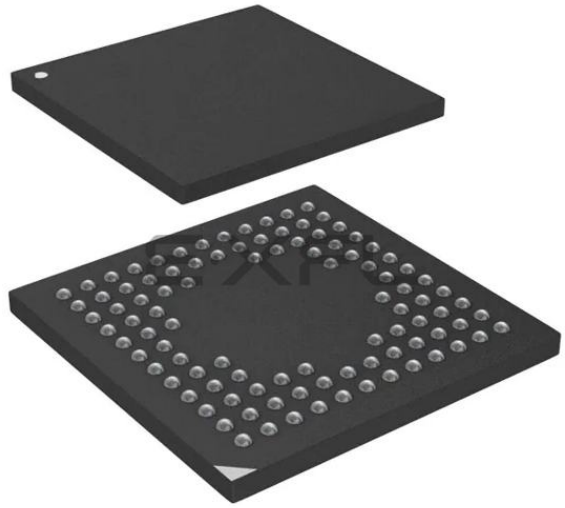

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, Cap Sense, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 83 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 24x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-UFBGA |
| Supplier Device Package | 100-UFBGA (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152v8h6a |

# 2 Description

The ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A devices incorporate the connectivity power of the universal serial bus (USB) with the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a frequency of 32 MHz (33.3 DMIPS), a memory protection unit (MPU), high-speed embedded memories (Flash memory up to 128 Kbytes and RAM up to 32 Kbytes) and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

All the devices offer a 12-bit ADC, 2 DACs and 2 ultra-low-power comparators, six general-purpose 16-bit timers and two basic timers, which can be used as time bases.

Moreover, the STM32L151x6/8/B-A and STM32L152x6/8/B-A devices contain standard and advanced communication interfaces: up to two $I^2C$s and SPIs, three USARTs and a USB. The STM32L151x6/8/B-A and STM32L152x6/8/B-A devices offer up to 20 capacitive sensing channels to simply add touch sensing functionality to any application.

They also include a real-time clock with sub-second counting and a set of backup registers that remain powered in Standby mode.

Finally, the integrated LCD controller (except STM32L151x6/8/B-A devices) has a built-in LCD voltage generator that allows to drive up to 8 multiplexed LCDs with contrast independent of the supply voltage.

The ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. They are available in the -40 to +85 °C and -40 to +105°C temperature ranges. A comprehensive set of power-saving modes allows the design of low-power applications.


## 3.4 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler**: to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching**: clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management**: to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Master clock source**: three different clock sources can be used to drive the master clock:
  - 1-24 MHz high-speed external crystal (HSE), that can supply a PLL
  - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65.5 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz) with a consumption proportional to speed, down to 750 nA typical. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a ±0.5% accuracy.
- **Auxiliary clock source**: two ultra-low-power clock sources that can be used to drive the LCD controller and the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE)
  - 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.
- **RTC and LCD clock sources:** the LSI, LSE or HSE sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **USB clock source:** the embedded PLL has a dedicated 48 MHz clock output to supply the USB interface.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 2.1 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.
- **Clock-out capability (MCO: microcontroller clock output):** it outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

## 3.5 Low-power real-time clock and backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the sub-second, second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are made automatically. The RTC provides two programmable alarms and programmable periodic interrupts with wakeup from Stop and Standby modes.

The programmable wakeup time ranges from 120 µs to 36 hours.

The RTC can be calibrated with an external 512 Hz output, and a digital compensation circuit helps reduce drift due to crystal deviation. The RTC can also be automatically corrected with a 50/60Hz stable power line.

The RTC calendar can be updated on the fly down to sub second precision, which enables network system synchronization. A time stamp can record an external event occurrence, and generates an interrupt.

There are twenty 32-bit backup registers provided to store 80 bytes of user application data. They are cleared in case of tamper detection. Three pins can be used to detect tamper events. A change on one of these pins can reset backup register and generate an interrupt. To prevent false tamper event, like ESD event, these three tamper inputs can be digitally filtered.

## 3.6 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated AFIO registers. All GPIOs are high current capable. The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to the AHB with a toggling speed of up to 16 MHz.

### External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 83 GPIOs can be connected to the 16 external interrupt lines. The 7 other lines are connected to RTC, PVD, USB or Comparator events.

### 3.15.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit down-counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

## 3.16 Communication interfaces

### 3.16.1 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7- and 10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

### 3.16.2 Universal synchronous/asynchronous receiver transmitter (USART)

All USART interfaces are able to communicate at speeds of up to 4 Mbit/s. They provide hardware management of the CTS and RTS signals and are ISO 7816 compliant. They support IrDA SIR ENDEC and have LIN Master/Slave capability.

All USART interfaces can be served by the DMA controller.

### 3.16.3 Serial peripheral interface (SPI)

Up to two SPIs are able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

Both SPIs can be served by the DMA controller.

### 3.16.4 Universal serial bus (USB)

The STM32L151x6/8/B-A and STM32L152x6/8/B-A devices embed a USB device peripheral compatible with the USB full speed 12 Mbit/s. The USB interface implements a full speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and supports suspend/resume. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

Table 9. STM32L151x6/8/B-A and STM32L152x6/8/B-A pin definitions (continued)

| Pins | | | | | Pin name | Pin type(1) | I/O structure | Main function(2) (after reset) | Pins functions | |
|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | LQFP64 | TFBGA64 | UFBGA100 | LQFP48 or UFQFPN48 | | | | | Alternate functions | Additional functions |
| 35 | 26 | F5 | M5 | 18 | PB0 | I/O | TC | PB0 | TIM3_CH3/ LCD_SEG5 | ADC_IN8/ COMP1_INP/ VREF_OUT /VLCDRAIL3 |
| 36 | 27 | G5 | M6 | 19 | PB1 | I/O | FT | PB1 | TIM3_CH4/ LCD_SEG6 | ADC_IN9/ COMP1_INP/ VREF_OUT |
| 37 | 28 | G6 | L6 | 20 | PB2 | I/O | FT | PB2/ BOOT1 | BOOT1 | VLCDRAIL1 |
| 38 | - | - | M7 | - | PE7 | I/O | TC | PE7 | - | ADC_IN22/ COMP1_INP |
| 39 | - | - | L7 | - | PE8 | I/O | TC | PE8 | - | ADC_IN23/ COMP1_INP |
| 40 | - | - | M8 | - | PE9 | I/O | TC | PE9 | TIM2_CH1_ETR | ADC_IN24/ COMP1_INP |
| 41 | - | - | L8 | - | PE10 | I/O | TC | PE10 | TIM2_CH2 | ADC_IN25/ COMP1_INP |
| 42 | - | - | M9 | - | PE11 | I/O | FT | PE11 | TIM2_CH3 | VLCDRAIL2 |
| 43 | - | - | L9 | - | PE12 | I/O | FT | PE12 | TIM2_CH4/ SPI1_NSS | VLCDRAIL3 |
| 44 | - | - | M10 | - | PE13 | I/O | FT | PE13 | SPI1_SCK | - |
| 45 | - | - | M11 | - | PE14 | I/O | FT | PE14 | SPI1_MISO | - |
| 46 | - | - | M12 | - | PE15 | I/O | FT | PE15 | SPI1_MOSI | - |
| 47 | 29 | G7 | L10 | 21 | PB10 | I/O | FT | PB10 | I2C2_SCL/USART3_TX /TIM2_CH3/ LCD_SEG10 | - |
| 48 | 30 | H7 | L11 | 22 | PB11 | I/O | FT | PB11 | I2C2_SDA/USART3_RX /TIM2_CH4/ LCD_SEG11 | - |
| 49 | 31 | D6 | F12 | 23 | $V_{SS\_1}$ | S | - | $V_{SS\_1}$ | - | - |
| 50 | 32 | E6 | G12 | 24 | $V_{DD\_1}$ | S | - | $V_{DD\_1}$ | - | - |

Table 9. STM32L151x6/8/B-A and STM32L152x6/8/B-A pin definitions (continued)

| Pins | | | | | Pin name | Pin type(1) | I/O structure | Main function(2) (after reset) | Pins functions | |
|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | LQFP64 | TFBGA64 | UFBGA100 | LQFP48 or UFQFPN48 | | | | | Alternate functions | Additional functions |
| 51 | 33 | H8 | L12 | 25 | PB12 | I/O | FT | PB12 | SPI2_NSS/I2C2_SMBA/ USART3_CK/ LCD_SEG12/ TIM10_CH1 | ADC_IN18/ COMP1_INP /VLCDRAIL2 |
| 52 | 34 | G8 | K12 | 26 | PB13 | I/O | FT | PB13 | SPI2_SCK/ USART3_CTS/ LCD_SEG13/TIM9_CH1 | ADC_IN19/ COMP1_INP |
| 53 | 35 | F8 | K11 | 27 | PB14 | I/O | FT | PB14 | SPI2_MISO/ USART3_RTS/ LCD_SEG14/TIM9_CH2 | ADC_IN20/ COMP1_INP |
| 54 | 36 | F7 | K10 | 28 | PB15 | I/O | FT | PB15 | SPI2_MOSI/ LCD_SEG15/ TIM11_CH1 | ADC_IN21/ COMP1_INP/ RTC_REFIN |
| 55 | - | - | K9 | - | PD8 | I/O | FT | PD8 | USART3_TX/ LCD_SEG28 | - |
| 56 | - | - | K8 | - | PD9 | I/O | FT | PD9 | USART3_RX/ LCD_SEG29 | - |
| 57 | - | - | J12 | - | PD10 | I/O | FT | PD10 | USART3_CK/ LCD_SEG30 | - |
| 58 | - | - | J11 | - | PD11 | I/O | FT | PD11 | USART3_CTS/ LCD_SEG31 | - |
| 59 | - | - | J10 | - | PD12 | I/O | FT | PD12 | TIM4_CH1/ USART3_RTS/ LCD_SEG32 | - |
| 60 | - | - | H12 | - | PD13 | I/O | FT | PD13 | TIM4_CH2/LCD_SEG33 | - |
| 61 | - | - | H11 | - | PD14 | I/O | FT | PD14 | TIM4_CH3/LCD_SEG34 | - |
| 62 | - | - | H10 | - | PD15 | I/O | FT | PD15 | TIM4_CH4/LCD_SEG35 | - |
| 63 | 37 | F6 | E12 | - | PC6 | I/O | FT | PC6 | TIM3_CH1/LCD_SEG24 | - |
| 64 | 38 | E7 | E11 | - | PC7 | I/O | FT | PC7 | TIM3_CH2/LCD_SEG25 | - |
| 65 | 39 | E8 | E10 | - | PC8 | I/O | FT | PC8 | TIM3_CH3/LCD_SEG26 | - |
| 66 | 40 | D8 | D12 | - | PC9 | I/O | FT | PC9 | TIM3_CH4/LCD_SEG27 | - |

## Table 10. Alternate function input/output

| Port name | Digital alternate function number | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | AFIO0 | AFIO1 | AFIO2 | AFIO3 | AFIO4 | AFIO5 | AFOI6 | AFIO7 | AFIO8 | AFIO9 | AFIO11 | AFIO12 | AFIO13 | AFIO14 | AFIO15 |
| | Alternate function | | | | | | | | | | | | | | |
| | SYSTEM | TIM2 | TIM3/4 | TIM9/10/11 | I2C1/2 | SPI1/2 | N/A | USART 1/2/3 | N/A | N/A | LCD | N/A | N/A | RI | SYSTEM |
| BOOT0 | BOOT0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| NRST | NRST | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| PA0-WKUP1 | - | TIM2_CH1_ETR | - | - | - | - | - | USART2_CTS | - | - | - | - | - | TIMx_IC1 | EVENTOUT |
| PA1 | - | TIM2_CH2 | - | - | - | - | - | USART2_RTS | - | - | [SEG0] | - | - | TIMx_IC2 | EVENTOUT |
| PA2 | - | TIM2_CH3 | - | TIM9_CH1 | - | - | - | USART2_TX | - | - | [SEG1] | - | - | TIMx_IC3 | EVENTOUT |
| PA3 | - | TIM2_CH4 | - | TIM9_CH2 | - | - | - | USART2_RX | - | - | [SEG2] | - | - | TIMx_IC4 | EVENTOUT |
| PA4 | - | - | - | - | - | SPI1_NSS | - | USART2_CK | - | - | - | - | - | TIMx_IC1 | EVENTOUT |
| PA5 | - | TIM2_CH1_ETR | - | - | - | SPI1_SCK | - | - | - | - | - | - | - | TIMx_IC2 | EVENTOUT |
| PA6 | - | - | TIM3_CH1 | TIM10_CH1 | - | SPI1_MISO | - | - | - | - | [SEG3] | - | - | TIMx_IC3 | EVENTOUT |
| PA7 | - | - | TIM3_CH2 | TIM11_CH1 | - | SPI1_MOSI | - | - | - | - | [SEG4] | - | - | TIMx_IC4 | EVENTOUT |
| PA8 | MCO | - | - | - | - | - | - | USART1_CK | - | - | [COM0] | - | - | TIMx_IC1 | EVENTOUT |
| PA9 | - | - | - | - | - | - | - | USART1_TX | - | - | [COM1] | - | - | TIMx_IC2 | EVENTOUT |
| PA10 | - | - | - | - | - | - | - | USART1_RX | - | - | [COM2] | - | - | TIMx_IC3 | EVENTOUT |
| PA11 | - | - | - | - | - | SPI1_MISO | - | USART1_CTS | - | - | - | - | - | TIMx_IC4 | EVENTOUT |
| PA12 | - | - | - | - | - | SPI1_MOSI | - | USART1_RTS | - | - | - | - | - | TIMx_IC1 | EVENTOUT |
| PA13 | JTMS-SWDIO | - | - | - | - | - | - | - | - | - | - | - | - | TIMx_IC2 | EVENTOUT |
| PA14 | JTCK-SWCLK | - | - | - | - | - | - | - | - | - | - | - | - | TIMx_IC3 | EVENTOUT |
| PA15 | JTDI | TIM2_CH1_ETR | - | - | - | SPI1_NSS | - | - | - | - | SEG17 | - | - | TIMx_IC4 | EVENTOUT |
| PB0 | - | - | TIM3_CH3 | - | - | - | - | - | - | - | [SEG5] | - | - | - | EVENTOUT |
| PB1 | - | - | TIM3_CH4 | - | - | - | - | - | - | - | [SEG6] | - | - | - | EVENTOUT |
| PB2 | BOOT1 | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| PB3 | JTDO | TIM2_CH2 | - | - | - | SPI1_SCK | - | - | - | - | [SEG7] | - | - | - | EVENTOUT |

**Table 10. Alternate function input/output (continued)**

| Port name | Digital alternate function number | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | AFIO0 | AFIO1 | AFIO2 | AFIO3 | AFIO4 | AFIO5 | AFOI6 | AFIO7 | AFIO8 | AFIO9 | AFIO11 | AFIO12 | AFIO13 | AFIO14 | AFIO15 |
| | Alternate function | | | | | | | | | | | | | | |
| | SYSTEM | TIM2 | TIM3/4 | TIM9/10/11 | I2C1/2 | SPI1/2 | N/A | USART 1/2/3 | N/A | N/A | LCD | N/A | N/A | RI | SYSTEM |
| PB4 | NJTRST | - | TIM3_CH1 | - | - | SPI1_MISO | - | - | - | - | [SEG8] | - | - | - | EVENTOUT |
| PB5 | - | - | TIM3_CH2 | - | I2C1_ SMBA | SPI1_MOSI | - | - | - | - | [SEG9] | - | - | - | EVENTOUT |
| PB6 | - | - | TIM4_CH1 | - | I2C1_SCL | - | - | USART1_TX | - | - | - | - | - | - | EVENTOUT |
| PB7 | - | - | TIM4_CH2 | - | I2C1_SDA | - | - | USART1_RX | - | - | - | - | - | - | EVENTOUT |
| PB8 | - | - | TIM4_CH3 | TIM10_CH1* | I2C1_SCL | - | - | - | - | - | SEG16 | - | - | - | EVENTOUT |
| PB9 | - | - | TIM4_CH4 | TIM11_CH1* | I2C1_SDA | - | - | - | - | - | [COM3] | - | - | - | EVENTOUT |
| PB10 | - | TIM2_CH3 | - | - | I2C2_SCL | - | - | USART3_TX | - | - | SEG10 | - | - | - | EVENTOUT |
| PB11 | - | TIM2_CH4 | - | - | I2C2_SDA | - | - | USART3_RX | - | - | SEG11 | - | - | - | EVENTOUT |
| PB12 | - | - | - | TIM10_CH1 | I2C2_ SMBA | SPI2_NSS | - | USART3_CK | - | - | SEG12 | - | - | - | EVENTOUT |
| PB13 | - | - | - | TIM9_CH1 | - | SPI2_SCK | - | USART3_CTS | - | - | SEG13 | - | - | - | EVENTOUT |
| PB14 | - | - | - | TIM9_CH2 | - | SPI2_MISO | - | USART3_RTS | - | - | SEG14 | - | - | - | EVENTOUT |
| PB15 | - | - | - | TIM11_CH1 | - | SPI2_MOSI | - | - | - | - | SEG15 | - | - | - | EVENTOUT |
| PC0 | - | - | - | - | - | - | - | - | - | - | SEG18 | - | - | TIMx_IC1 | EVENTOUT |
| PC1 | - | - | - | - | - | - | - | - | - | - | SEG19 | - | - | TIMx_IC2 | EVENTOUT |
| PC2 | - | - | - | - | - | - | - | - | - | - | SEG20 | - | - | TIMx_IC3 | EVENTOUT |
| PC3 | - | - | - | - | - | - | - | - | - | - | SEG21 | - | - | TIMx_IC4 | EVENTOUT |
| PC4 | - | - | - | - | - | - | - | - | - | - | SEG22 | - | - | TIMx_IC1 | EVENTOUT |
| PC5 | - | - | - | - | - | - | - | - | - | - | SEG23 | - | - | TIMx_IC2 | EVENTOUT |
| PC6 | - | - | TIM3_CH1 | - | - | - | - | - | - | - | SEG24 | - | - | TIMx_IC3 | EVENTOUT |
| PC7 | - | - | TIM3_CH2 | - | - | - | - | - | - | - | SEG25 | - | - | TIMx_IC4 | EVENTOUT |
| PC8 | - | - | TIM3_CH3 | - | - | - | - | - | - | - | SEG26 | - | - | TIMx_IC1 | EVENTOUT |
| PC9 | - | - | TIM3_CH4 | - | - | - | - | - | - | - | SEG27 | - | - | TIMx_IC2 | EVENTOUT |

**Table 10. Alternate function input/output (continued)**

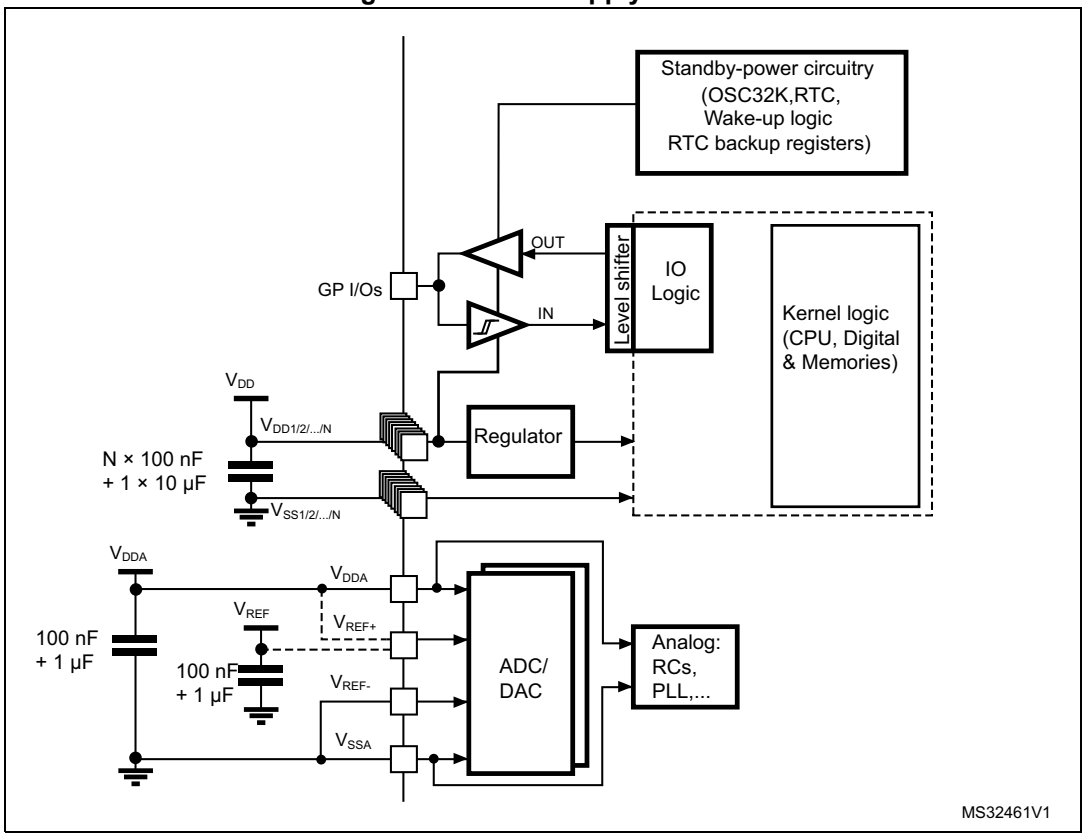
| Port name | Digital alternate function number | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | AFIO0 | AFIO1 | AFIO2 | AFIO3 | AFIO4 | AFIO5 | AFOI6 | AFIO7 | AFIO8 | AFIO9 | AFIO11 | AFIO12 | AFIO13 | AFIO14 | AFIO15 |
| | Alternate function | | | | | | | | | | | | | | |
| | SYSTEM | TIM2 | TIM3/4 | TIM9/10/11 | I2C1/2 | SPI1/2 | N/A | USART 1/2/3 | N/A | N/A | LCD | N/A | N/A | RI | SYSTEM |
| PD10 | - | - | - | - | - | - | - | USART3_CK | - | - | - | - | - | TIMx_IC3 | EVENTOUT |
| PD11 | - | - | - | - | - | - | - | USART3_CTS | - | - | - | - | - | TIMx_IC4 | EVENTOUT |
| PD12 | - | - | TIM4_CH1 | - | - | - | - | USART3_RTS | - | - | - | - | - | TIMx_IC1 | EVENTOUT |
| PD13 | - | - | TIM4_CH2 | - | - | - | - | - | - | - | - | - | - | TIMx_IC2 | EVENTOUT |
| PD14 | - | - | TIM4_CH3 | - | - | - | - | - | - | - | - | - | - | TIMx_IC3 | EVENTOUT |
| PD15 | - | - | TIM4_CH4 | - | - | - | - | - | - | - | - | - | - | TIMx_IC4 | EVENTOUT |
| PE0 | - | - | TIM4_ETR | TIM10_CH1 | - | - | - | - | - | - | - | - | - | TIMx_IC1 | EVENTOUT |
| PE1 | - | - | | TIM11_CH1 | - | - | - | - | - | - | - | - | - | TIMx_IC2 | EVENTOUT |
| PE2 | TRACECK | - | TIM3_ETR | - | - | - | - | - | - | - | - | - | - | TIMx_IC3 | EVENTOUT |
| PE3 | TRACED0 | - | TIM3_CH1 | - | - | - | - | - | - | - | - | - | - | TIMx_IC4 | EVENTOUT |
| PE4 | TRACED1 | - | TIM3_CH2 | - | - | - | - | - | - | - | - | - | - | TIMx_IC1 | EVENTOUT |
| PE5 | TRACED2 | - | - | TIM9_CH1* | - | - | - | - | - | - | - | - | - | TIMx_IC2 | EVENTOUT |
| PE6 | TRACED3 | - | - | TIM9_CH2* | - | - | - | - | - | - | - | - | - | TIMx_IC3 | EVENTOUT |
| PE7 | - | - | - | - | - | - | - | - | - | - | - | - | - | TIMx_IC4 | EVENTOUT |
| PE8 | - | - | - | - | - | - | - | - | - | - | - | - | - | TIMx_IC1 | EVENTOUT |
| PE9 | - | TIM2_CH1_ETR | - | - | - | - | - | - | - | - | - | - | - | TIMx_IC2 | EVENTOUT |
| PE10 | - | TIM2_CH2 | - | - | - | - | - | - | - | - | - | - | - | TIMx_IC3 | EVENTOUT |
| PE11 | - | TIM2_CH3 | - | - | - | - | - | - | - | - | - | - | - | TIMx_IC4 | EVENTOUT |
| PE12 | - | TIM2_CH4 | - | - | - | SPI1_NSS | - | - | - | - | - | - | - | TIMx_IC1 | EVENTOUT |
| PE13 | - | - | - | - | - | SPI1_SCK | - | - | - | - | - | - | - | TIMx_IC2 | EVENTOUT |
| PE14 | - | - | - | - | - | SPI1_MISO | - | - | - | - | - | - | - | TIMx_IC3 | EVENTOUT |
| PE15 | - | - | - | - | - | SPI1_MOSI | - | - | - | - | - | - | - | TIMx_IC4 | EVENTOUT |
| PH0-OSC_IN | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |

**Table 10. Alternate function input/output (continued)**

| Port name | Digital alternate function number | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | AFIO0 | AFIO1 | AFIO2 | AFIO3 | AFIO4 | AFIO5 | AFOI6 | AFIO7 | AFIO8 | AFIO9 | AFIO11 | AFIO12 | AFIO13 | AFIO14 | AFIO15 |
| | Alternate function | | | | | | | | | | | | | | |
| | SYSTEM | TIM2 | TIM3/4 | TIM9/10/11 | I2C1/2 | SPI1/2 | N/A | USART 1/2/3 | N/A | N/A | LCD | N/A | N/A | RI | SYSTEM |
| PH1-OSC_OUT | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| PH2 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |

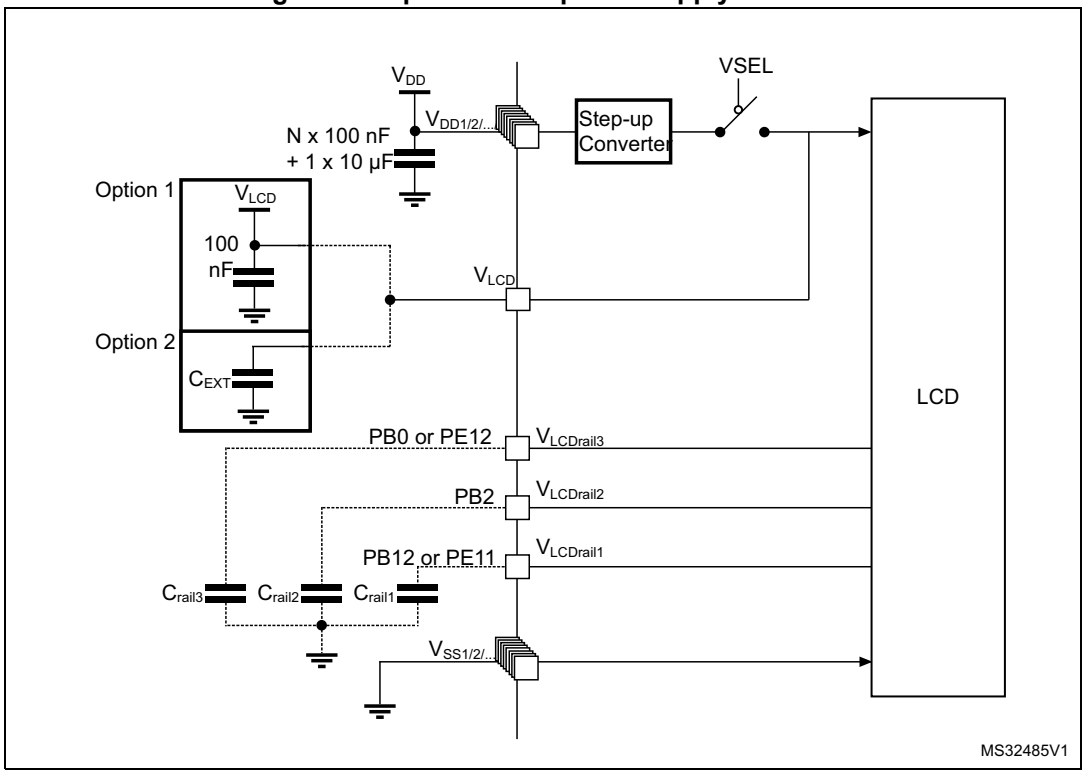
### 6.1.6 Power supply scheme

**Figure 12. Power supply scheme**



### 6.1.7 Optional LCD power supply scheme

**Figure 13. Optional LCD power supply scheme**




1. Option 1: LCD power supply is provided by a dedicated VLCD supply source, VSEL switch is open.
2. Option 2: LCD power supply is provided by the internal step-up converter, VSEL switch is closed, an external capacitance is needed for correct behavior of this converter.

### 6.1.8 Current consumption measurement

**Figure 14. Current consumption measurement scheme**

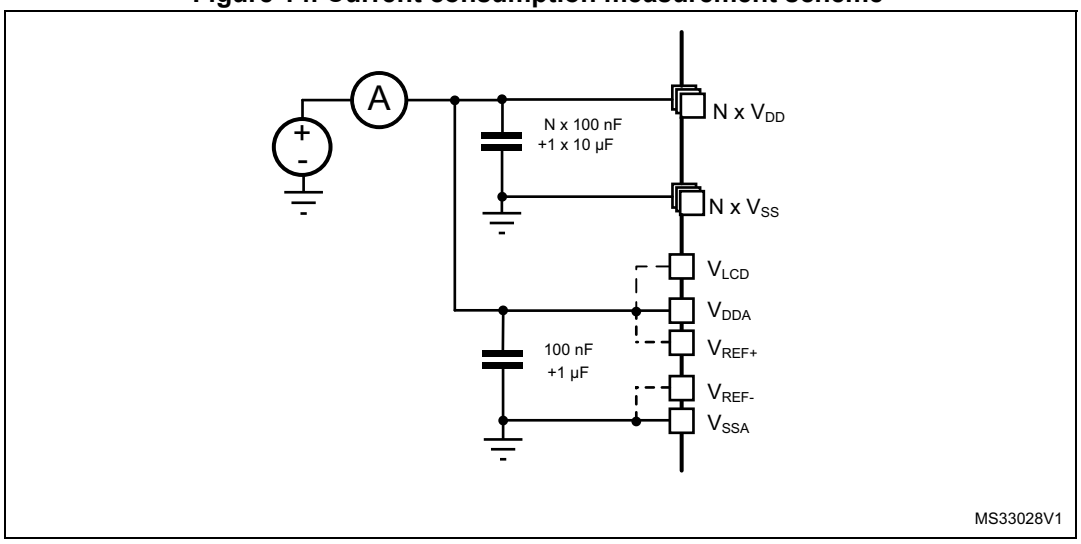


**Table 24. Typical and maximum current consumptions in Standby mode**

| Symbol | Parameter | Conditions | | Typ(1) | Max (1)(2) | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ (Standby with RTC) | Supply current in Standby mode with RTC enabled | RTC clocked by LSI (no independent watchdog) | $T_A$ = -40 °C to 25 °C $V_{DD}$ = 1.8 V | 0.865 | - | µA |
| | | | $T_A$ = -40 °C to 25 °C | 1.11 | 1.9 | |
| | | | $T_A$ = 55 °C | 1.15 | 2.2 | |
| | | | $T_A$= 85 °C | 1.35 | 4 | |
| | | | $T_A$ = 105 °C | 1.93 | 8.3(3) | |
| | | RTC clocked by LSE (no independent watchdog)(4) | $T_A$ = -40 °C to 25 °C $V_{DD}$ = 1.8 V | 0.97 | - | |
| | | | $T_A$ = -40 °C to 25 °C | 1.28 | - | |
| | | | $T_A$ = 55 °C | 1.4 | - | |
| | | | $T_A$= 85 °C | 1.7 | - | |
| | | | $T_A$ = 105 °C | 2.34 | - | |
| $I_{DD}$ (Standby) | Supply current in Standby mode with RTC disabled | Independent watchdog and LSI enabled | $T_A$ = -40 °C to 25 °C | 1.0 | 1.7 | |
| | | Independent watchdog and LSI OFF | $T_A$ = -40 °C to 25 °C | 0.277 | 0.6 | |
| | | | $T_A$ = 55 °C | 0.31 | 0.9 | |
| | | | $T_A$ = 85 °C | 0.52 | 2.75 | |
| | | | $T_A$ = 105 °C | 1.09 | 7(3) | |
| $I_{DD}$ (WU from Standby) | RMS supply current during wakeup time when exiting from Standby mode | - | $V_{DD}$ = 3.0 V $T_A$ = -40 °C to 25 °C | 1 | - | mA |

1. The typical values are given for $V_{DD}$ = 3.0 V and max values are given for $V_{DD}$ = 3.6 V, unless otherwise specified.
2. Guaranteed by characterization results, unless otherwise specified.
3. Guaranteed by test in production.
4. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8pF loading capacitors.

### On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on

**Table 29. HSE oscillator characteristics(1)(2) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| C | Recommended load capacitance versus equivalent serial resistance of the crystal ($R_S$)(3) | $R_S$ = 30 Ω | - | 20 | - | pF |
| $I_{HSE}$ | HSE driving current | $V_{DD}$= 3.3 V, $V_{IN}$ = $V_{SS}$ with 30 pF load | - | - | 3 | mA |
| $I_{DD(HSE)}$ | HSE oscillator power consumption | C = 20 pF $f_{OSC}$ = 16 MHz | - | - | 2.5 (startup) 0.7 (stabilized) | mA |
| | | C = 10 pF $f_{OSC}$ = 16 MHz | - | - | 2.5 (startup) 0.46 (stabilized) | |
| $g_m$ | Oscillator transconductance | Startup | 3.5 | - | - | mA /V |
| $t_{SU(HSE)}$ (4) | Startup time | $V_{DD}$ is stabilized | - | 1 | - | ms |

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For $C_{L1}$ and $C_{L2}$, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 17*). $C_{L1}$ and $C_{L2}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of $C_{L1}$ and $C_{L2}$. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing $C_{L1}$ and $C_{L2}$. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

### Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 19* and *Table 45*, respectively.

Unless otherwise specified, the parameters given in *Table 45* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 14*.

**Table 45. I/O AC characteristics(1)**

| OSPEEDRx [1:0] bit value(1) | Symbol | Parameter | Conditions | Min | Max(2) | Unit |
|---|---|---|---|---|---|---|
| 00 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 400 | kHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 1.65 V to 2.7 V | - | 400 | |
| | $t_{f(IO)out}$ $t_{r(IO)out}$ | Output rise and fall time | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 625 | ns |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 1.65 V to 2.7 V | - | 625 | |
| 01 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 2 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 1.65 V to 2.7 V | - | 1 | |
| | $t_{f(IO)out}$ $t_{r(IO)out}$ | Output rise and fall time | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 125 | ns |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 1.65 V to 2.7 V | - | 250 | |
| 10 | $F_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 10 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 1.65 V to 2.7 V | - | 2 | |
| | $t_{f(IO)out}$ $t_{r(IO)out}$ | Output rise and fall time | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 25 | ns |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 1.65 V to 2.7 V | - | 125 | |
| 11 | $F_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 50 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 1.65 V to 2.7 V | - | 8 | |
| | $t_{f(IO)out}$ $t_{r(IO)out}$ | Output rise and fall time | $C_L$ = 30 pF, $V_{DD}$ = 2.7 V to 3.6 V | - | 5 | ns |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 1.65 V to 2.7 V | - | 30 | |
| - | $t_{EXTIpw}$ | Pulse width of external signals detected by the EXTI controller | - | 8 | - | |

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. The maximum frequency is defined in *Figure 19*.

### 6.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 55* are guaranteed by design.

**Table 54. ADC clock frequency**

| Symbol | Parameter | Conditions | | | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{ADC}$ | ADC clock frequency | Voltage Range 1 & 2 | 2.4 V ≤$V_{DDA}$ ≤3.6 V | $V_{REF+}$ = $V_{DDA}$ | 0.480 | 16 | MHz |
| | | | | $V_{REF+}$ < $V_{DDA}$ $V_{REF+}$ > 2.4 V | | 8 | |
| | | | | $V_{REF+}$ < $V_{DDA}$ $V_{REF+}$ ≤2.4 V | | 4 | |
| | | | 1.8 V ≤$V_{DDA}$ ≤2.4 V | $V_{REF+}$ = $V_{DDA}$ | | 8 | |
| | | | | $V_{REF+}$ < $V_{DDA}$ | | 4 | |
| | | Voltage Range 3 | | | | 4 | |

**Table 55. ADC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Power supply | - | 1.8 | - | 3.6 | V |
| $V_{REF+}$ | Positive reference voltage | 2.4 V ≤$V_{DDA}$ ≤3.6 V $V_{REF+}$ must be below or equal to $V_{DDA}$ | 1.8(1) | - | $V_{DDA}$ | V |
| $V_{REF-}$ | Negative reference voltage | - | - | $V_{SSA}$ | - | V |
| $I_{VDDA}$ | Current on the $V_{DDA}$ input pin | - | - | 1000 | 1450 | µA |
| $I_{VREF}$(2) | Current on the $V_{REF}$ input pin | Peak | - | 400 | 700 | µA |
| | | Average | - | | 450 | µA |
| $V_{AIN}$ | Conversion voltage range(3) | - | 0(4) | - | $V_{REF+}$ | V |
| $f_S$ | 12-bit sampling rate | Direct channels | - | - | 1 | Msps |
| | | Multiplexed channels | - | - | 0.76 | |
| | 10-bit sampling rate | Direct channels | - | - | 1.07 | Msps |
| | | Multiplexed channels | - | - | 0.8 | |
| | 8-bit sampling rate | Direct channels | - | - | 1.23 | Msps |
| | | Multiplexed channels | - | - | 0.89 | |
| | 6-bit sampling rate | Direct channels | - | - | 1.45 | Msps |
| | | Multiplexed channels | - | - | 1 | |

**Table 55. ADC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_S$ | Sampling time(5) | Direct channels 2.4 V ≤$V_{DDA}$ ≤3.6 V | 0.25 | - | - | µs |
| | | Multiplexed channels 2.4 V ≤$V_{DDA}$ ≤3.6 V | 0.56 | - | - | |
| | | Direct channels 1.8 V ≤$V_{DDA}$ ≤2.4 V | 0.56 | - | - | |
| | | Multiplexed channels 1.8 V ≤$V_{DDA}$ ≤2.4 V | 1 | - | - | |
| | | - | 4 | - | 384 | $1/f_{ADC}$ |
| $t_{CONV}$ | Total conversion time (including sampling time) | $f_{ADC}$ = 16 MHz | 1 | - | 24.75 | µs |
| | | - | 4 to 384 (sampling phase) +12 (successive approximation) | | | $1/f_{ADC}$ |
| $C_{ADC}$ | Internal sample and hold capacitor | Direct channels | - | 16 | - | pF |
| | | Multiplexed channels | - | | - | |
| $f_{TRIG}$ | External trigger frequency Regular sequencer | 12-bit conversions | - | - | Tconv+1 | $1/f_{ADC}$ |
| | | 6/8/10-bit conversions | - | - | Tconv | $1/f_{ADC}$ |
| $f_{TRIG}$ | External trigger frequency Injected sequencer | 12-bit conversions | - | - | Tconv+2 | $1/f_{ADC}$ |
| | | 6/8/10-bit conversions | - | - | Tconv+1 | $1/f_{ADC}$ |
| $R_{AIN}$ | Signal source impedance(5) | - | - | - | 50 | kΩ |
| $t_{lat}$ | Injection trigger conversion latency | $f_{ADC}$ = 16 MHz | 219 | - | 281 | ns |
| | | - | 3.5 | - | 4.5 | $1/f_{ADC}$ |
| $t_{latr}$ | Regular trigger conversion latency | $f_{ADC}$ = 16 MHz | 156 | - | 219 | ns |
| | | - | 2.5 | - | 3.5 | $1/f_{ADC}$ |
| $t_{STAB}$ | Power-up time | - | - | - | 3.5 | µs |

1. The $V_{REF+}$ input can be grounded if neither the ADC nor the DAC are used (this allows to shut down an external voltage reference).
2. The current consumption through $V_{REF}$ is composed of two parameters:

   - one constant (max 300 µA)

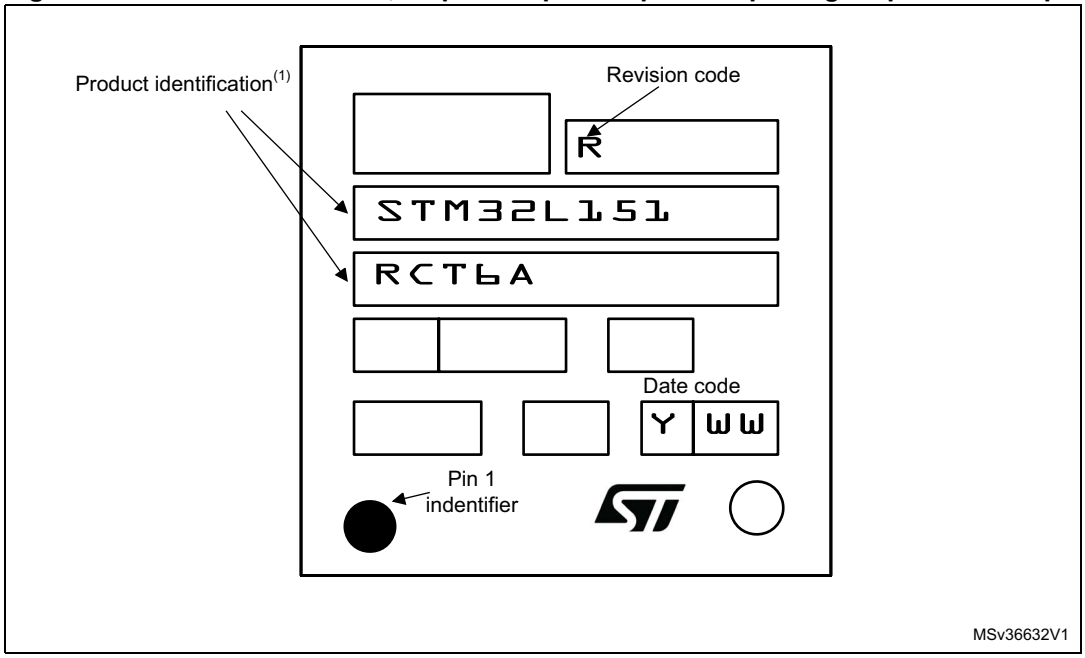
   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses.

   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
3. $V_{REF+}$ can be internally connected to $V_{DDA}$ and $V_{REF-}$ can be internally connected to $V_{SSA}$, depending on the package. Refer to *Section 4: Pin descriptions* for further details.
4. $V_{SSA}$ or $V_{REF-}$ must be tied to ground.
5. See *Table 57: Maximum source impedance RAIN max* for $R_{AIN}$ limitations

### LQFP64 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

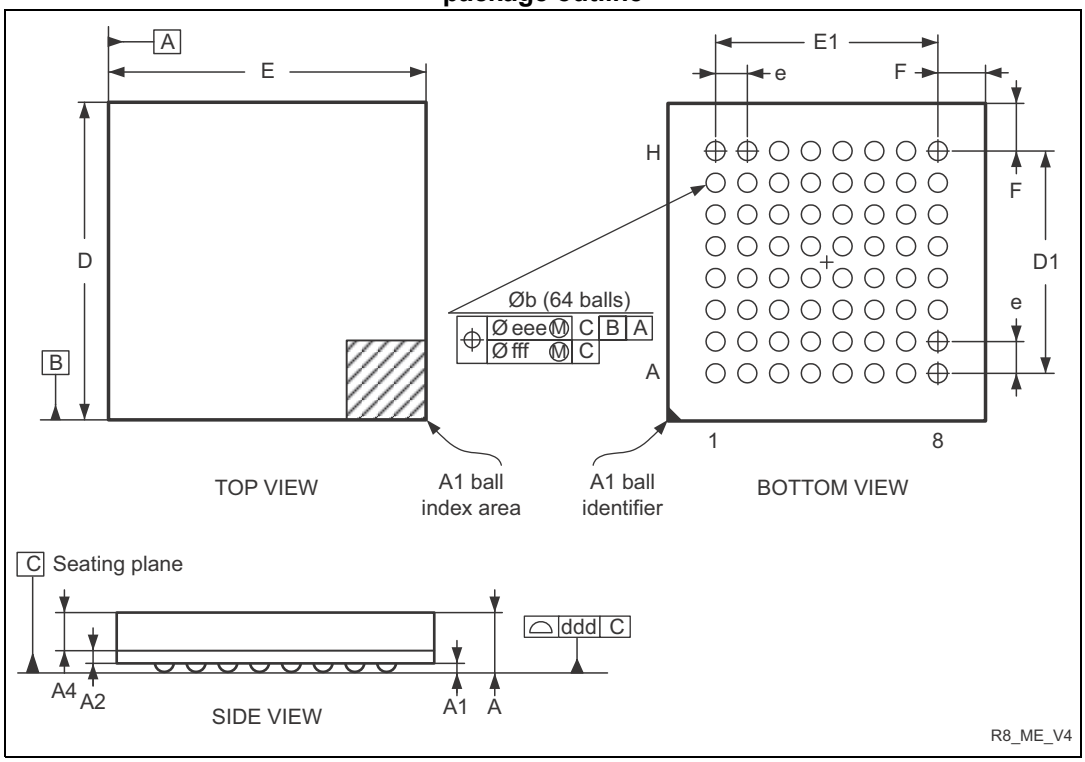
**Figure 35. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package top view example**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

## 7.6 TFBGA64 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package information

**Figure 45. TFBGA64 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package outline**




1. Drawing is not to scale.

**Table 70. TFBGA64 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.200 | - | - | 0.0472 |
| A1 | 0.150 | - | - | 0.0059 | - | - |
| A2 | - | 0.200 | - | - | 0.0079 | - |
| A4 | - | - | 0.600 | - | - | 0.0236 |
| b | 0.250 | 0.300 | 0.350 | 0.0098 | 0.0118 | 0.0138 |
| D | 4.850 | 5.000 | 5.150 | 0.1909 | 0.1969 | 0.2028 |
| D1 | - | 3.500 | - | - | 0.1378 | - |
| E | 4.850 | 5.000 | 5.150 | 0.1909 | 0.1969 | 0.2028 |
| E1 | - | 3.500 | - | - | 0.1378 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| F | - | 0.750 | - | - | 0.0295 | - |

# 9 Revision history

Table 74. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 04-Feb-2014 | 1 | Initial release. |
| 12-Mar-2014 | 2 | Updated *Section 3.5: Low-power real-time clock and backup registers*, *Section 6.1.2: Typical values* and *Section 6.3.4: Supply current characteristics*.<br>Updated *General PCB design guidelines*.<br>Updated *Table 5: Working mode-dependent functionalities (from Run/active down to standby)*, *Table 14: General operating conditions*, *Table 21: Current consumption in Low-power run mode*, *Table 22: Current consumption in Low-power sleep mode*, *Table 23: Typical and maximum current consumptions in Stop mode*, *Table 24: Typical and maximum current consumptions in Standby mode*, *Table 25: Peripheral current consumption*, *Table 42: I/O current injection susceptibility*, *Table 66: I/O static characteristics* and *Table 46: NRST pin characteristics*.<br>Updated *Figure 14: Current consumption measurement scheme*. |
| 04-Feb-2015 | 3 | Updated DMIPS features in cover page and *Section 2: Description*.<br>Updated max temperature at 105°C instead of 85°C in the whole datasheet.<br>Updated current consumption in *Table 20: Current consumption in Sleep mode*.<br>Updated *Table 25: Peripheral current consumption* with new measured values.<br>Updated *Table 57: Maximum source impedance RAIN max* adding note 2.<br>Updated *Section 7: Package information* with new package device marking.<br>Updated *Figure 9: Memory map*. |