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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152v8t6a

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L151x6/8/B-A and STM32L152x6/8/B-A ultra-low-power ARM® Cortex®-M3 based microcontrollers product line.

The ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A microcontroller family includes devices in 3 different package types: from 48 to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A microcontroller family suitable for a wide range of applications:

- Medical and handheld equipment
- Application control and user interface
- PC peripherals, gaming, GPS and sport equipment
- Alarm systems, Wired and wireless sensors, Video intercom
- Utility metering

This STM32L151x6/8/B-A and STM32L152x6/8/B-A datasheet should be read in conjunction with the STM32L1xxxx reference manual (RM0038). The document "Getting started with STM32L1xxxx hardware development" AN3216 gives a hardware implementation overview.

Both documents are available from the STMicroelectronics website *www.st.com*.

For information on the ARM® Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the ARM website.

Figure 1 shows the general block diagram of the device family.

Caution: This datasheet does not apply to:

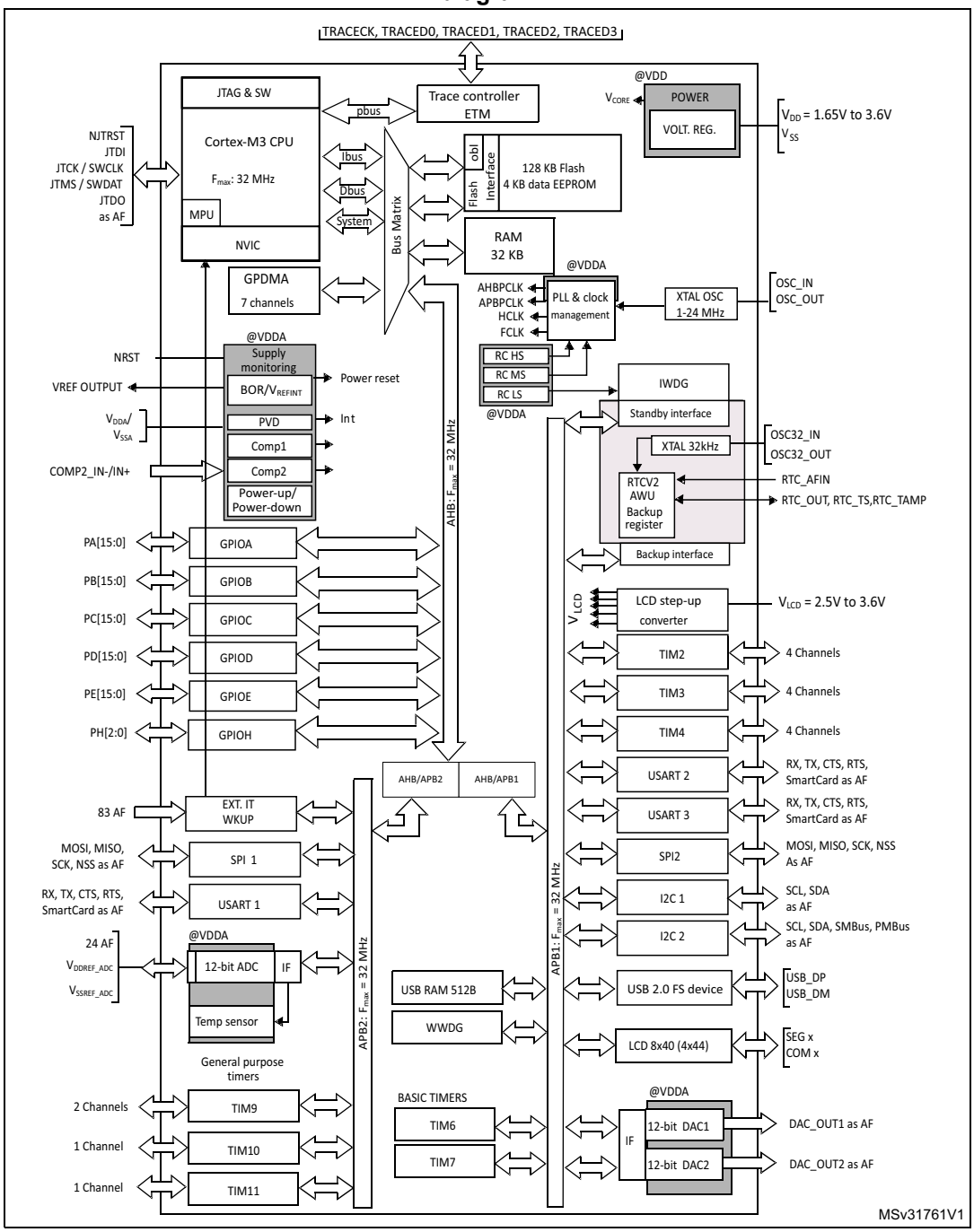
– STM32L15xx6/8/B

covered by a separate datasheet.

3 Functional overview

Figure 1 shows the block diagram.

Figure 1. Ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A block diagram



1. AF = alternate function on I/O port pin.

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A devices embed a nested vectored interrupt controller able to handle up to 45 maskable interrupt channels (not including the 16 interrupt lines of Cortex-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving*, higher-priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.3 Reset and supply management

3.3.1 Power supply schemes

- V_{DD} = 1.65 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

The device exists in two versions:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the V_{DD} threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the V_{DD} min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the power ramp-up should guarantee that 1.65 V is reached on V_{DD} at least 1 ms after it exits the POR area.

Figure 2. Clock tree

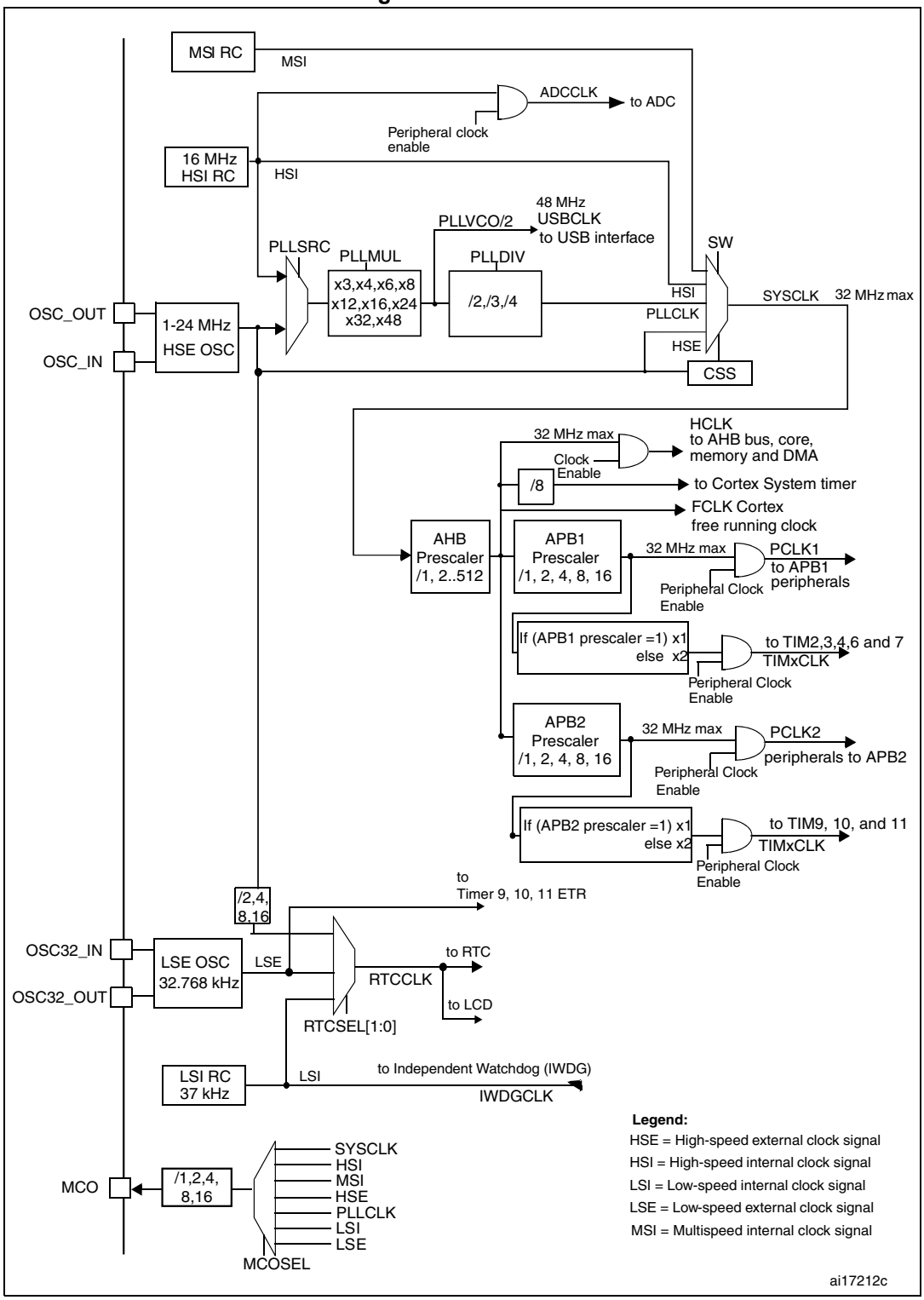


Table 7. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2, TIM3, TIM4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM9	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No
TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.15.1 General-purpose timers (TIM2, TIM3, TIM4, TIM9, TIM10 and TIM11)

There are six synchronizable general-purpose timers embedded in the STM32L151x6/8/B-A and STM32L152x6/8/B-A devices (see *Table 7* for differences).

TIM2, TIM3, TIM4

These timers are based on a 16-bit auto-reload up/down-counter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2, TIM3, TIM4 general-purpose timers can work together or with the TIM10, TIM11 and TIM9 general-purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4 all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

TIM10, TIM11 and TIM9

TIM10 and TIM11 are based on a 16-bit auto-reload upcounter. TIM9 is based on a 16-bit auto-reload up/down counter. They include a 16-bit prescaler. TIM10 and TIM11 feature one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4 full-featured general-purpose timers.

They can also be used as simple time bases and be clocked by the LSE clock source (32.768 kHz) to provide time bases independent from the main CPU clock.

3.15.2 Basic timers (TIM6 and TIM7)

These timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit time bases.

3.15.3 SysTick timer

This timer is dedicated to the OS, but could also be used as a standard downcounter. It is based on a 24-bit down-counter with autoreload capability and a programmable clock source. It features a maskable system interrupt generation when the counter reaches 0.

3.15.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit down-counter and 8-bit prescaler. It is clocked from an independent 37 kHz internal RC and, as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

Table 9. STM32L151x6/8/B-A and STM32L152x6/8/B-A pin definitions (continued)

Pins					Pin name	Pin type(1)	I/O structure	Main function(2) (after reset)	Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48					Alternate functions	Additional functions
82	-	-	B9	-	PD1	I/O	FT	PD1	SPI2_SCK	-
83	54	B5	C8	-	PD2	I/O	FT	PD2	TIM3_ETR/LCD_SEG31 /LCD_SEG43/ LCD_COM7	-
84	-	-	B8	-	PD3	I/O	FT	PD3	USART2_CTS/ SPI2_MISO	-
85	-	-	B7	-	PD4	I/O	FT	PD4	USART2_RTS/ SPI2_MOSI	-
86	-	-	A6	-	PD5	I/O	FT	PD5	USART2_TX	-
87	-	-	B6	-	PD6	I/O	FT	PD6	USART2_RX	-
88	-	-	A5	-	PD7	I/O	FT	PD7	USART2_CK/ TIM9_CH2	-
89	55	A5	A8	39	PB3	I/O	FT	JTDO	TIM2_CH2/PB3/ SPI1_SCK/ LCD_SEG7/JTDO	COMP2_INM
90	56	A4	A7	40	PB4	I/O	FT	NJTRST	TIM3_CH1/PB4/ SPI1_MISO/LCD_SEG8 /NJTRST	COMP2_INP
91	57	C4	C5	41	PB5	I/O	FT	PB5	I2C1_SMBA/TIM3_CH2/ SPI1_MOSI/LCD_SEG9	COMP2_INP
92	58	D3	B5	42	PB6	I/O	FT	PB6	I2C1_SCL/TIM4_CH1/ USART1_TX	-
93	59	C3	B4	43	PB7	I/O	FT	PB7	I2C1_SDA/TIM4_CH2/ USART1_RX	PVD_IN
94	60	B4	A4	44	BOOT0	I	B	BOOT0	-	-
95	61	B3	A3	45	PB8	I/O	FT	PB8	TIM4_CH3/I2C1_SCL/ LCD_SEG16/ TIM10_CH1	-
96	62	A3	B3	46	PB9	I/O	FT	PB9	TIM4_CH4/I2C1_SDA/ LCD_COM3/ TIM11_CH1	-
97	-	-	C3	-	PE0	I/O	FT	PE0	TIM4_ETR/LCD_SEG36 / TIM10_CH1	-

Table 9. STM32L151x6/8/B-A and STM32L152x6/8/B-A pin definitions (continued)

Pins					Pin name	Pin type[1]	I/O structure	Main function[2] (after reset)	Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48					Alternate functions	Additional functions
98	-	-	A2	-	PE1	I/O	FT	PE1	LCD_SEG37/ TIM11_CH1	-
99	63	D4	D3	47	V_{SS_3}	S	-	V_{SS_3}	-	-
100	64	E4	C4	48	V_{DD_3}	S	-	V_{DD_3}	-	-

1. I = input, O = output, S = supply.
2. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripheral that is included. For example, if a device has only one SPI and two USARTs, they will be called SPI1 and USART1 & USART2, respectively. Refer to *Table 2 on page 11*.
3. Applicable to STM32L152xxxxA devices only. In STM32L151xxxxA devices, this pin should be connected to V_{DD}.
4. The PC14 and PC15 I/Os are only configured as OSC32_IN/OSC32_OUT when the LSE oscillator is on (by setting the LSEON bit in the RCC_CSR register). The LSE oscillator pins OSC32_IN/OSC32_OUT can be used as general-purpose PC14/PC15 I/Os, respectively, when the LSE oscillator is off (after reset, the LSE oscillator is off). The LSE has priority over the GPIO function. For more details, refer to Using the OSC32_IN/OSC32_OUT pins as GPIO PC14/PC15 port pins section in the STM32L1xxxx reference manual (RM0038).
5. The PH0 and PH1 I/Os are only configured as OSC_IN/OSC_OUT when the HSE oscillator is on (by setting the HSEON bit in the RCC_CR register). The HSE oscillator pins OSC_IN/OSC_OUT can be used as general-purpose PH0/PH1 I/Os, respectively, when the HSE oscillator is off (after reset, the HSE oscillator is off). The HSE has priority over the GPIO function.
6. Unlike in the LQFP64 package, there is no PC3 in the TFBGA64 package. The V_{REF+} functionality is provided instead.

Table 18. Current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Run from Flash)	Supply current in Run mode, code executed from Flash	$f_{HSE} = f_{HCLK}$ up to 16 MHz, included $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	215	285	µA
				2 MHz	400	490	
				4 MHz	725	1000	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	0.915	1.3	mA
				8 MHz	1.75	2.15	
				16 MHz	3.4	4	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	2.1	2.9	
				16 MHz	4.2	5.2	
				32 MHz	8.25	9.6	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	3.5	4.4	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	8.2	10.2	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	65 kHz	0.041	0.085	
		MSI clock, 524 kHz		524 kHz	0.125	0.180	
		MSI clock, 4.2 MHz		4.2 MHz	0.775	0.935	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 19. Current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Run from RAM)	Supply current in Run mode, code executed from RAM, Flash switched off	$f_{HSE} = f_{HCLK}$ up to 16 MHz, included $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	185	255	µA
				2 MHz	345	435	
				4 MHz	645	930	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	0.755	1.5	mA
				8 MHz	1.5	2.2	
				16 MHz	3.0	3.6	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	1.8	2.9	
				16 MHz	3.6	4.3	
				32 MHz	7.15	8.5	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	2.95	3.7	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	7.15	8.7	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	65 kHz	39	115	µA
		MSI clock, 524 kHz		524 kHz	110	205	
		MSI clock, 4.2 MHz		4.2 MHz	690	870	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 20. Current consumption in Sleep mode

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Sleep)	Supply current in Sleep mode, Flash OFF	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	50	155	µA
				2 MHz	78.5	235	
				4 MHz	140	370(3)	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	165	375	
				8 MHz	310	530	
				16 MHz	590	1000	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	350	615	
				16 MHz	680	1200	
				32 MHz	1600	2350	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	640	970	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	1600	2350	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	65 kHz	19	60	
		MSI clock, 524 kHz		524 kHz	33	90	
		MSI clock, 4.2 MHz		4.2 MHz	145	210	
	Supply current in Sleep mode, Flash ON	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	60.5	145	µA
				2 MHz	89.5	225	
				4 MHz	150	360	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	180	370	
				8 MHz	320	490	
				16 MHz	605	895	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	380	565	
				16 MHz	695	1070	
				32 MHz	1600	2200	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	650	970	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	1600	2320	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2V VOS[1:0] = 11	65 kHz	29.5	65	
		MSI clock, 524 kHz		524 kHz	44	80	
		MSI clock, 4.2 MHz		4.2 MHz	155	220	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register)
3. Guaranteed by test in production.

Table 24. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions		Typ(1)	Max (1)(2)	Unit
I_{DD} (Standby with RTC)	Supply current in Standby mode with RTC enabled	RTC clocked by LSI (no independent watchdog)	T_A = -40 °C to 25 °C V_{DD} = 1.8 V	0.865	-	µA
			T_A = -40 °C to 25 °C	1.11	1.9	
			T_A = 55 °C	1.15	2.2	
			T_A= 85 °C	1.35	4	
			T_A = 105 °C	1.93	8.3(3)	
		RTC clocked by LSE (no independent watchdog)(4)	T_A = -40 °C to 25 °C V_{DD} = 1.8 V	0.97	-	
			T_A = -40 °C to 25 °C	1.28	-	
			T_A = 55 °C	1.4	-	
			T_A= 85 °C	1.7	-	
			T_A = 105 °C	2.34	-	
I_{DD} (Standby)	Supply current in Standby mode with RTC disabled	Independent watchdog and LSI enabled	T_A = -40 °C to 25 °C	1.0	1.7	
		Independent watchdog and LSI OFF	T_A = -40 °C to 25 °C	0.277	0.6	
			T_A = 55 °C	0.31	0.9	
			T_A = 85 °C	0.52	2.75	
			T_A = 105 °C	1.09	7(3)	
I_{DD} (WU from Standby)	RMS supply current during wakeup time when exiting from Standby mode	-	V_{DD} = 3.0 V T_A = -40 °C to 25 °C	1	-	mA

1. The typical values are given for V_{DD} = 3.0 V and max values are given for V_{DD} = 3.6 V, unless otherwise specified.
2. Guaranteed by characterization results, unless otherwise specified.
3. Guaranteed by test in production.
4. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8pF loading capacitors.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on

Table 25. Peripheral current consumption(1)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}= 1.8 V VOS[1:0] = 01	Range 2, V_{CORE}= 1.5 V VOS[1:0] = 10	Range 3, V_{CORE}= 1.2 V VOS[1:0] = 11	Low-power sleep and run	
APB1	TIM2	11.3	9.0	7.3	9.0	µA/MHz (f_{HCLK})
	TIM3	11.4	9.1	7.1	9.1	
	TIM4	11.3	9.0	7.3	9.0	
	TIM6	3.9	3.1	2.5	3.1	
	TIM7	4.2	3.3	2.6	3.3	
	LCD	4.7	3.6	2.9	3.6	
	WWDG	3.7	2.9	2.4	2.9	
	SPI2	5.9	4.8	3.9	4.8	
	USART2	8.1	6.6	5.1	6.6	
	USART3	7.9	6.4	5.0	6.4	
	I2C1	7.8	6.1	4.9	6.1	
	I2C2	7.2	5.7	4.6	5.7	
	USB	12.7	10.3	8.1	10.3	
	PWR	3.1	2.4	2.0	2.4	
	DAC	6.6	5.3	4.3	5.3	
	COMP	5.3	4.3	3.4	4.3	
APB2	SYSCFG & RI	2.2	1.9	1.6	1.9	µA/MHz (f_{HCLK})
	TIM9	9.1	7.3	5.9	7.3	
	TIM10	6.0	4.9	3.9	4.9	
	TIM11	5.8	4.6	3.8	4.6	
	ADC(2)	8.7	7.0	5.6	7.0	
	SPI1	4.4	3.4	2.8	3.4	
	USART1	8.1	6.5	5.2	6.5	
AHB	GPIOA	4.4	3.5	2.9	3.5	
	GPIOB	4.4	3.5	2.9	3.5	
	GPIOC	3.7	3.0	2.5	3.0	
	GPIOD	3.6	2.8	2.4	2.8	
	GPIOE	4.7	3.8	3.1	3.8	
	GPIOH	3.7	2.9	2.4	2.9	
	CRC	0.6	0.4	0.4	0.4	
	FLASH	12.2	10.2	7.8	-(3)	
	DMA1	12.4	10.1	8.2	10.1	
All enabled		160	135	103	124.8	

Table 26. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	f_{HCLK} = 32 MHz	0.4	-	µs
$t_{WUSLEEP\_LP}$	Wakeup from Low-power sleep mode f_{HCLK} = 262 kHz	f_{HCLK} = 262 kHz Flash enabled	46	-	
		f_{HCLK} = 262 kHz Flash switched OFF	46	-	
t_{WUSTOP}	Wakeup from Stop mode, regulator in Run mode	$f_{HCLK} = f_{MSI}$ = 4.2 MHz	8.2	-	
	Wakeup from Stop mode, regulator in low-power mode	$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage Range 1 and 2	7.7	8.9	
		$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage Range 3	8.2	13.1	
		$f_{HCLK} = f_{MSI}$ = 2.1 MHz	10.2	13.4	
		$f_{HCLK} = f_{MSI}$ = 1.05 MHz	16	20	
		$f_{HCLK} = f_{MSI}$ = 524 kHz	31	37	
		$f_{HCLK} = f_{MSI}$ = 262 kHz	57	66	
		$f_{HCLK} = f_{MSI}$ = 131 kHz	112	123	
		f_{HCLK} = MSI = 65 kHz	221	236	
$t_{WUSTDBY}$	Wakeup from Standby mode FWU bit = 1	f_{HCLK} = MSI = 2.1 MHz	58	104	
	Wakeup from Standby mode FWU bit = 0	f_{HCLK} = MSI = 2.1 MHz	2.6	3.25	ms

1. Guaranteed by characterization results, unless otherwise specified

6.3.9 Memory characteristics

The characteristics are given at T_A = -40 to 105 °C unless otherwise specified.

RAM memory

Table 35. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VRM	Data retention mode(1)	STOP mode (or RESET)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode).

Flash memory and data EEPROM

Table 36. Flash memory and data EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DD}	Operating voltage Read / Write / Erase	-	1.65	-	3.6	V
t_{prog}	Programming / erasing time for byte / word / double word / half-page	Erasing	-	3.28	3.94	ms
		Programming	-	3.28	3.94	
I_{DD}	Average current during whole program/erase operation	T_A = 25 °C, V_{DD} = 3.6 V	-	300	-	µA
	Maximum current (peak) during program/erase operation		-	1.5	2.5	mA

1. Guaranteed by design.

Table 37. Flash memory, data EEPROM endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
			Min(1)	Typ	Max	
NCYC(2)	Cycling (erase / write) Program memory	T_A = -40°C to 105 °C	10	-	-	kcycles
	Cycling (erase / write) EEPROM data memory		300	-	-	
t_{RET}(2)	Data retention (program memory) after 10 kcycles at T_A = 85 °C	TRET = +85 °C	30	-	-	years
	Data retention (EEPROM data memory) after 300 kcycles at T_A = 85 °C		30	-	-	
	Data retention (program memory) after 10 kcycles at T_A = 105 °C	TRET = +105 °C	10	-	-	
	Data retention (EEPROM data memory) after 300 kcycles at T_A = 105 °C		10	-	-	

1. Guaranteed by characterization results.
2. Characterization is done according to JEDEC JESD22-A117.

6.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 43* are derived from tests performed under conditions summarized in *Table 14*. All I/Os are CMOS and TTL compliant.

Table 43. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TC and FT I/O	-	-	0.3 V_{DD}(1)(2)	V
		BOOT0	-		0.14 V_{DD}(2)	
V_{IH}	Input high level voltage	TC I/O	0.45 V_{DD}+0.38(2)	-	-	
		FT I/O	0.39 V_{DD}+0.59(2)	-	-	
		BOOT0	0.15 V_{DD}+0.56(2)	-	-	
V_{hys}	I/O Schmitt trigger voltage hysteresis(2)	TC and FT I/O	-	10% V_{DD}(3)	-	
		BOOT0	-	0.01	-	
I_{lkg}	Input leakage current(4)	$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with LCD	-	-	±50	nA
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with analog switches	-	-	±50	
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with analog switches and LCD	-	-	±50	
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with USB	-	-	±250	
		$V_{SS} \le V_{IN} \le V_{DD}$ TC and FT I/O	-	-	±50	
		FT I/O $V_{DD} \le V_{IN} \le 5V$	-	-	±10	uA
R_{PU}	Weak pull-up equivalent resistor(5)(1)	$V_{IN} = V_{SS}$	30	45	60	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN} = V_{DD}$	30	45	60	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Guaranteed by test in production.
2. Guaranteed by design.
3. With a minimum of 200 mV.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

Table 55. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_S	Sampling time(5)	Direct channels 2.4 V ≤V_{DDA} ≤3.6 V	0.25	-	-	µs
		Multiplexed channels 2.4 V ≤V_{DDA} ≤3.6 V	0.56	-	-	
		Direct channels 1.8 V ≤V_{DDA} ≤2.4 V	0.56	-	-	
		Multiplexed channels 1.8 V ≤V_{DDA} ≤2.4 V	1	-	-	
		-	4	-	384	$1/f_{ADC}$
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 16 MHz	1	-	24.75	µs
		-	4 to 384 (sampling phase) +12 (successive approximation)			$1/f_{ADC}$
C_{ADC}	Internal sample and hold capacitor	Direct channels	-	16	-	pF
		Multiplexed channels	-		-	
f_{TRIG}	External trigger frequency Regular sequencer	12-bit conversions	-	-	Tconv+1	$1/f_{ADC}$
		6/8/10-bit conversions	-	-	Tconv	$1/f_{ADC}$
f_{TRIG}	External trigger frequency Injected sequencer	12-bit conversions	-	-	Tconv+2	$1/f_{ADC}$
		6/8/10-bit conversions	-	-	Tconv+1	$1/f_{ADC}$
R_{AIN}	Signal source impedance(5)	-	-	-	50	kΩ
t_{lat}	Injection trigger conversion latency	f_{ADC} = 16 MHz	219	-	281	ns
		-	3.5	-	4.5	$1/f_{ADC}$
t_{latr}	Regular trigger conversion latency	f_{ADC} = 16 MHz	156	-	219	ns
		-	2.5	-	3.5	$1/f_{ADC}$
t_{STAB}	Power-up time	-	-	-	3.5	µs

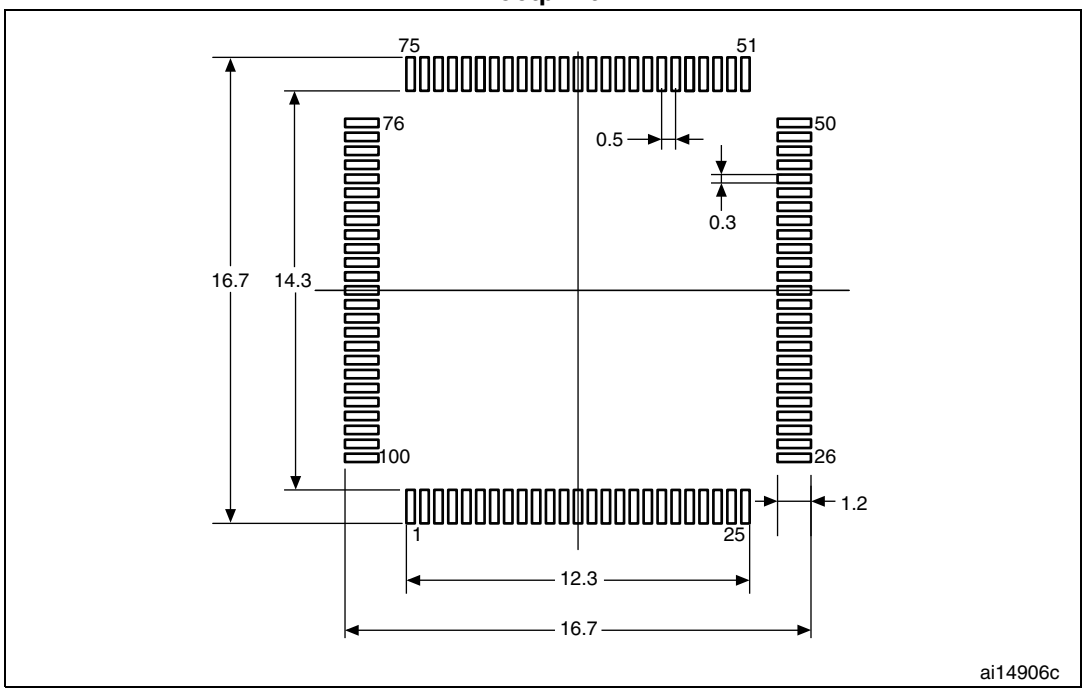
1. The V_{REF+} input can be grounded if neither the ADC nor the DAC are used (this allows to shut down an external voltage reference).
2. The current consumption through V_{REF} is composed of two parameters:

   - one constant (max 300 µA)

   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses.

   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 4: Pin descriptions* for further details.
4. V_{SSA} or V_{REF-} must be tied to ground.
5. See *Table 57: Maximum source impedance RAIN max* for R_{AIN} limitations

Figure 31. LQPF100 14 x 14 mm, 100-pin low-profile quad flat package recommended footprint

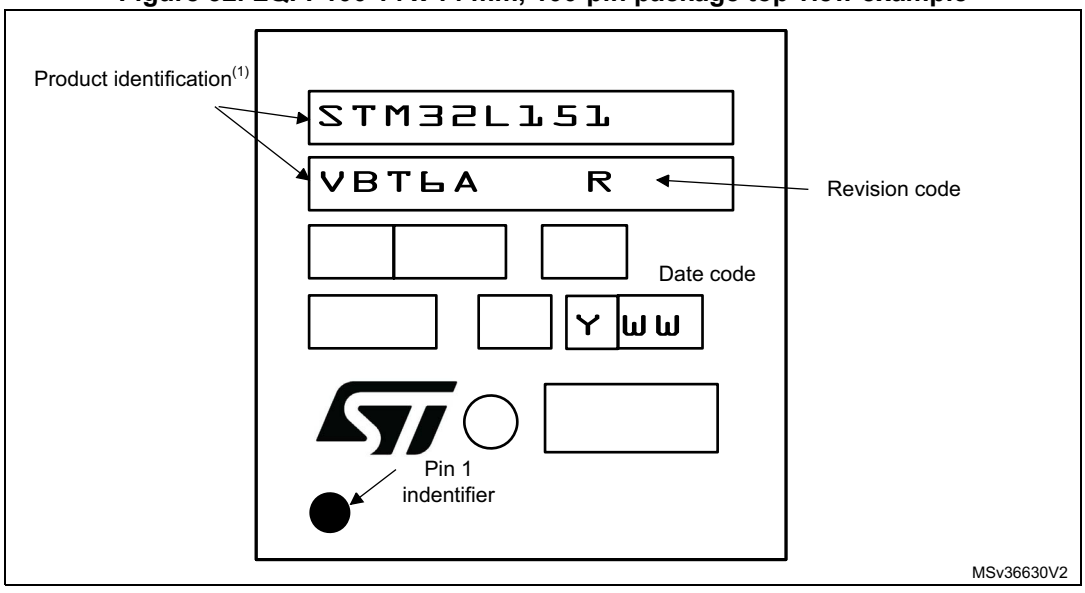


1. Dimensions are in millimeters.

LQFP100 device Marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 32. LQFP100 14 x 14 mm, 100-pin package top view example



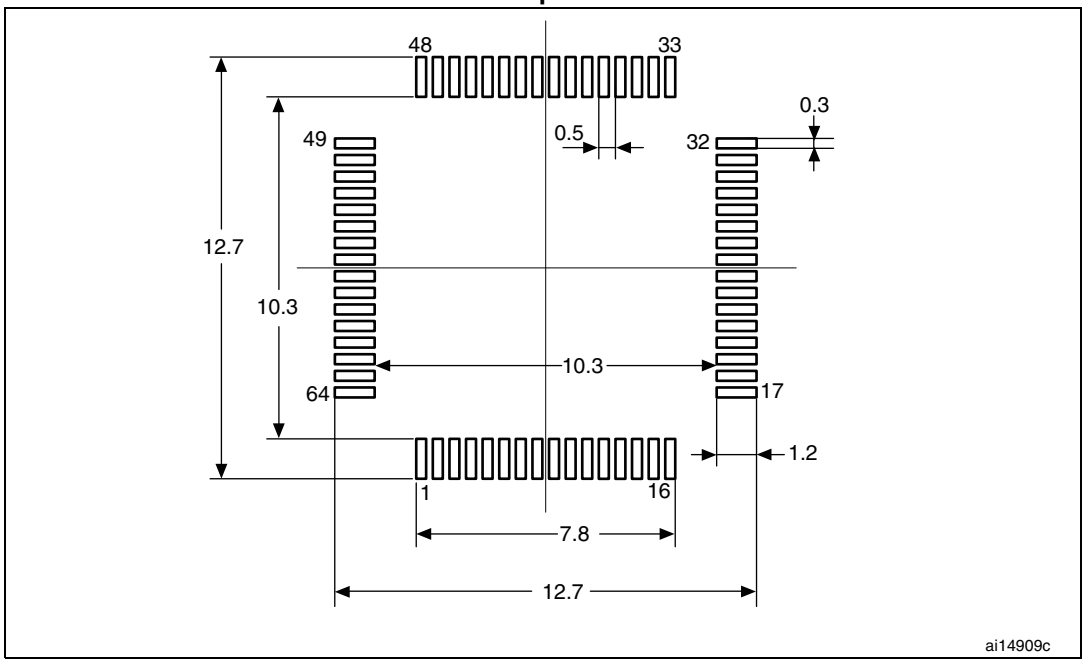
1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 65. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Typ	Min	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 34. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package recommended footprint

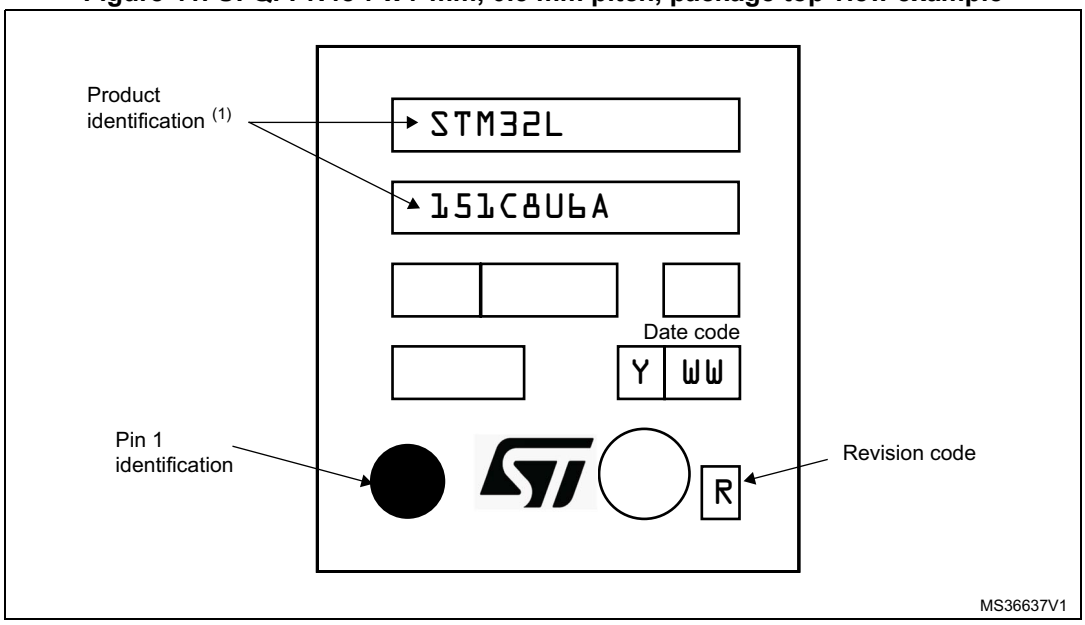


1. Dimensions are in millimeters.

UFQFPN48 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 41. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.