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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-MQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f874-04-pq

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Name	Bit#	Buffer	Function
RA0/AN0	bit0	TTL	Input/output or analog input.
RA1/AN1	bit1	TTL	Input/output or analog input.
RA2/AN2	bit2	TTL	Input/output or analog input.
RA3/AN3/VREF	bit3	TTL	Input/output or analog input or VREF.
RA4/T0CKI	bit4	ST	Input/output or external clock input for Timer0. Output is open drain type.
RA5/SS/AN4	bit5	TTL	Input/output or slave select input for synchronous serial port or analog input.

TABLE 3-1: PORTA FUNCTIONS

Legend: TTL = TTL input, ST = Schmitt Trigger input

TABLE 3-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
05h	PORTA			RA5	RA4	RA3	RA2	RA1	RA0	0x 0000	0u 0000
85h	TRISA		—	PORTA	PORTA Data Direction Register						11 1111
9Fh	ADCON1	ADFM	—			PCFG3	PCFG2	PCFG1	PCFG0	0- 0000	0- 0000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

Note: When using the SSP module in SPI Slave mode and \overline{SS} enabled, the A/D converter must be set to one of the following modes, where PCFG3:PCFG0 = 0100,0101, 011x, 1101, 1110, 1111.

3.5 PORTE and TRISE Register

PORTE and TRISE are not implemented on the PIC16F873 or PIC16F876.

PORTE has three pins (RE0/RD/AN5, RE1/WR/AN6, and RE2/CS/AN7) which are individually configureable as inputs or outputs. These pins have Schmitt Trigger input buffers.

The PORTE pins become the I/O control inputs for the microprocessor port when bit PSPMODE (TRISE<4>) is set. In this mode, the user must make certain that the TRISE<2:0> bits are set, and that the pins are configured as digital inputs. Also ensure that ADCON1 is configured for digital I/O. In this mode, the input buffers are TTL.

Register 3-1 shows the TRISE register, which also controls the parallel slave port operation.

PORTE pins are multiplexed with analog inputs. When selected for analog input, these pins will read as '0's.

TRISE controls the direction of the RE pins, even when they are being used as analog inputs. The user must make sure to keep the pins configured as inputs when using them as analog inputs.

Note: On a Power-on Reset, these pins are configured as analog inputs, and read as '0'.

FIGURE 3-8: PORTE BLOCK DIAGRAM (IN I/O PORT MODE)



Name	Bit#	Buffer Type	Function
	hit0	от/тті (1)	I/O port pin or read control input in Parallel Slave Port mode or analog input: RD
REU/RD/AN5	bito	51/11L [.]	 a lide a Read operation. Contents of PORTD register are output to PORTD I/O pins (if chip selected)
RE1/WR/AN6	bit1	ST/TTL ⁽¹⁾	 I/O port pin or write control input in Parallel Slave Port mode or analog input: WR 1 = Idle 0 = Write operation. Value of PORTD I/O pins is latched into PORTD register (if chip selected)
RE2/CS/AN7	bit2	ST/TTL ⁽¹⁾	$\frac{I/O}{CS}$ port pin or chip select control input in Parallel Slave Port mode or analog input: 1 = Device is not selected 0 = Device is selected

TABLE 3-9:PORTE FUNCTIONS

Legend: ST = Schmitt Trigger input, TTL = TTL input

Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffers when in Parallel Slave Port mode.

TABLE 3-10: SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
09h	PORTE	—	_	_	—	_	RE2	RE1	RE0	xxx	uuu
89h	TRISE	IBF	OBF	IBOV	PSPMODE	_	PORTE Data Direction Bits			0000 -111	0000 -111
9Fh	ADCON1	ADFM	_	-	—	PCFG3	PCFG2	PCFG1	PCFG0	0- 0000	0- 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTE.

At the completion of the write cycle, the WR bit is cleared and the EEIF interrupt flag bit is set. (EEIF must be cleared by firmware.) Since the microcontroller does not execute instructions during the write cycle, the firmware does not necessarily have to check either EEIF, or WR, to determine if the write had finished.

EXAMPLE 4-4: FLASH PROGRAM WRITE

BSF	STATUS, RP1	;
BCF	STATUS, RPO	;Bank 2
MOVF	ADDRL, W	;Write address
MOVWF	EEADR	;of desired
MOVF	ADDRH, W	;program memory
MOVWF	EEADRH	;location
MOVF	VALUEL, W	;Write value to
MOVWF	EEDATA	;program at
MOVF	VALUEH, W	;desired memory
MOVWF	EEDATH	;location
BSF	STATUS, RPO	;Bank 3
BSF	EECON1, EEPGD	;Point to Program memory
BSF	EECON1, WREN	;Enable writes
		;Only disable interrupts
BCF	INTCON, GIE	; if already enabled,
		;otherwise discard
MOVLW	0x55	;Write 55h to
MOVWF	EECON2	;EECON2
MOVLW	0xAA	;Write AAh to
MOVWF	EECON2	; EECON2
BSF	EECON1, WR	;Start write operation
NOP		;Two NOPs to allow micro
NOP		;to setup for write
		;Only enable interrupts
BSF	INTCON, GIE	; if using interrupts,
		;otherwise discard
BCF	EECON1, WREN	;Disable writes

4.6 Write Verify

The PIC16F87X devices do not automatically verify the value written during a write operation. Depending on the application, good programming practice may dictate that the value written to memory be verified against the original value. This should be used in applications where excessive writes can stress bits near the specified endurance limits.

4.7 Protection Against Spurious Writes

There are conditions when the device may not want to write to the EEPROM data memory or FLASH program memory. To protect against these spurious write conditions, various mechanisms have been built into the PIC16F87X devices. On power-up, the WREN bit is cleared and the Power-up Timer (if enabled) prevents writes.

The write initiate sequence, and the WREN bit together, help prevent any accidental writes during brown-out, power glitches, or firmware malfunction.

4.8 Operation While Code Protected

The PIC16F87X devices have two code protect mechanisms, one bit for EEPROM data memory and two bits for FLASH program memory. Data can be read and written to the EEPROM data memory, regardless of the state of the code protection bit, CPD. When code protection is enabled and CPD cleared, external access via ICSP is disabled, regardless of the state of the program memory code protect bits. This prevents the contents of EEPROM data memory from being read out of the device.

The state of the program memory code protect bits, CP0 and CP1, do not affect the execution of instructions out of program memory. The PIC16F87X devices can always read the values in program memory, regardless of the state of the code protect bits. However, the state of the code protect bits and the WRT bit will have different effects on writing to program memory. Table 4-1 shows the effect of the code protect bits and the WRT bit on program memory.

Once code protection has been enabled for either EEPROM data memory or FLASH program memory, only a full erase of the entire device will disable code protection.

REGISTER 9-2: SSPCON: SYNC SERIAL PORT CONTROL REGISTER (ADDRESS 14h) R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 WCOL SSPOV SSPM0 SSPEN CKP SSPM3 SSPM2 SSPM1 bit 7 bit 0 bit 7 WCOL: Write Collision Detect bit Master mode: 1 = A write to SSPBUF was attempted while the I2C conditions were not valid 0 = No collision Slave mode: 1 = SSPBUF register is written while still transmitting the previous word (must be cleared in software) 0 = No collision bit 6 SSPOV: Receive Overflow Indicator bit In SPI mode: 1 = A new byte is received while SSPBUF holds previous data. Data in SSPSR is lost on overflow. In Slave mode, the user must read the SSPBUF, even if only transmitting data, to avoid overflows. In Master mode, the overflow bit is not set, since each operation is initiated by writing to the SSPBUF register. (Must be cleared in software.) 0 = No overflowIn I²C mode: 1 = A byte is received while the SSPBUF is holding the previous byte. SSPOV is a "don't care" in Transmit mode. (Must be cleared in software.) 0 = No overflowSSPEN: Synchronous Serial Port Enable bit bit 5 In SPI mode, When enabled, these pins must be properly configured as input or output 1 = Enables serial port and configures SCK, SDO, SDI, and SS as the source of the serial port pins 0 = Disables serial port and configures these pins as I/O port pins In I²C mode, When enabled, these pins must be properly configured as input or output 1 = Enables the serial port and configures the SDA and SCL pins as the source of the serial port pins 0 = Disables serial port and configures these pins as I/O port pins bit 4 CKP: Clock Polarity Select bit In SPI mode: 1 = Idle state for clock is a high level 0 = Idle state for clock is a low level In I²C Slave mode: SCK release control 1 = Enable clock 0 = Holds clock low (clock stretch). (Used to ensure data setup time.) In I²C Master mode: Unused in this mode bit 3-0 SSPM3:SSPM0: Synchronous Serial Port Mode Select bits 0000 = SPI Master mode, clock = Fosc/4 0001 = SPI Master mode, clock = Fosc/16 0010 = SPI Master mode, clock = Fosc/64 0011 = SPI Master mode, clock = TMR2 output/2 0100 = SPI Slave mode, clock = SCK pin. \overline{SS} pin control enabled. 0101 = SPI Slave mode, clock = SCK pin. SS pin control disabled. SS can be used as I/O pin. $0110 = I^2C$ Slave mode, 7-bit address $0111 = I^2C$ Slave mode, 10-bit address 1000 = I²C Master mode, clock = Fosc / (4 * (SSPADD+1)) $1011 = I^2C$ Firmware Controlled Master mode (slave idle) 1110 = I²C Firmware Controlled Master mode, 7-bit address with START and STOP bit interrupts enabled 1111 = I²C Firmware Controlled Master mode, 10-bit address with START and STOP bit interrupts enabled 1001, 1010, 1100, 1101 = Reserved

Legend:							
R = Readable bit	W = Writable bit	U = Unimplemented b	U = Unimplemented bit, read as '0'				
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

TABLE 9-1: REGISTERS ASSOCIATED WITH SPI OPERATION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR, WDT
0Bh, 8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
13h	SSPBUF	Synchrono	ous Serial	Port Recei	ive Buff	er/Transm	it Register			XXXX XXXX	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
94h	SSPSTAT	SMP	CKE	D/A	Ρ	S	R/W	UA	BF	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the SSP in SPI mode. **Note 1:** These bits are reserved on PCI16F873/876 devices; always maintain these bits clear.

9.2 MSSP I²C Operation

The MSSP module in I²C mode, fully implements all master and slave functions (including general call support) and provides interrupts on START and STOP bits in hardware, to determine a free bus (multi-master function). The MSSP module implements the standard mode specifications, as well as 7-bit and 10-bit addressing.

Refer to Application Note AN578, "Use of the SSP Module in the I^2C Multi-Master Environment."

A "glitch" filter is on the SCL and SDA pins when the pin is an input. This filter operates in both the 100 kHz and 400 kHz modes. In the 100 kHz mode, when these pins are an output, there is a slew rate control of the pin that is independent of device frequency.

FIGURE 9-5:

I²C SLAVE MODE BLOCK DIAGRAM



Two pins are used for data transfer. These are the SCL pin, which is the clock, and the SDA pin, which is the data. The SDA and SCL pins are automatically configured when the I^2C mode is enabled. The SSP module functions are enabled by setting SSP Enable bit SSPEN (SSPCON<5>).

The MSSP module has six registers for $\mathsf{I}^2\mathsf{C}$ operation. They are the:

- SSP Control Register (SSPCON)
- SSP Control Register2 (SSPCON2)
- SSP Status Register (SSPSTAT)
- Serial Receive/Transmit Buffer (SSPBUF)
- SSP Shift Register (SSPSR) Not directly accessible
- SSP Address Register (SSPADD)

The SSPCON register allows control of the I^2C operation. Four mode selection bits (SSPCON<3:0>) allow one of the following I^2C modes to be selected:

- I²C Slave mode (7-bit address)
- I²C Slave mode (10-bit address)
- I²C Master mode, clock = OSC/4 (SSPADD +1)
- I²C firmware modes (provided for compatibility to other mid-range products)

Before selecting any I^2C mode, the SCL and SDA pins must be programmed to inputs by setting the appropriate TRIS bits. Selecting an I^2C mode by setting the SSPEN bit, enables the SCL and SDA pins to be used as the clock and data lines in I^2C mode. Pull-up resistors must be provided externally to the SCL and SDA pins for the proper operation of the I^2C module.

The CKE bit (SSPSTAT<6:7>) sets the levels of the SDA and SCL pins in either Master or Slave mode. When CKE = 1, the levels will conform to the SMBus specification. When CKE = 0, the levels will conform to the I^2C specification.

The SSPSTAT register gives the status of the data transfer. This information includes detection of a START (S) or STOP (P) bit, specifies if the received byte was data or address, if the next byte is the completion of 10-bit address, and if this will be a read or write data transfer.

SSPBUF is the register to which the transfer data is written to, or read from. The SSPSR register shifts the data in or out of the device. In receive operations, the SSPBUF and SSPSR create a doubled buffered receiver. This allows reception of the next byte to begin before reading the last byte of received data. When the complete byte is received, it is transferred to the SSPBUF register and flag bit SSPIF is set. If another complete byte is received before the SSPBUF register is read, a receiver overflow has occurred and bit SSPOV (SSPCON<6>) is set and the byte in the SSPSR is lost.

The SSPADD register holds the slave address. In 10-bit mode, the user needs to write the high byte of the address (1111 0 A9 A8 0). Following the high byte address match, the low byte of the address needs to be loaded (A7:A0).

9.2.18.2 Bus Collision During a Repeated START Condition

During a Repeated START condition, a bus collision occurs if:

- a) A low level is sampled on SDA when SCL goes from low level to high level.
- b) SCL goes low before SDA is asserted low, indicating that another master is attempting to transmit a data '1'.

When the user de-asserts SDA and the pin is allowed to float high, the BRG is loaded with SSPADD<6:0> and counts down to 0. The SCL pin is then de-asserted, and when sampled high, the SDA pin is sampled. If SDA is low, a bus collision has occurred (i.e., another master is attempting to transmit a data'0'). If, however,

SDA is sampled high, the BRG is reloaded and begins counting. If SDA goes from high to low before the BRG times out, no bus collision occurs, because no two masters can assert SDA at exactly the same time.

If, however, SCL goes from high to low before the BRG times out and SDA has not already been asserted, a bus collision occurs. In this case, another master is attempting to transmit a data'1' during the Repeated START condition.

If at the end of the BRG time-out, both SCL and SDA are still high, the SDA pin is driven low, the BRG is reloaded and begins counting. At the end of the count, regardless of the status of the SCL pin, the SCL pin is driven low and the Repeated START condition is complete (Figure 9-23).

FIGURE 9-23: BUS COLLISION DURING A REPEATED START CONDITION (CASE 1)



FIGURE 9-24: BUS COLLISION DURING REPEATED START CONDITION (CASE 2)



TABLE 10-3: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 0)

BAUD	F	Fosc = 20 MHz			osc = 16 N	IHz	Fosc = 10 MHz		
RATE (K)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	-	-	-	-	-	-	-	-	-
1.2	1.221	1.75	255	1.202	0.17	207	1.202	0.17	129
2.4	2.404	0.17	129	2.404	0.17	103	2.404	0.17	64
9.6	9.766	1.73	31	9.615	0.16	25	9.766	1.73	15
19.2	19.531	1.72	15	19.231	0.16	12	19.531	1.72	7
28.8	31.250	8.51	9	27.778	3.55	8	31.250	8.51	4
33.6	34.722	3.34	8	35.714	6.29	6	31.250	6.99	4
57.6	62.500	8.51	4	62.500	8.51	3	52.083	9.58	2
HIGH	1.221	-	255	0.977	-	255	0.610	-	255
LOW	312.500	-	0	250.000	-	0	156.250	-	0

		Fosc = 4 M	Hz	Fo	Fosc = 3.6864 MHz			
RATE (K)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)		
0.3	0.300	0	207	0.3	0	191		
1.2	1.202	0.17	51	1.2	0	47		
2.4	2.404	0.17	25	2.4	0	23		
9.6	8.929	6.99	6	9.6	0	5		
19.2	20.833	8.51	2	19.2	0	2		
28.8	31.250	8.51	1	28.8	0	1		
33.6	-	-	-	-	-	-		
57.6	62.500	8.51	0	57.6	0	0		
HIGH	0.244	-	255	0.225	-	255		
LOW	62.500	-	0	57.6	-	0		

TABLE 10-4: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 1)

PAUD	F	osc = 20 M	Hz	F	osc = 16 M	Hz	Fosc = 10 MHz		
RATE (K)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	-	-	-	-	-	-	-	-	-
1.2	-	-	-	-	-	-	-	-	-
2.4	-	-	-	-	-	-	2.441	1.71	255
9.6	9.615	0.16	129	9.615	0.16	103	9.615	0.16	64
19.2	19.231	0.16	64	19.231	0.16	51	19.531	1.72	31
28.8	29.070	0.94	42	29.412	2.13	33	28.409	1.36	21
33.6	33.784	0.55	36	33.333	0.79	29	32.895	2.10	18
57.6	59.524	3.34	20	58.824	2.13	16	56.818	1.36	10
HIGH	4.883	-	255	3.906	-	255	2.441	-	255
LOW	1250.000	-	0	1000.000		0	625.000	-	0

DALID	F	osc = 4 M⊦	łz	Fosc = 3.6864 MHz				
RATE (K)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)		
0.3	-	-	-	-	-	-		
1.2	1.202	0.17	207	1.2	0	191		
2.4	2.404	0.17	103	2.4	0	95		
9.6	9.615	0.16	25	9.6	0	23		
19.2	19.231	0.16	12	19.2	0	11		
28.8	27.798	3.55	8	28.8	0	7		
33.6	35.714	6.29	6	32.9	2.04	6		
57.6	62.500	8.51	3	57.6	0	3		
HIGH	0.977	-	255	0.9	-	255		
LOW	250.000	-	0	230.4	-	0		

10.2.3 SETTING UP 9-BIT MODE WITH ADDRESS DETECT

When setting up an Asynchronous Reception with Address Detect Enabled:

- Initialize the SPBRG register for the appropriate baud rate. If a high speed baud rate is desired, set bit BRGH.
- Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
- If interrupts are desired, then set enable bit RCIE.
- Set bit RX9 to enable 9-bit reception.
- Set ADDEN to enable address detect.
- Enable the reception by setting enable bit CREN.

- Flag bit RCIF will be set when reception is complete, and an interrupt will be generated if enable bit RCIE was set.
- Read the RCSTA register to get the ninth bit and determine if any error occurred during reception.
- Read the 8-bit received data by reading the RCREG register, to determine if the device is being addressed.
- If any error occurred, clear the error by clearing enable bit CREN.
- If the device has been addressed, clear the ADDEN bit to allow data bytes and address bytes to be read into the receive buffer, and interrupt the CPU.



10.4.2 USART SYNCHRONOUS SLAVE RECEPTION

The operation of the Synchronous Master and Slave modes is identical, except in the case of the SLEEP mode. Bit SREN is a "don't care" in Slave mode.

If receive is enabled by setting bit CREN prior to the SLEEP instruction, then a word may be received during SLEEP. On completely receiving the word, the RSR register will transfer the data to the RCREG register and if enable bit RCIE bit is set, the interrupt generated will wake the chip from SLEEP. If the global interrupt is enabled, the program will branch to the interrupt vector (0004h).

When setting up a Synchronous Slave Reception, follow these steps:

1. Enable the synchronous master serial port by setting bits SYNC and SPEN and clearing bit CSRC.

- 2. If interrupts are desired, set enable bit RCIE.
- 3. If 9-bit reception is desired, set bit RX9.
- 4. To enable reception, set enable bit CREN.
- Flag bit RCIF will be set when reception is complete and an interrupt will be generated, if enable bit RCIE was set.
- 6. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
- 7. Read the 8-bit received data by reading the RCREG register.
- 8. If any error occurred, clear the error by clearing bit CREN.
- 9. If using interrupts, ensure that GIE and PEIE (bits 7 and 6) of the INTCON register are set.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh, 8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	R0IF	0000 000x	0000 000u
0Ch	PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
1Ah	RCREG	USART R	USART Receive Register							0000 0000	0000 0000
8Ch	PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register							0000 0000	0000 0000	

TABLE 10-11: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used for synchronous slave reception. **Note** 1: Bits PSPIE and PSPIF are reserved on PIC16F873/876 devices, always maintain these bits clear.

Register		Dev	ices		Power-on Reset, Brown-out Reset WDT Reset		Wake-up via WDT or Interrupt	
W	873	874	876	877	XXXX XXXX	սսսս սսսս	uuuu uuuu	
INDF	873	874	876	877	N/A	N/A	N/A	
TMR0	873	874	876	877	XXXX XXXX	uuuu uuuu	uuuu uuuu	
PCL	873	874	876	877	0000h	0000h	PC + 1 ⁽²⁾	
STATUS	873	874	876	877	0001 1xxx	000q quuu (3)	uuuq quuu (3)	
FSR	873	874	876	877	xxxx xxxx	uuuu uuuu	uuuu uuuu	
PORTA	873	874	876	877	0x 0000	0u 0000	uu uuuu	
PORTB	873	874	876	877	xxxx xxxx	uuuu uuuu	uuuu uuuu	
PORTC	873	874	876	877	xxxx xxxx	uuuu uuuu	uuuu uuuu	
PORTD	873	874	876	877	xxxx xxxx	սսսս սսսս	uuuu uuuu	
PORTE	873	874	876	877	xxx	uuu	uuu	
PCLATH	873	874	876	877	0 0000	0 0000	u uuuu	
INTCON	873	874	876	877	x000 0000	0000 000u	uuuu uuuu (1)	
PIR1	873	874	876	877	r000 0000	r000 0000	ruuu uuuu ⁽¹⁾	
	873	874	876	877	0000 0000	0000 0000	uuuu uuuu ⁽¹⁾	
PIR2	873	874	876	877	-r-0 00	-r-0 00	-r-u uu (1)	
TMR1L	873	874	876	877	xxxx xxxx	uuuu uuuu	uuuu uuuu	
TMR1H	873	874	876	877	xxxx xxxx	uuuu uuuu	uuuu uuuu	
T1CON	873	874	876	877	00 0000	uu uuuu	uu uuuu	
TMR2	873	874	876	877	0000 0000	0000 0000	uuuu uuuu	
T2CON	873	874	876	877	-000 0000	-000 0000	-uuu uuuu	
SSPBUF	873	874	876	877	XXXX XXXX	uuuu uuuu	uuuu uuuu	
SSPCON	873	874	876	877	0000 0000	0000 0000	uuuu uuuu	
CCPR1L	873	874	876	877	XXXX XXXX	uuuu uuuu	uuuu uuuu	
CCPR1H	873	874	876	877	XXXX XXXX	uuuu uuuu	uuuu uuuu	
CCP1CON	873	874	876	877	00 0000	00 0000	uu uuuu	
RCSTA	873	874	876	877	0000 000x	0000 000x	uuuu uuuu	
TXREG	873	874	876	877	0000 0000	0000 0000	uuuu uuuu	
RCREG	873	874	876	877	0000 0000	0000 0000	uuuu uuuu	
CCPR2L	873	874	876	877	XXXX XXXX	uuuu uuuu	uuuu uuuu	
CCPR2H	873	874	876	877	XXXX XXXX	uuuu uuuu	uuuu uuuu	
CCP2CON	873	874	876	877	0000 0000	0000 0000	uuuu uuuu	
ADRESH	873	874	876	877	XXXX XXXX	uuuu uuuu	uuuu uuuu	
ADCON0	873	874	876	877	0000 00-0	0000 00-0	uuuu uu-u	
OPTION_REG	873	874	876	877	1111 1111	1111 1111	uuuu uuuu	
TRISA	873	874	876	877	11 1111	11 1111	uu uuuu	
TRISB	873	874	876	877	1111 1111	1111 1111	uuuu uuuu	
TRISC	873	874	876	877	1111 1111	1111 1111	uuuu uuuu	
TRISD	873	874	876	877	1111 1111	1111 1111	uuuu uuuu	
TRISE	873	874	876	877	0000 -111	0000 -111	uuuu -uuu	
PIE1	873	874	876	877	r000 0000	r000 0000	ruuu uuuu	
	873	874	876	877	0000 0000	0000 0000	uuuu uuuu	

TABLE 12-6: INITIALIZATION CONDITIONS FOR ALL REGISTERS

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition, r = reserved, maintain clear

Note 1: One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 12-5 for RESET value for specific condition.

PIC16F87X



FIGURE 12-7: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 2



FIGURE 12-8: SLOW RISE TIME (MCLR TIED TO VDD)







FIGURE 15-4: PIC16F87X-10 VOLTAGE-FREQUENCY GRAPH (EXTENDED TEMPERATURE RANGE ONLY)







	TABLE 15-4:	TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS
--	-------------	---

Param No.	Symbol		Min	Тур†	Max	Units	Conditions		
40*	Tt0H	T0CKI High Pulse Width		No Prescaler	0.5Tcy + 20	—	—	ns	Must also meet
				With Prescaler	10	Ι		ns	parameter 42
41*	Tt0L	T0CKI Low Pulse	Width	No Prescaler	0.5TCY + 20	—	_	ns	Must also meet
				With Prescaler	10	—	_	ns	parameter 42
42*	Tt0P	T0CKI Period		No Prescaler	Tcy + 40	Ι		ns	
				With Prescaler	Greater of:	—	_	ns	N = prescale value
					20 or <u>Tcy + 40</u>				(2, 4,, 256)
					N				
45*	Tt1H	T1CKI High Time	Synchronous, Pro	escaler = 1	0.5TCY + 20	—	—	ns	Must also meet
			Synchronous,	Standard(F)	15	—	—	ns	parameter 47
			Prescaler = 2,4,8	Extended(LF)	25	_	—	ns	
			Asynchronous	Standard(F)	30	—	—	ns	
				Extended(LF)	50	—	—	ns	
46*	Tt1L	T1CKI Low Time	Synchronous, Pro	escaler = 1	0.5Tcy + 20	—	—	ns	Must also meet
		Synchronous,	Standard(F)	15	—	—	ns	parameter 47	
			Prescaler = 2,4,8	Extended(LF)	25	—	—	ns	
			Asynchronous	Standard(F)	30	_		ns	
				Extended(LF)	50	-	_	ns	
47*	Tt1P	T1CKI input	Synchronous	Standard(F)	Greater of:			ns	N = prescale value
	period				30 or <u>Tcy + 40</u>				(1, 2, 4, 8)
					N				
				Extended(LF)	Greater of:				N = prescale value
					50 OR <u>ICY + 40</u>				(1, 2, 4, 8)
			A		N 00				
			Asynchronous	Standard(F)	60			ns	
	F +4	Time and the sille to a li			100			ns	
	Ft1	i imer1 oscillator ir	put frequency ran	Ige	DC	-	200	KHZ	
40		(oscillator enabled by setting bit T1OSCEN)			27000		77000		
48	ICKEZIMI	Delay from externa	al clock edge to th	ner increment	21050	_	11080		

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



FIGURE 16-13: TYPICAL AND MAXIMUM AlwDT vs. VDD OVER TEMPERATURE





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PIC16F87X





FIGURE 16-20: MINIMUM AND MAXIMUM VIN vs. Vdd, (TTL INPUT, -40°C TO 125°C)



Package Marking Information (Cont'd)



44-Lead TQFP



Example

 \bigcirc

Example



 $\lambda \lambda$

PIC16F877-04/P

0112SAA

MICROCHIP

44-Lead MQFP



Example



44-Lead PLCC



Example



28-Lead Skinny Plastic Dual In-line (SP) – 300 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



		INCHES*		MILLIMETERS			
Dimension I	_imits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	р		.100			2.54	
Top to Seating Plane	А	.140	.150	.160	3.56	3.81	4.06
Molded Package Thickness	A2	.125	.130	.135	3.18	3.30	3.43
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	Е	.300	.310	.325	7.62	7.87	8.26
Molded Package Width	E1	.275	.285	.295	6.99	7.24	7.49
Overall Length	D	1.345	1.365	1.385	34.16	34.67	35.18
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	С	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.040	.053	.065	1.02	1.33	1.65
Lower Lead Width	В	.016	.019	.022	0.41	0.48	0.56
Overall Row Spacing §	eB	.320	.350	.430	8.13	8.89	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter § Significant Characteristic

Dimension D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed

.010" (0.254mm) per side. JEDEC Equivalent: MO-095

Drawing No. C04-070

Notes:

APPENDIX C: CONVERSION CONSIDERATIONS

Considerations for converting from previous versions of devices to the ones listed in this data sheet are listed in Table C-1.

TABLE C-1:	CONVERSION
	CONSIDERATIONS

Characteristic	PIC16C7X	PIC16F87X			
Pins	28/40	28/40			
Timers	3	3			
Interrupts	11 or 12	13 or 14			
Communication	PSP, USART, SSP (SPI, I ² C Slave)	PSP, USART, SSP (SPI, I ² C Master/Slave)			
Frequency	20 MHz	20 MHz			
Voltage	2.5V - 5.5V	2.0V - 5.5V			
A/D	8-bit	10-bit			
CCP	2	2			
Program Memory	4K, 8K EPROM	4K, 8K FLASH			
RAM	192, 368 bytes	192, 368 bytes			
EEPROM data	None	128, 256 bytes			
Other		In-Circuit Debugger, Low Voltage Programming			

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