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Details

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Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	22
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f876t-20-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Key Features PIC [®] MCU Mid-Range Reference Manual (DS33023)	PIC16F873	PIC16F874	PIC16F876	PIC16F877
Operating Frequency	DC - 20 MHz			
RESETS (and Delays)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)
FLASH Program Memory (14-bit words)	4K	4K	8K	8K
Data Memory (bytes)	192	192	368	368
EEPROM Data Memory	128	128	256	256
Interrupts	13	14	13	14
I/O Ports	Ports A,B,C	Ports A,B,C,D,E	Ports A,B,C	Ports A,B,C,D,E
Timers	3	3	3	3
Capture/Compare/PWM Modules	2	2	2	2
Serial Communications	MSSP, USART	MSSP, USART	MSSP, USART	MSSP, USART
Parallel Communications	—	PSP	—	PSP
10-bit Analog-to-Digital Module	5 input channels	8 input channels	5 input channels	8 input channels
Instruction Set	35 instructions	35 instructions	35 instructions	35 instructions

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2.2.2.2 OPTION_REG Register

The OPTION_REG Register is a readable and writable register, which contains various control bits to configure the TMR0 prescaler/WDT postscaler (single assignable register known also as the prescaler), the External INT Interrupt, TMR0 and the weak pull-ups on PORTB.

Note:	To achieve a 1:1 prescaler assignment for
	the TMR0 register, assign the prescaler to
	the Watchdog Timer.

R/W-1 R/W-1 R/W-1 R/W-1 R/W-1 R/W-1 R/W-1 R/W-1 RBPU INTEDG T0CS T0SE PSA PS2 PS1 PS0 bit 7 bit 0 **RBPU:** PORTB Pull-up Enable bit bit 7 1 = PORTB pull-ups are disabled 0 = PORTB pull-ups are enabled by individual port latch values bit 6 **INTEDG:** Interrupt Edge Select bit 1 = Interrupt on rising edge of RB0/INT pin 0 = Interrupt on falling edge of RB0/INT pin bit 5 TOCS: TMR0 Clock Source Select bit 1 = Transition on RA4/T0CKI pin 0 = Internal instruction cycle clock (CLKOUT) bit 4 TOSE: TMR0 Source Edge Select bit 1 = Increment on high-to-low transition on RA4/T0CKI pin 0 = Increment on low-to-high transition on RA4/T0CKI pin bit 3 PSA: Prescaler Assignment bit 1 = Prescaler is assigned to the WDT 0 = Prescaler is assigned to the Timer0 module bit 2-0 PS2:PS0: Prescaler Rate Select bits Bit Value TMR0 Rate WDT Rate 000 1:1 1:2 1:2 001 1:4 010 1:4 1:8 011 1:8 1:16 1:16 100 1:32 101 1:32 1:64 110 1:128 1:64 111 1:128 1:256 Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

Note: When using low voltage ICSP programming (LVP) and the pull-ups on PORTB are enabled, bit 3 in the TRISB register must be cleared to disable the pull-up on RB3 and ensure the proper operation of the device

REGISTER 2-2: OPTION_REG REGISTER (ADDRESS 81h, 181h)

2.2.2.4 **PIE1** Register

The PIE1 register contains the individual enable bits for the peripheral interrupts.

Note:	Bit PEIE (INTCON<6>) must be set to
	enable any peripheral interrupt.

PIE1 REGISTER (ADDRESS 8Ch) **REGISTER 2-4:**

	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE			
	bit 7							bit 0			
bit 7	PSPIE ⁽¹⁾ : F	Parallel Slav	e Port Read	d/Write Inter	rupt Enable bit						
	 1 = Enables the PSP read/write interrupt 0 = Disables the PSP read/write interrupt 										
bit 6	ADIE: A/D	Converter li	nterrupt Ena	able bit							
	1 = Enable 0 = Disable	s the A/D co s the A/D c	onverter inte onverter inte	errupt errupt							
bit 5	RCIE: USA	RT Receive	Interrupt E	nable bit							
	1 = Enable 0 = Disable	s the USAR es the USAF	T receive in RT receive in	nterrupt nterrupt							
bit 4	TXIE: USA	RT Transmi	t Interrupt E	nable bit							
	 1 = Enables the USART transmit interrupt 0 = Disables the USART transmit interrupt 										
bit 3	SSPIE: Syr	nchronous S	Serial Port In	nterrupt Ena	ble bit						
	1 = Enables the SSP interrupt 0 = Disables the SSP interrupt										
bit 2	CCP1IE: C	CP1 Interru	pt Enable b	it							
	1 = Enable	s the CCP1	interrupt								
	0 = Disable	es the CCP1	interrupt								
bit 1	TMR2IE: T	MR2 to PR2	2 Match Inte	errupt Enable	e bit						
	1 = Enable 0 = Disable	s the TMR2 es the TMR2	to PR2 ma to PR2 ma	tch interrupt atch interrup	t						
bit 0	TMR1IE: T	MR1 Overfle	ow Interrupt	Enable bit							
	1 = Enable 0 = Disable	s the TMR1 s the TMR1	overflow in overflow ir	terrupt nterrupt							

Note 1: PSPIE is reserved on PIC16F873/876 devices; always maintain this bit clear.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

NOTES:

TABLE 3-5:PORTC FUNCTIONS

Name	Bit#	Buffer Type	Function
RC0/T1OSO/T1CKI	bit0	ST	Input/output port pin or Timer1 oscillator output/Timer1 clock input.
RC1/T1OSI/CCP2	bit1	ST	Input/output port pin or Timer1 oscillator input or Capture2 input/ Compare2 output/PWM2 output.
RC2/CCP1	bit2	ST	Input/output port pin or Capture1 input/Compare1 output/ PWM1 output.
RC3/SCK/SCL	bit3	ST	RC3 can also be the synchronous serial clock for both SPI and I ² C modes.
RC4/SDI/SDA	bit4	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I ² C mode).
RC5/SDO	bit5	ST	Input/output port pin or Synchronous Serial Port data output.
RC6/TX/CK	bit6	ST	Input/output port pin or USART Asynchronous Transmit or Synchronous Clock.
RC7/RX/DT	bit7	ST	Input/output port pin or USART Asynchronous Receive or Synchronous Data.

Legend: ST = Schmitt Trigger input

TABLE 3-6: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
07h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	XXXX XXXX	uuuu uuuu
87h	TRISC	PORTC	Data Dire	ection Re	egister					1111 1111	1111 1111

Legend: x = unknown, u = unchanged

3.4 **PORTD and TRISD Registers**

PORTD and TRISD are not implemented on the PIC16F873 or PIC16F876.

PORTD is an 8-bit port with Schmitt Trigger input buffers. Each pin is individually configureable as an input or output.

PORTD can be configured as an 8-bit wide microprocessor port (parallel slave port) by setting control bit PSPMODE (TRISE<4>). In this mode, the input buffers are TTL.

FIGURE 3-7: PORTD BLOCK DIAGRAM (IN I/O PORT MODE)



Name	Bit#	Buffer Type	Function
RD0/PSP0	bit0	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit0.
RD1/PSP1	bit1	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit1.
RD2/PSP2	bit2	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit2.
RD3/PSP3	bit3	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit3.
RD4/PSP4	bit4	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit4.
RD5/PSP5	bit5	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit5.
RD6/PSP6	bit6	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit6.
RD7/PSP7	bit7	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit7.

TABLE 3-7: PORTD FUNCTIONS

Legend: ST = Schmitt Trigger input, TTL = TTL input

Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffers when in Parallel Slave Port mode.

TABLE 3-8: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
08h	PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx	uuuu uuuu
88h	TRISD	PORTD Data Direction Register							1111 1111	1111 1111	
89h	TRISE	IBF	OBF	IBOV	PSPMODE		PORTE	Data Direo	ction Bits	0000 -111	0000 -111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTD.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
01h,101h	TMR0	Timer0	Module's F	Registe	r					xxxx xxxx	uuuu uuuu
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
81h,181h	OPTION_REG	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer0.

6.7 Resetting of Timer1 Register Pair (TMR1H, TMR1L)

TMR1H and TMR1L registers are not reset to 00h on a POR, or any other RESET, except by the CCP1 and CCP2 special event triggers.

T1CON register is reset to 00h on a Power-on Reset, or a Brown-out Reset, which shuts off the timer and leaves a 1:1 prescale. In all other RESETS, the register is unaffected.

6.8 Timer1 Prescaler

The prescaler counter is cleared on writes to the TMR1H or TMR1L registers.

TABLE 6-2: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Address	Name	Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0							Value on: POR, BOR	Value on all other RESETS	
0Bh,8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF ⁽¹⁾ ADIF RCIF TXIF SSPIF CCP1IF TMR2IF TMR1IF							0000 0000	0000 0000	
8Ch	PIE1	PSPIE ⁽¹⁾ ADIE RCIE TXIE SSPIE CCP1IE TMR2IE TMR1IE					0000 0000	0000 0000			
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register									uuuu uuuu
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register									uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00 0000	uu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

Note 1: Bits PSPIE and PSPIF are reserved on the PIC16F873/876; always maintain these bits clear.

9.0 MASTER SYNCHRONOUS SERIAL PORT (MSSP) MODULE

The Master Synchronous Serial Port (MSSP) module is a serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D converters, etc. The MSSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I²C)

Figure 9-1 shows a block diagram for the SPI mode, while Figure 9-5 and Figure 9-9 show the block diagrams for the two different I^2C modes of operation.

The Application Note AN734, "Using the PIC[®] MCU SSP for Slave I²CTM Communication" describes the slave operation of the MSSP module on the PIC16F87X devices. AN735, "Using the PIC[®] MCU MSSP Module for I²CTM Communications" describes the master operation of the MSSP module on the PIC16F87X devices.

SSPSTAT: SYNC SERIAL PORT STATUS REGISTER (ADDRESS: 94h) REGISTER 9-1: R/W-0 R/W-0 R-0 R-0 R-0 R-0 R-0 R-0 SMP D/A Р R/W BF CKE S UA bit 7 bit 0 bit 7 SMP: Sample bit SPI Master mode: 1 = Input data sampled at end of data output time 0 = Input data sampled at middle of data output time SPI Slave mode: SMP must be cleared when SPI is used in slave mode In I²C Master or Slave mode: 1 = Slew rate control disabled for standard speed mode (100 kHz and 1 MHz) 0 = Slew rate control enabled for high speed mode (400 kHz) bit 6 CKE: SPI Clock Edge Select (Figure 9-2, Figure 9-3 and Figure 9-4) SPI mode: For CKP = 0 1 = Data transmitted on rising edge of SCK 0 = Data transmitted on falling edge of SCK For CKP = 1 1 = Data transmitted on falling edge of SCK 0 = Data transmitted on rising edge of SCK In I²C Master or Slave mode: 1 = Input levels conform to SMBus spec 0 = Input levels conform to I²C specs **D/A**: Data/Address bit (I²C mode only) bit 5 1 = Indicates that the last byte received or transmitted was data 0 = Indicates that the last byte received or transmitted was address bit 4 P: STOP bit (I²C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.) 1 = Indicates that a STOP bit has been detected last (this bit is '0' on RESET) 0 = STOP bit was not detected last bit 3 S: START bit (I²C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.) 1 = Indicates that a START bit has been detected last (this bit is '0' on RESET) 0 = START bit was not detected last bit 2 **R/W**: Read/Write bit Information (I²C mode only) This bit holds the R/W bit information following the last address match. This bit is only valid from the address match to the next START bit, STOP bit or not ACK bit. In I²C Slave mode: 1 = Read0 = WriteIn I²C Master mode: 1 = Transmit is in progress 0 = Transmit is not in progress Logical OR of this bit with SEN, RSEN, PEN, RCEN, or ACKEN will indicate if the MSSP is in IDLE mode. bit 1 **UA**: Update Address (10-bit I²C mode only) 1 = Indicates that the user needs to update the address in the SSPADD register 0 = Address does not need to be updated bit BF: Buffer Full Status bit Receive (SPI and I²C modes): 1 = Receive complete, SSPBUF is full 0 = Receive not complete, SSPBUF is empty Transmit (I²C mode only): 1 = Data transmit in progress (does not include the ACK and STOP bits), SSPBUF is full 0 = Data transmit complete (does not include the ACK and STOP bits), SSPBUF is empty Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

- n = Value at POR

'1' = Bit is set

x = Bit is unknown

'0' = Bit is cleared

9.1 SPI Mode

The SPI mode allows 8 bits of data to be synchronously transmitted and received simultaneously. All four modes of SPI are supported. To accomplish communication, typically three pins are used:

- Serial Data Out (SDO)
- Serial Data In (SDI)
- Serial Clock (SCK)

Additionally, a fourth pin may be used when in a Slave mode of operation:

Slave Select (SS)

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits (SSPCON<5:0> and SSPSTAT<7:6>). These control bits allow the following to be specified:

- Master mode (SCK is the clock output)
- Slave mode (SCK is the clock input)
- Clock Polarity (Idle state of SCK)
- Data input sample phase (middle or end of data output time)
- Clock edge (output data on rising/falling edge of SCK)
- Clock Rate (Master mode only)
- Slave Select mode (Slave mode only)

Figure 9-4 shows the block diagram of the MSSP module when in SPI mode.

To enable the serial port, MSSP Enable bit, SSPEN (SSPCON<5>) must be set. To reset or reconfigure SPI mode, clear bit SSPEN, re-initialize the SSPCON registers, and then set bit SSPEN. This configures the SDI, SDO, SCK and SS pins as serial port pins. For the pins to behave as the serial port function, some must have their data direction bits (in the TRIS register) appropriately programmed. That is:

- · SDI is automatically controlled by the SPI module
- SDO must have TRISC<5> cleared
- SCK (Master mode) must have TRISC<3> cleared
- SCK (Slave mode) must have TRISC<3> set
- SS must have TRISA<5> set and register ADCON1 (see Section 11.0: A/D Module) must be set in a way that pin RA5 is configured as a digital I/O

Any serial port function that is not desired may be overridden by programming the corresponding data direction (TRIS) register to the opposite value.

FIGURE 9-1: MSSP BLOCK DIAGRAM (SPI MODE)





9.3 Connection Considerations for I²C Bus

For standard-mode $I^{2}C$ bus devices, the values of resistors R_{p} and R_{s} in Figure 9-27 depend on the following parameters:

- Supply voltage
- Bus capacitance
- Number of connected devices (input current + leakage current)

The supply voltage limits the minimum value of resistor R_{p} , due to the specified minimum sink current of 3 mA at VOL max = 0.4V, for the specified output stages. For

example, with a supply voltage of VDD = $5V\pm10\%$ and VOL max = 0.4V at 3 mA, R_p min = $(5.5-0.4)/0.003 = 1.7 \text{ k}\Omega$. VDD as a function of R_p is shown in Figure 9-27. The desired noise margin of 0.1VDD for the low level limits the maximum value of R_s . Series resistors are optional and used to improve ESD susceptibility.

The bus capacitance is the total capacitance of wire, connections, and pins. This capacitance limits the maximum value of R_p due to the specified rise time (Figure 9-27).

The SMP bit is the slew rate control enabled bit. This bit is in the SSPSTAT register, and controls the slew rate of the I/O pins when in I^2C mode (master or slave).





PIC16F87X

	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-x					
	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D					
	bit 7							bit 0					
bit 7	SPEN: Ser	SPEN: Serial Port Enable bit											
	1 = Serial p	oort enabled	(configures	RC7/RX/D	I and RC6/I	X/CK pins a	is serial port	: pins)					
bit 6	0 = Senar	Pocoivo Enc	u ahla hit										
DIL U	1 = Selects	9-bit recept	tion										
	0 = Selects	8-bit recept	tion										
bit 5	SREN: Sin	gle Receive	Enable bit										
	Asynchron	<u>ous mode:</u>											
	Don't care												
	Synchrono	<u>us mode - m</u> a aingla raa	<u>naster:</u>										
	1 = Enables single receive 0 = Disables single receive												
	This bit is cleared after reception is complete.												
	Synchronous mode - slave:												
	Don't care												
bit 4	CREN: Cor	ntinuous Re	ceive Enabl	e bit									
	Asynchronous mode:												
	1 = Enable 0 = Disable	s continuou: es continuou	s receive										
	Synchronous mode:												
	1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)												
	0 = Disable	es continuou	s receive										
bit 3	ADDEN: A	ddress Dete	ect Enable b	it									
	Asynchron	<u>ous mode 9-</u>	<u>-bit (RX9 = ´</u>	<u>1):</u> ablasinterru	امحما امحما	of the react	a huffaruuh						
	 = Enables address detection, enables interrupt and load of the receive buffer when RSR<8> is set 												
	0 = Disable	es address d	letection, all	bytes are re	eceived, and	ninth bit ca	n be used a	s parity bit					
bit 2	FERR: Fra	ming Error b	oit										
	1 = Framin	g error (can	be updated	by reading	RCREG regi	ster and rec	ceive next va	alid byte)					
	0 = No frar	ning error											
bit 1		errun Error	bit	hu olooring l									
	1 = Overru	rrun error	be cleared	by cleaning i									
bit 0	RX9D: 9th	bit of Recei	ived Data (c	an be parity	bit but mus	t be calculat	ted by user i	firmware)					
2 0						. se calculu							
	Legend:												
	R = Reada	ble bit	W = W	/ritable bit	U = Unim	plemented	bit. read as	ʻ0'					

'1' = Bit is set

'0' = Bit is cleared

REGISTER 10-2: RCSTA: RECEIVE STATUS AND CONTROL REGISTER (ADDRESS 18h)

- n = Value at POR

x = Bit is unknown

12.13 Power-down Mode (SLEEP)

Power-down mode is entered by executing a $\ensuremath{\mathtt{SLEEP}}$ instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the PD bit (STATUS<3>) is cleared, the TO (STATUS<4>) bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, place all I/O pins at either VDD or VSS, ensure no external circuitry is drawing current from the I/O pin, power-down the A/D and disable external clocks. Pull all I/O pins that are hi-impedance inputs, high or low externally, to avoid switching currents caused by floating inputs. The TOCKI input should also be at VDD or VSS for lowest current consumption. The contribution from on-chip pull-ups on PORTB should also be considered.

The MCLR pin must be at a logic high level (VIHMC).

12.13.1 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

- 1. External RESET input on MCLR pin.
- 2. Watchdog Timer Wake-up (if WDT was enabled).
- 3. Interrupt from INT pin, RB port change or peripheral interrupt.

External MCLR Reset will cause a device RESET. All other events are considered a continuation of program execution and cause a "wake-up". The TO and PD bits in the STATUS register can be used to determine the cause of device RESET. The PD bit, which is set on power-up, is cleared when SLEEP is invoked. The TO bit is cleared if a WDT time-out occurred and caused wake-up.

The following peripheral interrupts can wake the device from SLEEP:

- 1. PSP read or write (PIC16F874/877 only).
- 2. TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
- 3. CCP Capture mode interrupt.
- 4. Special event trigger (Timer1 in Asynchronous mode using an external clock).
- 5. SSP (START/STOP) bit detect interrupt.
- SSP transmit or receive in Slave mode (SPI/I²C).
- 7. USART RX or TX (Synchronous Slave mode).
- 8. A/D conversion (when A/D clock source is RC).
- 9. EEPROM write operation completion

Other peripherals cannot generate interrupts since during SLEEP, no on-chip clocks are present. When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

12.13.2 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT postscaler will not be cleared, the TO bit will not be set and PD bits will not be cleared.
- If the interrupt occurs during or after the execution of a SLEEP instruction, the device will immediately wake-up from SLEEP. The SLEEP instruction will be completely executed before the wake-up. Therefore, the WDT and WDT postscaler will be cleared, the TO bit will be set and the PD bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the PD bit. If the PD bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction.





	TABLE 15-4:	TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS
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Param No.	Symbol		Characteristic		Min	Тур†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse	Width	No Prescaler	0.5Tcy + 20	—	—	ns	Must also meet
				With Prescaler	10	Ι		ns	parameter 42
41*	Tt0L	T0CKI Low Pulse	Width	No Prescaler	0.5TCY + 20	—	_	ns	Must also meet
				With Prescaler	10	—	_	ns	parameter 42
42*	Tt0P	T0CKI Period		No Prescaler	Tcy + 40	Ι		ns	
				With Prescaler	Greater of:	—	_	ns	N = prescale value
					20 or <u>Tcy + 40</u>				(2, 4,, 256)
					N				
45*	Tt1H	T1CKI High Time	Synchronous, Pro	escaler = 1	0.5TCY + 20	—	—	ns	Must also meet
			Synchronous,	Standard(F)	15	—	—	ns	parameter 47
		Prescaler = 2,4,8	Extended(LF)	25	_	—	ns		
			Asynchronous	Standard(F)	30	—	—	ns	-
				Extended(LF)	50	—	—	ns	
46*	Tt1L	T1CKI Low Time	Synchronous, Pro	escaler = 1	0.5Tcy + 20	—	—	ns	Must also meet
			Synchronous,	Standard(F)	15	—	—	ns	parameter 47
			Prescaler = 2,4,8	Extended(LF)	25	—	—	ns	
			Asynchronous	Standard(F)	30	_		ns	
				Extended(LF)	50	-	_	ns	
47*	Tt1P	T1CKI input	Synchronous	Standard(F)	Greater of:			ns	N = prescale value
		period			30 or <u>Tcy + 40</u>				(1, 2, 4, 8)
					N				
				Extended(LF)	Greater of:				N = prescale value
					50 OR <u>ICY + 40</u>				(1, 2, 4, 8)
			A		N 00				
			Asynchronous	Standard(F)	60			ns	
	F +4	Time and the sille to a li			100			ns	
	Ft1	i imer1 oscillator ir	put frequency ran	Ige	DC	-	200	KHZ	
40		Oscillator enabled	by setting bit 11C	JOCEN)	27000		77000		
48	ICKEZIMI	Delay from externa	al clock edge to th	ner increment	21050	_	11080		

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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NOTES: