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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f877t-20i-l

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Pin Diagrams



2.2 Data Memory Organization

The data memory is partitioned into multiple banks which contain the General Purpose Registers and the Special Function Registers. Bits RP1 (STATUS<6>) and RP0 (STATUS<5>) are the bank select bits.

RP1:RP0	Bank
00	0
01	1
10	2
11	3

Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers, implemented as static RAM. All implemented banks contain Special Function Registers. Some frequently used Special Function Registers from one bank may be mirrored in another bank for code reduction and quicker access.

Note:	EEPROM Data Memory description can be found in Section 4.0 of this data sheet.
0.0.4	

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file can be accessed either directly, or indirectly through the File Select Register (FSR).

FIC	GU	RF	2-3	-
			<u> </u>	

PIC16F877/876 REGISTER FILE MAP

	File Address	ŀ	File Address		File Address		Addre
Indirect addr.(*)) _{00h}	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180
TMR0	01h	OPTION REG	81h	TMR0	101h	OPTION REG	181
PCL	02h	PCI	82h	PCL	102h	PCI	182
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183
FSR	04h	FSR	8/h	FSR	104h	FSR	184
PORTA	05h	TRISA	85h		105h		185
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186
PORTC	07h	TRISC	87h	TORTE	107h		187
PORTD ⁽¹⁾	08h	TRISD ⁽¹⁾	88h		108h		188
	09h	TRISE ⁽¹⁾	80h		109h		189
PCLATH	0Ah	PCLATH	84h	PCLATH	10Ah	PCLATH	184
	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18F
PIR1	0Ch	PIF1	8Ch	FEDATA	10Ch	EECON1	180
PIR2	0Dh	PIF2	8Dh	EEADR	10Dh	EECON2	180
TMR1I	0Eh	PCON	8Eh	FEDATH	10Eh	Reserved ⁽²⁾	185
TMR1H	0Fh	10011	8Fh	EEADRH	10Fh	Reserved ⁽²⁾	185
T1CON	10h		Q0h		110h	110001100	190
TMR2	11h	SSPCON2	01h		111h		191
T2CON	12h	PR2	97h		112h		192
SSPBUE	13h	SSPADD	9211 93h		113h		193
SSPCON	14h	SSPSTAT	9311 97h		114h		194
CCPR1I	15h	00101/11	95h		115h		195
CCPR1H	16h		96h		116h		196
CCP1CON	17h		97h	General	117h	General	197
RCSTA	18h	TXSTA	98h	Purpose	118h	Purpose	198
TXREG	19h	SPBRG	aah	16 Bytes	119h	16 Bytes	190
RCREG	1Ah	OF BIXO	۹۵h	10 Dytes	11Ah	TO Dytoo	194
CCPR2I	1Bh		9Rh		11Bh		19F
CCPR2H	1Ch		9Ch		11Ch		190
CCP2CON	1Dh		9Dh		11Dh		190
	1Eh	ADRESI	9Dh QEh		11Eh		195
	1Fh		QEh		11Fh		19E
ADCONU	20h	ADCONT	A0h		120h		1A0
General Purpose Register 96 Bvtes		General Purpose Register 80 Bytes	FFh	General Purpose Register 80 Bytes	16Eb	General Purpose Register 80 Bytes	1EF
	7Fh	accesses 70h-7Fh	F0h	accesses 70h-7Fh	170h 17Fh	accesses 70h - 7Fh	1F0 1FF
D 1 2		Bank 1		Bank 2		Bank 3	

2: These registers are reserved, maintain these registers clear.

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral modules for controlling the desired operation of the device. These registers are implemented as static RAM. A list of these registers is given in Table 2-1. The Special Function Registers can be classified into two sets: core (CPU) and peripheral. Those registers associated with the core functions are described in detail in this section. Those related to the operation of the peripheral features are described in detail in the peripheral features section.

 TABLE 2-1:
 SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page:
Bank 0											
00h ⁽³⁾	INDF	Addressin	g this locatio	egister)	0000 0000	27					
01h	TMR0	Timer0 Mc	dule Registe	ər						xxxx xxxx	47
02h ⁽³⁾	PCL	Program C	Counter (PC)	Least Signif	icant Byte					0000 0000	26
03h ⁽³⁾	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	18
04h ⁽³⁾	FSR	Indirect Da	ata Memory	Address Poir	nter					xxxx xxxx	27
05h	PORTA		_	PORTA Da	ta Latch whe	n written: POI	RTA pins whe	n read		0x 0000	29
06h	PORTB	PORTB Da	ata Latch wh	en written: F	ORTB pins v	hen read				xxxx xxxx	31
07h	PORTC	PORTC D	ata Latch wh	en written: F	ORTC pins v	vhen read				xxxx xxxx	33
08h ⁽⁴⁾	PORTD	PORTD D	ata Latch wh	en written: F	ORTD pins v	vhen read				xxxx xxxx	35
09h ⁽⁴⁾	PORTE		_		_	_	RE2	RE1	RE0	xxx	36
0Ah ^(1,3)	PCLATH		_		Write Buffer	for the upper	r 5 bits of the l	Program Cou	unter	0 0000	26
0Bh ⁽³⁾	INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	20
0Ch	PIR1	PSPIF ⁽³⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	22
0Dh	PIR2	_	(5)	—	EEIF	BCLIF	_	_	CCP2IF	-r-0 00	24
0Eh	TMR1L	Holding re	Holding register for the Least Significant Byte of the 16-bit TMR1 Register								52
0Fh	TMR1H	Holding re	gister for the	Most Signif	icant Byte of	the 16-bit TM	R1 Register			xxxx xxxx	52
10h	T1CON		_	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00 0000	51
11h	TMR2	Timer2 Mo	dule Registe	ər						0000 0000	55
12h	T2CON		TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	55
13h	SSPBUF	Synchrono	ous Serial Po	ort Receive E	Suffer/Transm	it Register				xxxx xxxx	70, 73
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	67
15h	CCPR1L	Capture/C	ompare/PW	M Register1	(LSB)					xxxx xxxx	57
16h	CCPR1H	Capture/C	ompare/PWI	M Register1	(MSB)					xxxx xxxx	57
17h	CCP1CON		—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	58
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	96
19h	TXREG	USART Tr	ansmit Data	Register						0000 0000	99
1Ah	RCREG	USART Re	eceive Data	Register						0000 0000	101
1Bh	CCPR2L	Capture/C	ompare/PW	M Register2	(LSB)					xxxx xxxx	57
1Ch	CCPR2H	Capture/C	ompare/PWI	M Register2	(MSB)					xxxx xxxx	57
1Dh	CCP2CON	—	_	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	58
1Eh	ADRESH	A/D Resul	t Register Hi	gh Byte						xxxx xxxx	116
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	_	ADON	0000 00-0	111

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.

Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

2: Bits PSPIE and PSPIF are reserved on PIC16F873/876 devices; always maintain these bits clear.

3: These registers can be addressed from any bank.

4: PORTD, PORTE, TRISD, and TRISE are not physically implemented on PIC16F873/876 devices; read as '0'.

5: PIR2<6> and PIE2<6> are reserved on these devices; always maintain these bits clear.

2.2.2.6 PIE2 Register

The PIE2 register contains the individual enable bits for the CCP2 peripheral interrupt, the SSP bus collision interrupt, and the EEPROM write operation interrupt.

REGISTER 2-6: PIE2 REGISTER (ADDRESS 8Dh)

	U-0	R/W-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0				
	_	Reserved	_	EEIE	BCLIE	—	—	CCP2IE				
	bit 7							bit 0				
bit 7	Unimplem	ented: Read	l as '0'									
bit 6	Reserved:	Reserved: Always maintain this bit clear										
bit 5	Unimplem	Unimplemented: Read as '0'										
bit 4	EEIE: EEP	EEIE: EEPROM Write Operation Interrupt Enable										
	1 = Enable	1 = Enable EE Write Interrupt										
	0 = Disable	e EE Write In	terrupt									
bit 3	BCLIE: Bu	s Collision In	iterrupt Ena	able								
	 1 = Enable Bus Collision Interrupt 0 = Disable Bus Collision Interrupt 											
bit 2-1	Unimplemented: Read as '0'											
bit 0	CCP2IE: CCP2 Interrupt Enable bit											
	1 = Enables the CCP2 interrupt											
	0 = Disable	0 = Disables the CCP2 interrupt										
	Legend:											
	R = Reada	ble bit	VV = V	Vritable bit	U = Unimpl	emented b	it, read as '	0'				
	- n = Value	at POR	'1' = E	Bit is set	'0' = Bit is o	leared	x = Bit is u	nknown				

4.4 Reading the FLASH Program Memory

Reading FLASH program memory is much like that of EEPROM data memory, only two NOP instructions must be inserted after the RD bit is set. These two instruction cycles that the NOP instructions execute, will be used by the microcontroller to read the data out of program the memory and insert value into the EEDATH:EEDATA registers. Data will be available following the second NOP instruction. EEDATH and EEDATA will hold their value until another read operation is initiated, or until they are written by firmware.

The steps to reading the FLASH program memory are:

- 1. Write the address to EEADRH:EEADR. Make sure that the address is not larger than the memory size of the PIC16F87X device.
- 2. Set the EEPGD bit to point to FLASH program memory.
- 3. Set the RD bit to start the read operation.
- 4. Execute two NOP instructions to allow the microcontroller to read out of program memory.
- 5. Read the data from the EEDATH:EEDATA registers.

EXAMPLE 4-3: FLASH PROGRAM READ

BSF	STATUS, RP1	;
BCF	STATUS, RPO	;Bank 2
MOVF	ADDRL, W	;Write the
MOVWF	EEADR	;address bytes
MOVF	ADDRH,W	;for the desired
MOVWF	EEADRH	;address to read
BSF	STATUS, RPO	;Bank 3
BSF	EECON1, EEPGD	;Point to Program memory
BSF	EECON1, RD	;Start read operation
NOP		;Required two NOPs
NOP		;
BCF	STATUS, RPO	;Bank 2
MOVF	EEDATA, W	;DATAL = EEDATA
MOVWF	DATAL	;
MOVF	EEDATH,W	;DATAH = EEDATH
MOVWF	DATAH	;

4.5 Writing to the FLASH Program Memory

Writing to FLASH program memory is unique, in that the microcontroller does not execute instructions while programming is taking place. The oscillator continues to run and all peripherals continue to operate and queue interrupts, if enabled. Once the write operation completes (specification D133), the processor begins executing code from where it left off. The other important difference when writing to FLASH program memory, is that the WRT configuration bit, when clear, prevents any writes to program memory (see Table 4-1).

Just like EEPROM data memory, there are many steps in writing to the FLASH program memory. Both address and data values must be written to the SFRs. The EEPGD bit must be set, and the WREN bit must be set to enable writes. The WREN bit should be kept clear at all times, except when writing to the FLASH Program memory. The WR bit can only be set if the WREN bit was set in a previous operation, i.e., they both cannot be set in the same operation. The WREN bit should then be cleared by firmware after the write. Clearing the WREN bit before the write actually completes will not terminate the write in progress.

Writes to program memory must also be prefaced with a special sequence of instructions that prevent inadvertent write operations. This is a sequence of five instructions that must be executed without interruption for each byte written. These instructions must then be followed by two NOP instructions to allow the microcontroller to setup for the write operation. Once the write is complete, the execution of instructions starts with the instruction after the second NOP.

The steps to write to program memory are:

- 1. Write the address to EEADRH:EEADR. Make sure that the address is not larger than the memory size of the PIC16F87X device.
- 2. Write the 14-bit data value to be programmed in the EEDATH:EEDATA registers.
- 3. Set the EEPGD bit to point to FLASH program memory.
- 4. Set the WREN bit to enable program operations.
- 5. Disable interrupts (if enabled).
- 6. Execute the special five instruction sequence:
 - Write 55h to EECON2 in two steps (first to W, then to EECON2)
 - Write AAh to EECON2 in two steps (first to W, then to EECON2)
 - Set the WR bit
- 7. Execute two NOP instructions to allow the microcontroller to setup for write operation.
- 8. Enable interrupts (if using interrupts).
- 9. Clear the WREN bit to disable program operations.

At the completion of the write cycle, the WR bit is cleared and the EEIF interrupt flag bit is set. (EEIF must be cleared by firmware.) Since the microcontroller does not execute instructions during the write cycle, the firmware does not necessarily have to check either EEIF, or WR, to determine if the write had finished.

EXAMPLE 4-4: FLASH PROGRAM WRITE

BSF	STATUS, RP1	;
BCF	STATUS, RPO	;Bank 2
MOVF	ADDRL, W	;Write address
MOVWF	EEADR	;of desired
MOVF	ADDRH, W	;program memory
MOVWF	EEADRH	;location
MOVF	VALUEL, W	;Write value to
MOVWF	EEDATA	;program at
MOVF	VALUEH, W	;desired memory
MOVWF	EEDATH	;location
BSF	STATUS, RPO	;Bank 3
BSF	EECON1, EEPGD	;Point to Program memory
BSF	EECON1, WREN	;Enable writes
		;Only disable interrupts
BCF	INTCON, GIE	; if already enabled,
		;otherwise discard
MOVLW	0x55	;Write 55h to
MOVWF	EECON2	;EECON2
MOVLW	0xAA	;Write AAh to
MOVWF	EECON2	;EECON2
BSF	EECON1, WR	;Start write operation
NOP		;Two NOPs to allow micro
NOP		;to setup for write
		;Only enable interrupts
BSF	INTCON, GIE	; if using interrupts,
		;otherwise discard
BCF	EECON1, WREN	;Disable writes

4.6 Write Verify

The PIC16F87X devices do not automatically verify the value written during a write operation. Depending on the application, good programming practice may dictate that the value written to memory be verified against the original value. This should be used in applications where excessive writes can stress bits near the specified endurance limits.

4.7 Protection Against Spurious Writes

There are conditions when the device may not want to write to the EEPROM data memory or FLASH program memory. To protect against these spurious write conditions, various mechanisms have been built into the PIC16F87X devices. On power-up, the WREN bit is cleared and the Power-up Timer (if enabled) prevents writes.

The write initiate sequence, and the WREN bit together, help prevent any accidental writes during brown-out, power glitches, or firmware malfunction.

4.8 Operation While Code Protected

The PIC16F87X devices have two code protect mechanisms, one bit for EEPROM data memory and two bits for FLASH program memory. Data can be read and written to the EEPROM data memory, regardless of the state of the code protection bit, CPD. When code protection is enabled and CPD cleared, external access via ICSP is disabled, regardless of the state of the program memory code protect bits. This prevents the contents of EEPROM data memory from being read out of the device.

The state of the program memory code protect bits, CP0 and CP1, do not affect the execution of instructions out of program memory. The PIC16F87X devices can always read the values in program memory, regardless of the state of the code protect bits. However, the state of the code protect bits and the WRT bit will have different effects on writing to program memory. Table 4-1 shows the effect of the code protect bits and the WRT bit on program memory.

Once code protection has been enabled for either EEPROM data memory or FLASH program memory, only a full erase of the entire device will disable code protection.

4.9 FLASH Program Memory Write Protection

The configuration word contains a bit that write protects the FLASH program memory, called WRT. This bit can only be accessed when programming the PIC16F87X device via ICSP. Once write protection is enabled, only an erase of the entire device will disable it. When enabled, write protection prevents any writes to FLASH program memory. Write protection does not affect program memory reads.

TABLE 4-1: READ/WRITE STATE OF INTERNAL FLASH PROGRAM MEMORY

Со	Configuration Bits		MomenyLeastion	Internal	Internal		
CP1	CP0	WRT	Memory Location	Read	Write	ICSP Read	ICSP write
0	0	x	All program memory	Yes	No	No	No
0	1	0	Unprotected areas	Yes	No	Yes	No
0	1	0	Protected areas	Yes	No	No	No
0	1	1	Unprotected areas	Yes	Yes	Yes	No
0	1	1	Protected areas	Yes	No	No	No
1	0	0	Unprotected areas	Yes	No	Yes	No
1	0	0	Protected areas	Yes	No	No	No
1	0	1	Unprotected areas	Yes	Yes	Yes	No
1	0	1	Protected areas	Yes	No	No	No
1	1	0	All program memory	Yes	No	Yes	Yes
1	1	1	All program memory	Yes	Yes	Yes	Yes

|--|

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
10Dh	EEADR	EEPROM	1 Address	s Register	, Low Byt	е				xxxx xxxx	uuuu uuuu
10Fh	EEADRH	—	_	—	EEPROM Address, High Byte					xxxx xxxx	uuuu uuuu
10Ch	EEDATA	EEPROM	EEPROM Data Register, Low Byte							xxxx xxxx	uuuu uuuu
10Eh	EEDATH	—	_	EEPRO	EEPROM Data Register, High Byte					xxxx xxxx	uuuu uuuu
18Ch	EECON1	EEPGD	_	—	_	WRERR	WREN	WR	RD	x x000	x u000
18Dh	EECON2	EEPROM Control Register2 (not a physical register)							_	-	
8Dh	PIE2	_	(1)	—	EEIE	BCLIE	—	—	CCP2IE	-r-0 00	-r-0 00
0Dh	PIR2	—	(1)	_	EEIF	BCLIF	_	_	CCP2IF	-r-0 00	-r-0 00

Legend: x = unknown, u = unchanged, r = reserved, - = unimplemented, read as '0'. Shaded cells are not used during FLASH/EEPROM access.

Note 1: These bits are reserved; always maintain these bits clear.

9.0 MASTER SYNCHRONOUS SERIAL PORT (MSSP) MODULE

The Master Synchronous Serial Port (MSSP) module is a serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D converters, etc. The MSSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I²C)

Figure 9-1 shows a block diagram for the SPI mode, while Figure 9-5 and Figure 9-9 show the block diagrams for the two different I^2C modes of operation.

The Application Note AN734, "Using the PIC[®] MCU SSP for Slave I²CTM Communication" describes the slave operation of the MSSP module on the PIC16F87X devices. AN735, "Using the PIC[®] MCU MSSP Module for I²CTM Communications" describes the master operation of the MSSP module on the PIC16F87X devices.

Status Bi Transfer i	its as Data s Received	$SSPSR \to SSPBUF$	Generate ACK Pulse	Set bit SSPIF (SSP Interrupt occurs if enabled)		
BF	SSPOV					
0	0	Yes	Yes	Yes		
1	0	No	No	Yes		
1	1	No	No	Yes		
0	1	Yes	No	Yes		

TABLE 9-2: DATA TRANSFER RECEIVED BYTE ACTIONS

Note: Shaded cells show the conditions where the user software did not properly clear the overflow condition.

9.2.1.3 Slave Transmission

When the R/W bit of the incoming address byte is set and an address match occurs, the R/W bit of the SSPSTAT register is set. The received address is loaded into the SSPBUF register. The ACK pulse will be sent on the ninth bit, and the SCL pin is held low. The transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then, the SCL pin should be enabled by setting bit CKP (SSPCON<4>). The master must monitor the SCL pin prior to asserting another clock pulse. The slave devices may be holding off the master by stretching the clock. The eight data bits are shifted out on the falling edge of the SCL input. This ensures that the SDA signal is valid during the SCL high time (Figure 9-7). An SSP interrupt is generated for each data transfer byte. The SSPIF flag bit must be cleared in software and the SSPSTAT register is used to determine the status of the byte transfer. The SSPIF flag bit is set on the falling edge of the ninth clock pulse.

As a slave-transmitter, the \overline{ACK} pulse from the master receiver is latched on the rising edge of the ninth SCL input pulse. If the SDA line is high (not \overline{ACK}), then the data transfer is complete. When the not \overline{ACK} is latched by the slave, the slave logic is reset and the slave then monitors for another occurrence of the START bit. If the SDA line was low (\overline{ACK}), the transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then the SCL pin should be enabled by setting the CKP bit.



9.2.11 I²C MASTER MODE TRANSMISSION

Transmission of a data byte, a 7-bit address, or either half of a 10-bit address, is accomplished by simply writing a value to SSPBUF register. This action will set the Buffer Full flag (BF) and allow the baud rate generator to begin counting and start the next transmission. Each bit of address/data will be shifted out onto the SDA pin after the falling edge of SCL is asserted (see data hold time spec). SCL is held low for one baud rate generator rollover count (TBRG). Data should be valid before SCL is released high (see data setup time spec). When the SCL pin is released high, it is held that way for TBRG. The data on the SDA pin must remain stable for that duration and some hold time after the next falling edge of SCL. After the eighth bit is shifted out (the falling edge of the eighth clock), the BF flag is cleared and the master releases SDA allowing the slave device being addressed to respond with an ACK bit during the ninth bit time, if an address match occurs or if data was received properly. The status of ACK is read into the ACKDT on the falling edge of the ninth clock. If the master receives an Acknowledge, the Acknowledge Status bit (ACKSTAT) is cleared. If not, the bit is set. After the ninth clock, the SSPIF is set and the master clock (baud rate generator) is suspended until the next data byte is loaded into the SSPBUF, leaving SCL low and SDA unchanged (Figure 9-14).

After the write to the SSPBUF, each bit of address will be shifted out on the falling edge of SCL, until all seven address bits and the R/W bit are completed. On the falling edge of the eighth clock, the master will de-assert the SDA pin, allowing the slave to respond with an Acknowledge. On the falling edge of the ninth clock, the master will sample the SDA pin to see if the address was recognized by a slave. The status of the ACK bit is loaded into the ACKSTAT status bit (SSPCON2<6>). Following the falling edge of the ninth clock transmission of the address, the SSPIF is set, the BF flag is cleared, and the baud rate generator is turned off until another write to the SSPBUF takes place, holding SCL low and allowing SDA to float.

9.2.11.1 BF Status Flag

In Transmit mode, the BF bit (SSPSTAT<0>) is set when the CPU writes to SSPBUF and is cleared when all 8 bits are shifted out.

9.2.11.2 WCOL Status Flag

If the user writes the SSPBUF when a transmit is already in progress (i.e., SSPSR is still shifting out a data byte), then WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

WCOL must be cleared in software.

9.2.11.3 ACKSTAT Status Flag

In Transmit mode, the ACKSTAT bit (SSPCON2<6>) is cleared when the slave has sent an Acknowledge $(\overline{ACK} = 0)$, and is set when the slave does not Acknowledge ($\overline{ACK} = 1$). A slave sends an Acknowledge when it has recognized its address (including a general call), or when the slave has properly received its data.

9.2.13 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled by setting the Acknowledge Sequence Enable bit, ACKEN (SSPCON2<4>). When this bit is set, the SCL pin is pulled low and the contents of the Acknowledge data bit is presented on the SDA pin. If the user wishes to generate an Acknowledge, the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The baud rate generator then counts for one rollover period (TBRG), and the SCL pin is de-asserted high. When the SCL pin is sampled high (clock arbitration), the baud rate generator counts for TBRG. The SCL pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the baud rate generator is turned off, and the SSP module then goes into IDLE mode (Figure 9-16).

9.2.13.1 WCOL Status Flag

If the user writes the SSPBUF when an Acknowledge sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).



FIGURE 9-16: ACKNOWLEDGE SEQUENCE WAVEFORM

TABLE 13-2: PIC16F87X INSTRUCTION SET

Mner	Mnemonic, Description		Cycles	14-Bit Op)	Status	Notoc
Operands		Description		MSb			LSb	Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	lfff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	С	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	С	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
		BIT-ORIENTED FILE REGIST		ATION	IS				
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
		LITERAL AND CONTROL	OPERAT	IONS					r
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	TO,PD	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into standby mode	1	00	0000	0110	0011	TO,PD	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	
Note 1: When an I/O register is modified as a function of itself (e.g., MOVF PORTE, 1), the value used will be that value present									

 When an I/O register is modified as a function of itself (e.g., MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.

3: If Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

Note: Additional information on the mid-range instruction set is available in the PIC[®] MCU Mid-Range Family Reference Manual (DS33023).

14.13 PICDEM 3 Low Cost PIC16CXXX Demonstration Board

The PICDEM 3 demonstration board is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with an LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 3 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer with an adapter socket, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 3 demonstration board to test firmware. A prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM 3 demonstration board is a LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM 3 demonstration board provides an additional RS-232 interface and Windows software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

14.14 PICDEM 17 Demonstration Board

The PICDEM 17 demonstration board is an evaluation board that demonstrates the capabilities of several Microchip microcontrollers, including PIC17C752, PIC17C756A, PIC17C762 and PIC17C766. All necessary hardware is included to run basic demo programs, which are supplied on a 3.5-inch disk. A programmed sample is included and the user may erase it and program it with the other sample programs using the PRO MATE II device programmer, or the PICSTART Plus development programmer, and easily debug and test the sample code. In addition, the PICDEM 17 demonstration board supports downloading of programs to and executing out of external FLASH memory on board. The PICDEM 17 demonstration board is also usable with the MPLAB ICE in-circuit emulator, or the PICMASTER emulator and all of the sample programs can be run and modified using either emulator. Additionally, a generous prototype area is available for user hardware.

14.15 KEELOQ Evaluation and Programming Tools

KEELOQ evaluation and programming tools support Microchip's HCS Secure Data Products. The HCS evaluation kit includes a LCD display to show changing codes, a decoder to decode transmissions and a programming interface to program test transmitters.

15.0 ELECTRICAL CHARACTERISTICS

Absolute	Maximum	Ratings	t

Ambient temperature under bias	55 to +125°C
Storage temperature	65°C to +150°C
Voltage on any pin with respect to Vss (except VDD, MCLR. and RA4)	0.3 V to (VDD + 0.3 V)
Voltage on VDD with respect to Vss	0.3 to +7.5 V
Voltage on MCLR with respect to Vss (Note 2)	0 to +14 V
Voltage on RA4 with respect to Vss	0 to +8.5 V
Total power dissipation (Note 1)	1.0 W
Maximum current out of Vss pin	300 mA
Maximum current into VDD pin	250 mA
Input clamp current, Iικ (VI < 0 or VI > VDD)	± 20 mA
Output clamp current, Ioк (Vo < 0 or Vo > VDD)	± 20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by PORTA, PORTB, and PORTE (combined) (Note 3)	200 mA
Maximum current sourced by PORTA, PORTB, and PORTE (combined) (Note 3)	200 mA
Maximum current sunk by PORTC and PORTD (combined) (Note 3)	200 mA
Maximum current sourced by PORTC and PORTD (combined) (Note 3)	200 mA
Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - \sum IOH} + \sum {(VDD -	VOH) x IOH} + Σ (VOI x IOL)
2: Voltage spikes below Vss at the \overline{MCLR} pin, inducing currents greater than 80	mA, may cause latch-up.

- 2: Voltage spikes below VSS at the MCLR pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the MCLR pin, rather than pulling this pin directly to VSS.
- 3: PORTD and PORTE are not implemented on PIC16F873/876 devices.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

15.3 DC Characteristics: PIC16F873/874/876/877-04 (Extended) PIC16F873/874/876/877-10 (Extended)

PIC16F873/874/876/877-04 PIC16F873/874/876/877-20 (Extended)				Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +125^{\circ}C$					
Param No.	Symbol	Characteristic/ Device	Min Typ† Max Units Conditions						
	Vdd	Supply Voltage							
D001			4.0	—	5.5	V	LP, XT, RC osc configuration		
D001A			4.5		5.5	V	HS osc configuration		
D001A			VBOR		5.5	V	BOR enabled, FMAX = 10 MHz ⁽⁷⁾		
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾		1.5	_	V			
D003	VPOR	VDD Start Voltage to ensure internal Power-on Reset signal	_	Vss	—	V	See section on Power-on Reset for details		
D004	Svdd	VDD Rise Rate to ensure internal Power-on Reset signal	0.05			V/ms	See section on Power-on Reset for details		
D005	VBOR	Brown-out Reset Voltage	3.7	4.0	4.35	V	BODEN bit in configuration word enabled		

† Data is "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading, switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD;

MCLR = VDD; WDT enabled/disabled as specified.

- 3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.
- **4:** For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kOhm.
- **5:** Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.
- 6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.
- 7: When BOR is enabled, the device will operate correctly until the VBOR voltage trip point is reached.

15.4 DC Characteristics: PIC16F873/874/876/877-04 (Extended) PIC16F873/874/876/877-10 (Extended) (Continued)

DC CHA	C CHARACTERISTICS Standard Operating Conditions (unless otherwise stores of the conditions) C CHARACTERISTICS Operating temperature -40°C ≤ TA ≤ +125°C Operating voltage VDD range as described in DC specific (Section 15.1)					TA \leq +125°C described in DC specification			
Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions		
	Vol	Output Low Voltage							
D080A		I/O ports		—	0.6	V	IOL = 7.0 mA, VDD = 4.5V		
D083A		OSC2/CLKOUT (RC osc config)	—	—	0.6	V	IOL = 1.2 mA, VDD = 4.5V		
	Voн	Output High Voltage							
D090A		I/O ports ⁽³⁾	VDD - 0.7	_	_	V	Юн = -2.5 mA, VDD = 4.5V		
D092A		OSC2/CLKOUT (RC osc config)	Vdd - 0.7	—	_	V	IOH = -1.0 mA, VDD = 4.5V		
D150*	Vod	Open Drain High Voltage	—	—	8.5	V	RA4 pin		
		Capacitive Loading Specs on C	utput Pins	5					
D100	Cosc2	OSC2 pin	_		15	pF	In XT, HS and LP modes when external clock is used to drive OSC1		
D101	Сю	All I/O pins and OSC2 (RC mode)		_	50	pF			
D102	Св	SCL, SDA (I ² C mode)	—	—	400	pF			
		Data EEPROM Memory							
D120	ED	Endurance	100K		_	E/W	25°C at 5V		
D121	Vdrw	VDD for read/write	VMIN		5.5	V	Using EECON to read/write VMIN = min. operating voltage		
D122	TDEW	Erase/write cycle time	—	4	8	ms			
		Program FLASH Memory							
D130	Eр	Endurance	1000		_	E/W	25°C at 5V		
D131	Vpr	VDD for read	VMIN	—	5.5	V	VMIN = min operating voltage		
D132A		VDD for erase/write	VMIN		5.5	V	Using EECON to read/write, VMIN = min. operating voltage		
D133	TPEW	Erase/Write cycle time	—	4	8	ms			

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16F87X be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

PIC16F87X





FIGURE 16-8: AVERAGE FOSC vs. VDD FOR VARIOUS VALUES OF R (RC MODE, C = 100 pF, 25° C)



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FIGURE 16-21: MINIMUM AND MAXIMUM VIN vs. VDD (ST INPUT, -40°C TO 125°C)





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