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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf874-04-p

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8.2 Compare Mode

In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the RC2/CCP1 pin is:

- Driven high
- Driven low
- Remains unchanged

The action on the pin is based on the value of control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). At the same time, interrupt flag bit CCP1IF is set.

FIGURE 8-2: COMPARE MODE OPERATION BLOCK DIAGRAM



8.2.1 CCP PIN CONFIGURATION

The user must configure the RC2/CCP1 pin as an output by clearing the TRISC<2> bit.

Note: Clearing the CCP1CON register will force the RC2/CCP1 compare output latch to the default low level. This is not the PORTC I/O data latch.

8.2.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode, or Synchronized Counter mode, if the CCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

8.2.3 SOFTWARE INTERRUPT MODE

When Generate Software Interrupt mode is chosen, the CCP1 pin is not affected. The CCPIF bit is set, causing a CCP interrupt (if enabled).

8.2.4 SPECIAL EVENT TRIGGER

In this mode, an internal hardware trigger is generated, which may be used to initiate an action.

The special event trigger output of CCP1 resets the TMR1 register pair. This allows the CCPR1 register to effectively be a 16-bit programmable period register for Timer1.

The special event trigger output of CCP2 resets the TMR1 register pair and starts an A/D conversion (if the A/D module is enabled).

Note: The special event trigger from the CCP1and CCP2 modules will not set interrupt flag bit TMR1IF (PIR1<0>).

PIC16F87X

8.3.3 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

- 1. Set the PWM period by writing to the PR2 register.
- 2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON<5:4> bits.
- 3. Make the CCP1 pin an output by clearing the TRISC<2> bit.
- 4. Set the TMR2 prescale value and enable Timer2 by writing to T2CON.
- 5. Configure the CCP1 module for PWM operation.

TABLE 8-3: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 20 MHz

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12kHz	156.3 kHz	208.3 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFFh	0xFFh	0xFFh	0x3Fh	0x1Fh	0x17h
Maximum Resolution (bits)	10	10	10	8	7	5.5

TABLE 8-4: REGISTERS ASSOCIATED WITH CAPTURE, COMPARE, AND TIMER1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value PC BC	e on: DR, DR	Valu all o RES	e on other SETS
0Bh,8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000	000x	0000	000u
0Ch	PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000	0000	0000
0Dh	PIR2	—	_	—	—	—	—	—	CCP2IF		0		0
8Ch	PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000	0000	0000
8Dh	PIE2	—	—	—	_	—	-	—	CCP2IE		0		0
87h	TRISC	PORTC D	PORTC Data Direction Register								1111	1111	1111
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx	xxxx	uuuu	uuuu
0Fh	TMR1H	Holding R	egister fo	r the Most S	Significant B	yte of the 16	6-bit TMR1	Register		xxxx	xxxx	uuuu	uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00	0000	uu	uuuu
15h	CCPR1L	Capture/C	Capture/Compare/PWM Register1 (LSB)								xxxx	uuuu	uuuu
16h	CCPR1H	Capture/Compare/PWM Register1 (MSB)							xxxx	xxxx	uuuu	uuuu	
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00	0000	00	0000
1Bh	CCPR2L	Capture/Compare/PWM Register2 (LSB)								xxxx	xxxx	uuuu	uuuu
1Ch	CCPR2H	Capture/Compare/PWM Register2 (MSB)								uuuu	uuuu		
1Dh	CCP2CON		_	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00	0000	00	0000

 $\label{eq:legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by Capture and Timer1.$

Note 1: The PSP is not implemented on the PIC16F873/876; always maintain these bits clear.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value PC BC	e on:)R,)R	Valu all o RES	e on ther ETS
0Bh,8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000	000x	0000	000u
0Ch	PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000	0000	0000
0Dh	PIR2	—	—	_	—	—	_	—	CCP2IF		0		0
8Ch	PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000	0000	0000
8Dh	PIE2	—	—	_	_	—	_	—	CCP2IE		0		0
87h	TRISC	PORTC D	PORTC Data Direction Register								1111	1111	1111
11h	TMR2	Timer2 Module's Register								0000	0000	0000	0000
92h	PR2	Timer2 M	odule's Perio	od Register						1111	1111	1111	1111
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000	0000	-000	0000
15h	CCPR1L	Capture/Compare/PWM Register1 (LSB)								xxxx	xxxx	uuuu	uuuu
16h	CCPR1H	Capture/Compare/PWM Register1 (MSB)								xxxx	xxxx	uuuu	uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00	0000	00	0000
1Bh	CCPR2L	Capture/Compare/PWM Register2 (LSB)								xxxx	xxxx	uuuu	uuuu
1Ch	CCPR2H	Capture/Compare/PWM Register2 (MSB)								xxxx	xxxx	uuuu	uuuu
1Dh	CCP2CON	—		CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00	0000	00	0000

|--|

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PWM and Timer2. Note 1: Bits PSPIE and PSPIF are reserved on the PIC16F873/876; always maintain these bits clear.

Status Bits as Data Transfer is Received		$SSPSR \to SSPBUF$	Generate ACK Pulse	Set bit SSPIF (SSP Interrupt occurs		
BF	SSPOV			if enabled)		
0	0	Yes	Yes	Yes		
1	0	No	No	Yes		
1	1	No	No	Yes		
0	1	Yes	No	Yes		

TABLE 9-2: DATA TRANSFER RECEIVED BYTE ACTIONS

Note: Shaded cells show the conditions where the user software did not properly clear the overflow condition.

9.2.1.3 Slave Transmission

When the R/W bit of the incoming address byte is set and an address match occurs, the R/W bit of the SSPSTAT register is set. The received address is loaded into the SSPBUF register. The ACK pulse will be sent on the ninth bit, and the SCL pin is held low. The transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then, the SCL pin should be enabled by setting bit CKP (SSPCON<4>). The master must monitor the SCL pin prior to asserting another clock pulse. The slave devices may be holding off the master by stretching the clock. The eight data bits are shifted out on the falling edge of the SCL input. This ensures that the SDA signal is valid during the SCL high time (Figure 9-7). An SSP interrupt is generated for each data transfer byte. The SSPIF flag bit must be cleared in software and the SSPSTAT register is used to determine the status of the byte transfer. The SSPIF flag bit is set on the falling edge of the ninth clock pulse.

As a slave-transmitter, the \overline{ACK} pulse from the master receiver is latched on the rising edge of the ninth SCL input pulse. If the SDA line is high (not \overline{ACK}), then the data transfer is complete. When the not \overline{ACK} is latched by the slave, the slave logic is reset and the slave then monitors for another occurrence of the START bit. If the SDA line was low (\overline{ACK}), the transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then the SCL pin should be enabled by setting the CKP bit.



9.2.7 I²C MASTER MODE SUPPORT

Master mode is enabled by setting and clearing the appropriate SSPM bits in SSPCON and by setting the SSPEN bit. Once Master mode is enabled, the user has six options:

- Assert a START condition on SDA and SCL.
- Assert a Repeated START condition on SDA and SCL.
- Write to the SSPBUF register initiating transmission of data/address.
- Generate a STOP condition on SDA and SCL.
- Configure the I²C port to receive data.
- Generate an Acknowledge condition at the end of a received byte of data.
- Note: The MSSP Module, when configured in I²C Master mode, does not allow queueing of events. For instance, the user is not allowed to initiate a START condition and immediately write the SSPBUF register to initiate transmission before the START condition is complete. In this case, the SSPBUF will not be written to and the WCOL bit will be set, indicating that a write to the SSPBUF did not occur.

9.2.7.1 I²C Master Mode Operation

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a Repeated START condition. Since the Repeated START condition is also the beginning of the next serial transfer, the l^2C bus will not be released.

In Master Transmitter mode, serial data is output through SDA, while SCL outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (7 bits) and the Read/Write (R/W) bit. In this case, the R/W bit will be logic '0'. Serial data is transmitted 8 bits at a time. After each byte is transmitted, an Acknowledge bit is received. START and STOP conditions are output to indicate the beginning and the end of a serial transfer.

In Master Receive mode, the first byte transmitted contains the slave address of the transmitting device (7 bits) and the R/W bit. In this case, the R/W bit will be logic '1'. Thus, the first byte transmitted is a 7-bit slave address followed by a '1' to indicate receive bit. Serial data is received via SDA, while SCL outputs the serial clock. Serial data is received 8 bits at a time. After each byte is received, an Acknowledge bit is transmitted. START and STOP conditions indicate the beginning and end of transmission.

The baud rate generator used for SPI mode operation is now used to set the SCL clock frequency for either 100 kHz, 400 kHz, or 1 MHz I²C operation. The baud rate generator reload value is contained in the lower 7 bits of the SSPADD register. The baud rate generator will automatically begin counting on a write to the SSPBUF. Once the given operation is complete (i.e., transmission of the last data bit is followed by ACK), the internal clock will automatically stop counting and the SCL pin will remain in its last state.

A typical transmit sequence would go as follows:

- a) User generates a START condition by setting the START enable bit (SEN) in SSPCON2.
- b) SSPIF is set. The module will wait the required start time before any other operation takes place.
- c) User loads SSPBUF with address to transmit.
- d) Address is shifted out the SDA pin until all 8 bits are transmitted.
- e) MSSP module shifts in the ACK bit from the slave device and writes its value into the SSPCON2 register (SSPCON2<6>).
- f) MSSP module generates an interrupt at the end of the ninth clock cycle by setting SSPIF.
- g) User loads SSPBUF with eight bits of data.
- h) DATA is shifted out the SDA pin until all 8 bits are transmitted.
- MSSP module shifts in the ACK bit from the slave device, and writes its value into the SSPCON2 register (SSPCON2<6>).
- MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSPIF bit.
- k) User generates a STOP condition by setting the STOP enable bit, PEN, in SSPCON2.
- I) Interrupt is generated once the STOP condition is complete.

9.2.8 BAUD RATE GENERATOR

In I^2C Master mode, the reload value for the BRG is located in the lower 7 bits of the SSPADD register (Figure 9-10). When the BRG is loaded with this value, the BRG counts down to 0 and stops until another reload has taken place. The BRG count is decremented twice per instruction cycle (Tcr), on the Q2 and Q4 clock.

In I²C Master mode, the BRG is reloaded automatically. If clock arbitration is taking place, the BRG will be reloaded when the SCL pin is sampled high (Figure 9-11).

Note: Baud Rate = Fosc / (4 * (SSPADD + 1))

FIGURE 9-10:

BAUD RATE GENERATOR BLOCK DIAGRAM





9.2.15 CLOCK ARBITRATION

Clock arbitration occurs when the master, during any receive, transmit, or Repeated START/STOP condition, de-asserts the SCL pin (SCL allowed to float high). When the SCL pin is allowed to float high, the baud rate generator (BRG) is suspended from counting until the SCL pin is actually sampled high. When the SCL pin is sampled high, the baud rate generator is reloaded with the contents of SSPADD<6:0> and begins counting. This ensures that the SCL high time will always be at least one BRG rollover count in the event that the clock is held low by an external device (Figure 9-18).

9.2.16 SLEEP OPERATION

While in SLEEP mode, the I²C module can receive addresses or data, and when an address match or complete byte transfer occurs, wake the processor from SLEEP (if the SSP interrupt is enabled).

9.2.17 EFFECTS OF A RESET

A RESET disables the SSP module and terminates the current transfer.

FIGURE 9-18: CLOCK ARBITRATION TIMING IN MASTER TRANSMIT MODE



9.2.18.2 Bus Collision During a Repeated START Condition

During a Repeated START condition, a bus collision occurs if:

- a) A low level is sampled on SDA when SCL goes from low level to high level.
- b) SCL goes low before SDA is asserted low, indicating that another master is attempting to transmit a data '1'.

When the user de-asserts SDA and the pin is allowed to float high, the BRG is loaded with SSPADD<6:0> and counts down to 0. The SCL pin is then de-asserted, and when sampled high, the SDA pin is sampled. If SDA is low, a bus collision has occurred (i.e., another master is attempting to transmit a data'0'). If, however,

SDA is sampled high, the BRG is reloaded and begins counting. If SDA goes from high to low before the BRG times out, no bus collision occurs, because no two masters can assert SDA at exactly the same time.

If, however, SCL goes from high to low before the BRG times out and SDA has not already been asserted, a bus collision occurs. In this case, another master is attempting to transmit a data'1' during the Repeated START condition.

If at the end of the BRG time-out, both SCL and SDA are still high, the SDA pin is driven low, the BRG is reloaded and begins counting. At the end of the count, regardless of the status of the SCL pin, the SCL pin is driven low and the Repeated START condition is complete (Figure 9-23).

FIGURE 9-23: BUS COLLISION DURING A REPEATED START CONDITION (CASE 1)



FIGURE 9-24: BUS COLLISION DURING REPEATED START CONDITION (CASE 2)



10.2.2 USART ASYNCHRONOUS RECEIVER

The receiver block diagram is shown in Figure 10-4. The data is received on the RC7/RX/DT pin and drives the data recovery block. The data recovery block is actually a high speed shifter, operating at x16 times the baud rate; whereas, the main receive serial shifter operates at the bit rate or at Fosc.

Once Asynchronous mode is selected, reception is enabled by setting bit CREN (RCSTA<4>).

The heart of the receiver is the receive (serial) shift register (RSR). After sampling the STOP bit, the received data in the RSR is transferred to the RCREG register (if it is empty). If the transfer is complete, flag bit RCIF (PIR1<5>) is set. The actual interrupt can be enabled/ disabled by setting/clearing enable bit RCIE (PIE1<5>). Flag bit RCIF is a read only bit, which is cleared by the hardware. It is cleared when the RCREG register has been read and is empty. The RCREG is a double buffered register (i.e., it is a two deep FIFO). It is possible for two bytes of data to be received and transferred to the RCREG FIFO and a third byte to begin shifting to the RSR register. On the detection of the STOP bit of the third byte, if the RCREG register is still full, the overrun error bit OERR (RCSTA<1>) will be set. The word in the RSR will be lost. The RCREG register can be read twice to retrieve the two bytes in the FIFO. Overrun bit OERR has to be cleared in software. This is done by resetting the receive logic (CREN is cleared and then set). If bit OERR is set, transfers from the RSR register to the RCREG register are inhibited, and no further data will be received. It is therefore, essential to clear error bit OERR if it is set. Framing error bit FERR (RCSTA<2>) is set if a STOP bit is detected as clear. Bit FERR and the 9th receive bit are buffered the same way as the receive data. Reading the RCREG will load bits RX9D and FERR with new values, therefore, it is essential for the user to read the RCSTA register before reading the RCREG register in order not to lose the old FERR and RX9D information.





12.12 Watchdog Timer (WDT)

The Watchdog Timer is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run, even if the clock on the OSC1/CLKIN and OSC2/ CLKOUT pins of the device has been stopped, for example, by execution of a SLEEP instruction.

During normal operation, a WDT time-out generates a device RESET (Watchdog Timer Reset). If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation (Watchdog Timer Wake-up). The TO bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

The WDT can be permanently disabled by clearing configuration bit WDTE (Section 12.1).

WDT time-out period values may be found in the Electrical Specifications section under parameter #31. Values for the WDT prescaler (actually a postscaler, but shared with the Timer0 prescaler) may be assigned using the OPTION_REG register.

- Note 1: The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.
 - 2: When a CLRWDT instruction is executed and the prescaler is assigned to the WDT, the prescaler count will be cleared, but the prescaler assignment is not changed.



FIGURE 12-10: WATCHDOG TIMER BLOCK DIAGRAM

TABLE 12-7: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. bits	(1)	BODEN ⁽¹⁾	CP1	CP0	PWRTE ⁽¹⁾	WDTE	FOSC1	FOSC0
81h,181h	OPTION_REG	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0

Legend: Shaded cells are not used by the Watchdog Timer. **Note 1:** See Register 12-1 for operation of these bits.

	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1		Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4
OSC1	·/~~~~/			-		<u>;</u> ~~~~~~		
CLKOUT ⁽⁴⁾	\/\		<u> </u>	Tost(2)	/	\	¦/ \	
INT pin	· · ·	1		· ·		1 1	1 I 1 I	
INTF Flag (INTCON<1>)		י י י י	Ĺ	/		Interrupt Latency	(2)	
GIE bit (INTCON<7>)	1 I 1 I 1 I 1 I	i 	Processor i	n		·	1 1 1 1 1 1	ו ו ו ו
INSTRUCTIO	N FLOW			· ·		1	1 1 1 1	1
PC	Х РС Х	PC+1	ХР	C+2	PC+2	X PC + 2	<u>X 0004h X</u>	0005h
Instruction { Fetched {	Inst(PC) = SLEEP	Inst(PC + 1)		1	Inst(PC + 2)	1 1 1	Inst(0004h)	Inst(0005h)
Instruction	Inst(PC - 1)	SLEEP		, , ,	Inst(PC + 1)	Dummy cycle	Dummy cycle	Inst(0004h)
Note 1: XT, 1 2: Tos	HS or LP oscillator n r = 1024Tosc (drawi	node assumed. ing not to scale)	This delay v	vill not be th	here for RC osc n	node.		

F

If GIE = '0', execution will continue in-line.

4: CLKOUT is not available in these osc modes, but shown here for timing reference.

12.14 In-Circuit Debugger

When the DEBUG bit in the configuration word is programmed to a '0', the In-Circuit Debugger functionality is enabled. This function allows simple debugging functions when used with MPLAB® ICD. When the microcontroller has this feature enabled, some of the resources are not available for general use. Table 12-8 shows which features are consumed by the background debugger.

I/O pins	RB6, RB7
Stack	1 level
Program Memory	Address 0000h must be NOP
	Last 100h words
Data Memory	0x070 (0x0F0, 0x170, 0x1F0) 0x1EB - 0x1EF

To use the In-Circuit Debugger function of the microcontroller, the design must implement In-Circuit Serial Programming connections to MCLR/VPP, VDD, GND, RB7 and RB6. This will interface to the In-Circuit Debugger module available from Microchip, or one of the third party development tool companies.

12.15 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

12.16 ID Locations

Four memory locations (2000h - 2003h) are designated as ID locations, where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution, but are readable and writable during program/verify. It is recommended that only the 4 Least Significant bits of the ID location are used.

DECFSZ	Decrement f, Skip if 0
Syntax:	[label] DECFSZ f,d
Operands:	$\begin{array}{l} 0\leq f\leq 127\\ d\in [0,1] \end{array}$
Operation:	(f) - 1 \rightarrow (destination); skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are decremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 1, the next instruction is executed. If the result is 0, then a NOP is executed instead making it a 2TCY instruction.

INCFSZ	Increment f, Skip if 0
Syntax:	[label] INCFSZ f,d
Operands:	$\begin{array}{l} 0\leq f\leq 127\\ d\in [0,1] \end{array}$
Operation:	(f) + 1 \rightarrow (destination), skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 1, the next instruc-
	tion is executed. If the result is 0, a NOP is executed instead, making it a 2TCY instruction.

GOTO	Unconditional Branch							
Syntax:	[<i>label</i>] GOTO k							
Operands:	$0 \leq k \leq 2047$							
Operation:	$k \rightarrow PC<10:0>$ PCLATH<4:3> \rightarrow PC<12:11>							
Status Affected:	None							
Description:	GOTO is an unconditional branch. The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two- cycle instruction.							

IORLW	Inclusive OR Literal with W
Syntax:	[<i>label</i>] IORLW k
Operands:	$0 \leq k \leq 255$
Operation:	(W) .OR. $k \rightarrow$ (W)
Status Affected:	Z
Description:	The contents of the W register are OR'ed with the eight bit literal 'k'. The result is placed in the W register.

INCF	Increment f	IORWF	Inclusive OR W with f
Syntax:	[<i>label</i>] INCF f,d	Syntax:	[label] IORWF f,d
Operands:	$0 \le f \le 127$ d $\in [0,1]$	Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$
Operation:	(f) + 1 \rightarrow (destination)	Operation:	(W) .OR. (f) \rightarrow (destination)
Status Affected:	Z	Status Affected:	Z
Description:	The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.	Description:	Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

14.0 DEVELOPMENT SUPPORT

The PIC[®] microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
 - MPLAB[®] IDE Software
- Assemblers/Compilers/Linkers
 - MPASM[™] Assembler
 - MPLAB C17 and MPLAB C18 C Compilers
 - MPLINK™ Object Linker/
 - MPLIB[™] Object Librarian
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB ICE 2000 In-Circuit Emulator
- ICEPIC[™] In-Circuit Emulator
- In-Circuit Debugger
 - MPLAB ICD for PIC16F87X
- Device Programmers
 - PRO MATE[®] II Universal Device Programmer
- PICSTART[®] Plus Entry-Level Development Programmer
- Low Cost Demonstration Boards
 - PICDEM[™]1 Demonstration Board
 - PICDEM 2 Demonstration Board
 - PICDEM 3 Demonstration Board
 - PICDEM 17 Demonstration Board
 - KEELOQ[®] Demonstration Board

14.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. The MPLAB IDE is a Windows[®]-based application that contains:

- An interface to debugging tools
 - simulator
 - programmer (sold separately)
 - emulator (sold separately)
 - in-circuit debugger (sold separately)
- A full-featured editor
- · A project manager
- Customizable toolbar and key mapping
- A status bar
- On-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
 - source files
 - absolute listing file
 - machine code

The ability to use MPLAB IDE with multiple debugging tools allows users to easily switch from the cost-effective simulator to a full-featured emulator with minimal retraining.

14.2 MPASM Assembler

The MPASM assembler is a full-featured universal macro assembler for all $\text{PIC}^{\textcircled{R}}$ MCUs.

The MPASM assembler has a command line interface and a Windows shell. It can be used as a stand-alone application on a Windows 3.x or greater system, or it can be used through MPLAB IDE. The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel[®] standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file that contains source lines and generated machine code, and a COD file for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects.
- User-defined macros to streamline assembly code.
- Conditional assembly for multi-purpose source files.
- Directives that allow complete control over the assembly process.

14.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI 'C' compilers for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

15.0 ELECTRICAL CHARACTERISTICS

Absolute	Maximum	Ratings	t

Ambient temperature under bias	55 to +125°C
Storage temperature	65°C to +150°C
Voltage on any pin with respect to Vss (except VDD, MCLR. and RA4)	0.3 V to (VDD + 0.3 V)
Voltage on VDD with respect to Vss	0.3 to +7.5 V
Voltage on MCLR with respect to Vss (Note 2)	0 to +14 V
Voltage on RA4 with respect to Vss	0 to +8.5 V
Total power dissipation (Note 1)	1.0 W
Maximum current out of Vss pin	300 mA
Maximum current into VDD pin	250 mA
Input clamp current, Iικ (VI < 0 or VI > VDD)	± 20 mA
Output clamp current, Ioк (Vo < 0 or Vo > VDD)	± 20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by PORTA, PORTB, and PORTE (combined) (Note 3)	200 mA
Maximum current sourced by PORTA, PORTB, and PORTE (combined) (Note 3)	200 mA
Maximum current sunk by PORTC and PORTD (combined) (Note 3)	200 mA
Maximum current sourced by PORTC and PORTD (combined) (Note 3)	200 mA
Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - \sum IOH} + \sum {(VDD -	VOH) x IOH} + Σ (VOI x IOL)
2: Voltage spikes below Vss at the \overline{MCLR} pin, inducing currents greater than 80	mA, may cause latch-up.

- 2: Voltage spikes below VSS at the MCLR pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the MCLR pin, rather than pulling this pin directly to VSS.
- 3: PORTD and PORTE are not implemented on PIC16F873/876 devices.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

15.2 DC Characteristics: PIC16F873/874/876/877-04 (Commercial, Industrial) PIC16F873/874/876/877-20 (Commercial, Industrial) PIC16LF873/874/876/877-04 (Commercial, Industrial)

			Standard Operating Conditions (unless otherwise stated)							
			Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial							
DC CHA	RACTER	RISTICS	$0^{\circ}C \le IA \le +70^{\circ}C$ for commercial							
			(Section 15.1)							
Daram				0.1)						
No.	Sym	Characteristic	Min Typ† Max Units Conditions				Conditions			
	VIL	Input Low Voltage								
		I/O ports								
D030		with TTL buffer	Vss	—	0.15Vdd	V	For entire VDD range			
D030A			Vss	—	0.8V	V	$4.5V \le VDD \le 5.5V$			
D031		with Schmitt Trigger buffer	Vss	—	0.2Vdd	V				
D032		MCLR, OSC1 (in RC mode)	Vss	—	0.2Vdd	V				
D033		OSC1 (in XT, HS and LP)	Vss	—	0.3Vdd	V	(Note 1)			
		Ports RC3 and RC4		—						
D034		with Schmitt Trigger buffer	Vss	—	0.3Vdd	V	For entire VDD range			
D034A		with SMBus	-0.5	—	0.6	V	for VDD = 4.5 to 5.5V			
	Vi∺ Input High Voltage									
		I/O ports								
D040		with TTL buffer	2.0	—	Vdd	V	$4.5V \leq V\text{DD} \leq 5.5V$			
D040A			0.25Vdd	—	Vdd	V	For entire VDD range			
			+ 0.8V							
D041		with Schmitt Trigger buffer	0.8Vdd	—	Vdd	V	For entire VDD range			
D042		MCLR	0.8Vdd	—	Vdd	V				
D042A		OSC1 (XT, HS and LP)	0.7Vdd	—	Vdd	V	(Note 1)			
D043		OSC1 (in RC mode)	0.9Vdd	—	Vdd	V				
		Ports RC3 and RC4								
D044		with Schmitt Trigger buffer	0.7Vdd	—	Vdd	V	For entire VDD range			
D044A		with SMBus	1.4	—	5.5	V	for $VDD = 4.5$ to $5.5V$			
D070	IPURB	PORTB Weak Pull-up Current	50	250	400	μA	VDD = 5V, VPIN = VSS,			
	Lo.	(0, 0)					-40°C TO +85°C			
	IIL	Input Leakage Current ^(2, 3)								
D060		I/O ports	—	—	±1	μA	$Vss \leq VPIN \leq VDD,$			
							Pin at hi-impedance			
D061		MCLR, RA4/T0CKI	—	—	±5	μA	$VSS \leq VPIN \leq VDD$			
D063		OSC1	—	—	±5	μA	$Vss \le VPIN \le VDD, XT, HS$			
	-						and LP osc configuration			

These parameters are characterized but not tested.

Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance † only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16F87X be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

15.3 DC Characteristics: PIC16F873/874/876/877-04 (Extended) PIC16F873/874/876/877-10 (Extended)

PIC16F873/874/876/877-04 PIC16F873/874/876/877-20 (Extended)				Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +125^{\circ}C$						
Param No.	Symbol	Characteristic/ Device	Min Typ† Max Units Conditions							
	Vdd	Supply Voltage								
D001			4.0	—	5.5	V	LP, XT, RC osc configuration			
D001A			4.5		5.5	V	HS osc configuration			
D001A			VBOR		5.5	V	BOR enabled, FMAX = 10 MHz ⁽⁷⁾			
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾		1.5	_	V				
D003	VPOR	VDD Start Voltage to ensure internal Power-on Reset signal	_	Vss	—	V	See section on Power-on Reset for details			
D004	Svdd	VDD Rise Rate to ensure internal Power-on Reset signal	0.05			V/ms	See section on Power-on Reset for details			
D005	VBOR	Brown-out Reset Voltage	3.7	4.0	4.35	V	BODEN bit in configuration word enabled			

† Data is "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading, switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD;

MCLR = VDD; WDT enabled/disabled as specified.

- 3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.
- **4:** For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kOhm.
- **5:** Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.
- 6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.
- 7: When BOR is enabled, the device will operate correctly until the VBOR voltage trip point is reached.



TABLE 15-6: PARALLEL SLAVE PORT REQUIREMENTS (PIC16F874/877 ONLY)

Parameter No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions	
62	TdtV2wrH	Data in valid before WR↑ or CS↑ (setup ti	20 25		_	ns ns	Extended Range Only	
63*	TwrH2dtl	$\overline{\text{WR}}^{\uparrow}$ or $\overline{\text{CS}}^{\uparrow}$ to data–in invalid (hold time)	Standard(F)	20	_	—	ns	
			Extended(LF)		—		ns	
64	TrdL2dtV	$\overline{RD}\downarrow$ and $\overline{CS}\downarrow$ to data–out valid	↓ and \overline{CS} ↓ to data–out valid			80 90	ns ns	Extended Range Only
65	TrdH2dtI	RD↑ or CS↓ to data–out invalid		10	_	30	ns	

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.







28-Lead Skinny Plastic Dual In-line (SP) – 300 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES*		MILLIMETERS			
Dimension I	_imits	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		28			28		
Pitch	р		.100			2.54		
Top to Seating Plane	А	.140	.150	.160	3.56	3.81	4.06	
Molded Package Thickness	A2	.125	.130	.135	3.18	3.30	3.43	
Base to Seating Plane	A1	.015			0.38			
Shoulder to Shoulder Width	Е	.300	.310	.325	7.62	7.87	8.26	
Molded Package Width	E1	.275	.285	.295	6.99	7.24	7.49	
Overall Length	D	1.345	1.365	1.385	34.16	34.67	35.18	
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43	
Lead Thickness	С	.008	.012	.015	0.20	0.29	0.38	
Upper Lead Width	B1	.040	.053	.065	1.02	1.33	1.65	
Lower Lead Width	В	.016	.019	.022	0.41	0.48	0.56	
Overall Row Spacing §	eB	.320	.350	.430	8.13	8.89	10.92	
Mold Draft Angle Top	α	5	10	15	5	10	15	
Mold Draft Angle Bottom	β	5	10	15	5	10	15	

* Controlling Parameter § Significant Characteristic

Dimension D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed

.010" (0.254mm) per side. JEDEC Equivalent: MO-095

Drawing No. C04-070

Notes:

44-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 1.0/0.10 mm Lead Form (TQFP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



		INCHES		MILLIMETERS*			
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		44			44	
Pitch	р		.031			0.80	
Pins per Side	n1		11			11	
Overall Height	Α	.039	.043	.047	1.00	1.10	1.20
Molded Package Thickness	A2	.037	.039	.041	0.95	1.00	1.05
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Foot Length	L	.018	.024	.030	0.45	0.60	0.75
Footprint (Reference)	(F)		.039		1.00		
Foot Angle	¢	0	3.5	7	0	3.5	7
Overall Width	E	.463	.472	.482	11.75	12.00	12.25
Overall Length	D	.463	.472	.482	11.75	12.00	12.25
Molded Package Width	E1	.390	.394	.398	9.90	10.00	10.10
Molded Package Length	D1	.390	.394	.398	9.90	10.00	10.10
Lead Thickness	С	.004	.006	.008	0.09	0.15	0.20
Lead Width	В	.012	.015	.017	0.30	0.38	0.44
Pin 1 Corner Chamfer	СН	.025	.035	.045	0.64	0.89	1.14
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-026 Drawing No. C04-076