



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16lf874t-04i-pt">https://www.e-xfl.com/product-detail/microchip-technology/pic16lf874t-04i-pt</a>

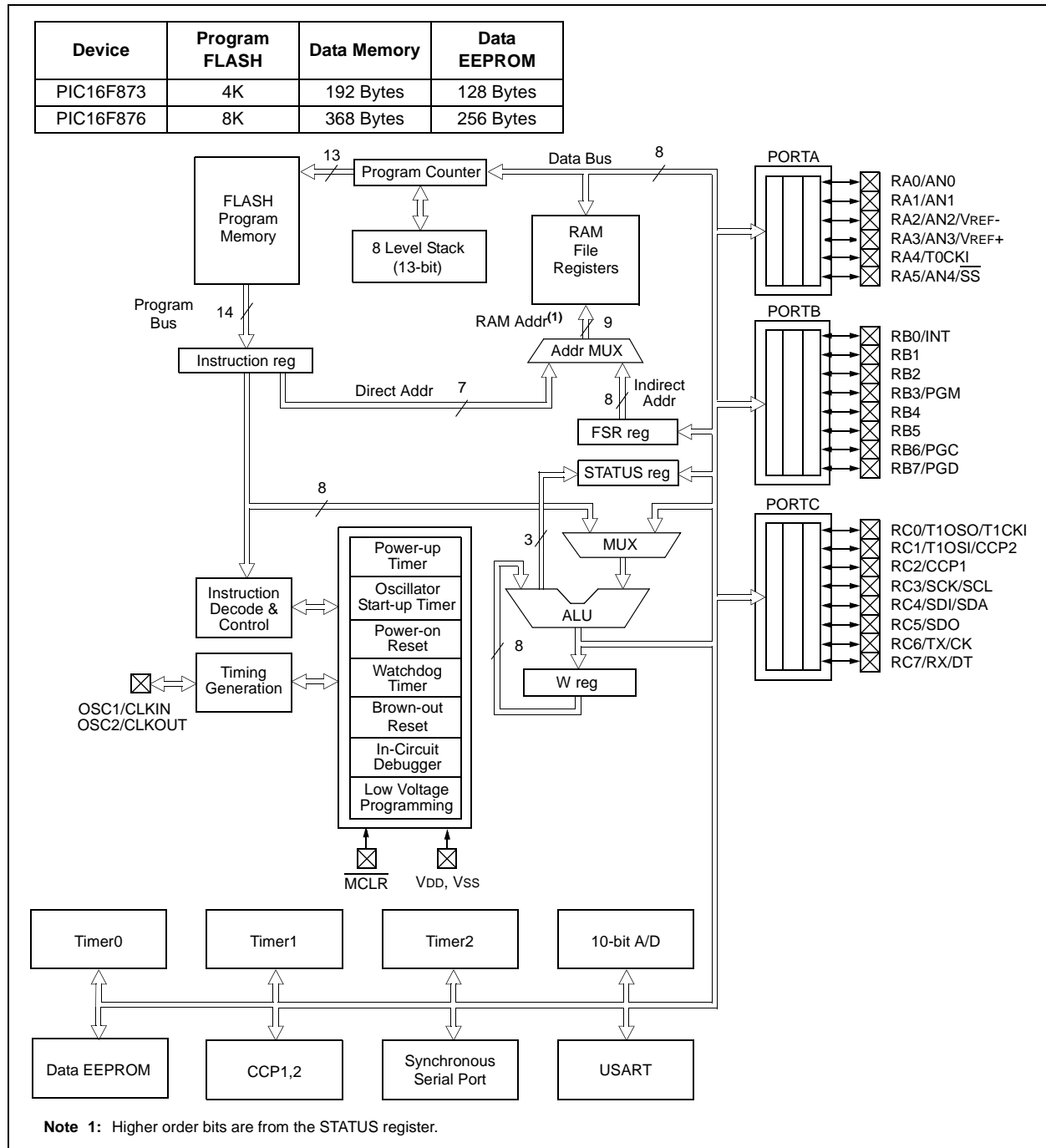
## 1.0 DEVICE OVERVIEW

This document contains device specific information. Additional information may be found in the PIC® MCU Mid-Range Reference Manual (DS33023), which may be obtained from your local Microchip Sales Representative or downloaded from the Microchip website. The Reference Manual should be considered a complementary document to this data sheet, and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

There are four devices (PIC16F873, PIC16F874, PIC16F876 and PIC16F877) covered by this data sheet. The PIC16F876/873 devices come in 28-pin packages and the PIC16F877/874 devices come in 40-pin packages. The Parallel Slave Port is not implemented on the 28-pin devices.

The following device block diagrams are sorted by pin number; 28-pin for Figure 1-1 and 40-pin for Figure 1-2. The 28-pin and 40-pin pinouts are listed in Table 1-1 and Table 1-2, respectively.

### FIGURE 1-1: PIC16F873 AND PIC16F876 BLOCK DIAGRAM



## REGISTER 3-1: TRISE REGISTER (ADDRESS 89h)

R-0	R-0	R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1
IBF	OBF	IBOV	PSPMODE	—	Bit2	Bit1	Bit0

bit 7

bit 0

### Parallel Slave Port Status/Control Bits:

- bit 7 **IBF:** Input Buffer Full Status bit  
 1 = A word has been received and is waiting to be read by the CPU  
 0 = No word has been received
- bit 6 **OBF:** Output Buffer Full Status bit  
 1 = The output buffer still holds a previously written word  
 0 = The output buffer has been read
- bit 5 **IBOV:** Input Buffer Overflow Detect bit (in Microprocessor mode)  
 1 = A write occurred when a previously input word has not been read (must be cleared in software)  
 0 = No overflow occurred
- bit 4 **PSPMODE:** Parallel Slave Port Mode Select bit  
 1 = PORTD functions in Parallel Slave Port mode  
 0 = PORTD functions in general purpose I/O mode
- bit 3 **Unimplemented:** Read as '0'
- PORTC Data Direction Bits:**
- bit 2 **Bit2:** Direction Control bit for pin RE2/ $\overline{\text{CS}}$ /AN7  
 1 = Input  
 0 = Output
- bit 1 **Bit1:** Direction Control bit for pin RE1/ $\overline{\text{WR}}$ /AN6  
 1 = Input  
 0 = Output
- bit 0 **Bit0:** Direction Control bit for pin RE0/ $\overline{\text{RD}}$ /AN5  
 1 = Input  
 0 = Output

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared    x = Bit is unknown

# PIC16F87X

## 5.2 Using Timer0 with an External Clock

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

## 5.3 Prescaler

There is only one prescaler available, which is mutually exclusively shared between the Timer0 module and the Watchdog Timer. A prescaler assignment for the

Timer0 module means that there is no prescaler for the Watchdog Timer, and vice-versa. This prescaler is not readable or writable (see Figure 5-1).

The PSA and PS2:PS0 bits (OPTION\_REG<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g. CLRF 1, MOVWF 1, BSF 1, x....etc.) will clear the prescaler. When assigned to WDT, a CLRWDI instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.

**Note:** Writing to TMR0, when the prescaler is assigned to Timer0, will clear the prescaler count, but will not change the prescaler assignment.

**REGISTER 5-1: OPTION\_REG REGISTER**

	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
	bit 7							bit 0
bit 7	<b>RBPU</b>							
bit 6	<b>INTEDG</b>							
bit 5	<b>T0CS:</b> TMR0 Clock Source Select bit							
	1 = Transition on T0CKI pin							
	0 = Internal instruction cycle clock (CLKOUT)							
bit 4	<b>T0SE:</b> TMR0 Source Edge Select bit							
	1 = Increment on high-to-low transition on T0CKI pin							
	0 = Increment on low-to-high transition on T0CKI pin							
bit 3	<b>PSA:</b> Prescaler Assignment bit							
	1 = Prescaler is assigned to the WDT							
	0 = Prescaler is assigned to the Timer0 module							
bit 2-0	<b>PS2:PS0:</b> Prescaler Rate Select bits							
	Bit Value	TMR0 Rate	WDT Rate					
	000	1 : 2	1 : 1					
	001	1 : 4	1 : 2					
	010	1 : 8	1 : 4					
	011	1 : 16	1 : 8					
	100	1 : 32	1 : 16					
	101	1 : 64	1 : 32					
	110	1 : 128	1 : 64					
	111	1 : 256	1 : 128					

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

**Note:** To avoid an unintended device RESET, the instruction sequence shown in the PIC<sup>®</sup> MCU Mid-Range Family Reference Manual (DS33023) must be executed when changing the prescaler assignment from Timer0 to the WDT. This sequence must be followed even if the WDT is disabled.

## 6.4 Timer1 Operation in Asynchronous Counter Mode

If control bit  $\overline{T1SYNC}$  ( $T1CON<2>$ ) is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during SLEEP and can generate an interrupt-on-overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (Section 6.4.1).

In Asynchronous Counter mode, Timer1 cannot be used as a time-base for capture or compare operations.

### 6.4.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock, will guarantee a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the timer register.

Reading the 16-bit value requires some care. Examples 12-2 and 12-3 in the PIC<sup>®</sup> MCU Mid-Range Family Reference Manual (DS33023) show how to read and write Timer1 when it is running in Asynchronous mode.

## 6.5 Timer1 Oscillator

A crystal oscillator circuit is built-in between pins T1OSI (input) and T1OSO (amplifier output). It is enabled by setting control bit T1OSCEN ( $T1CON<3>$ ). The oscillator is a low power oscillator, rated up to 200 kHz. It will continue to run during SLEEP. It is primarily intended for use with a 32 kHz crystal. Table 6-1 shows the capacitor selection for the Timer1 oscillator.

The Timer1 oscillator is identical to the LP oscillator. The user must provide a software time delay to ensure proper oscillator start-up.

**TABLE 6-1: CAPACITOR SELECTION FOR THE TIMER1 OSCILLATOR**

Osc Type	Freq.	C1	C2
LP	32 kHz	33 pF	33 pF
	100 kHz	15 pF	15 pF
	200 kHz	15 pF	15 pF
These values are for design guidance only.			
Crystals Tested:			
32.768 kHz	Epson C-001R32.768K-A	± 20 PPM	
100 kHz	Epson C-2 100.00 KC-P	± 20 PPM	
200 kHz	STD XTL 200.000 kHz	± 20 PPM	
<b>Note 1:</b> Higher capacitance increases the stability of oscillator, but also increases the start-up time.			
<b>2:</b> Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.			

## 6.6 Resetting Timer1 using a CCP Trigger Output

If the CCP1 or CCP2 module is configured in Compare mode to generate a “special event trigger” ( $CCP1M3:CCP1M0 = 1011$ ), this signal will reset Timer1.

**Note:** The special event triggers from the CCP1 and CCP2 modules will not set interrupt flag bit TMR1IF ( $PIR1<0>$ ).

Timer1 must be configured for either Timer or Synchronized Counter mode to take advantage of this feature. If Timer1 is running in Asynchronous Counter mode, this RESET operation may not work.

In the event that a write to Timer1 coincides with a special event trigger from CCP1 or CCP2, the write will take precedence.

In this mode of operation, the CCPRxH:CCPRxL register pair effectively becomes the period register for Timer1.

## 9.2.1 SLAVE MODE

In Slave mode, the SCL and SDA pins must be configured as inputs. The MSSP module will override the input state with the output data, when required (slave-transmitter).

When an address is matched, or the data transfer after an address match is received, the hardware automatically will generate the Acknowledge ( $\overline{\text{ACK}}$ ) pulse, and then load the SSPBUF register with the received value currently in the SSPSR register.

There are certain conditions that will cause the MSSP module not to give this  $\overline{\text{ACK}}$  pulse. These are if either (or both):

- The buffer full bit BF (SSPSTAT<0>) was set before the transfer was received.
- The overflow bit SSPOV (SSPCON<6>) was set before the transfer was received.

If the BF bit is set, the SSPSR register value is not loaded into the SSPBUF, but bit SSPIF and SSPOV are set. Table 9-2 shows what happens when a data transfer byte is received, given the status of bits BF and SSPOV. The shaded cells show the condition where user software did not properly clear the overflow condition. Flag bit BF is cleared by reading the SSPBUF register, while bit SSPOV is cleared through software.

The SCL clock input must have a minimum high and low time for proper operation. The high and low times of the I<sup>2</sup>C specification, as well as the requirement of the MSSP module, is shown in timing parameter #100 and parameter #101 of the electrical specifications.

### 9.2.1.1 Addressing

Once the MSSP module has been enabled, it waits for a START condition to occur. Following the START condition, the 8-bits are shifted into the SSPSR register. All incoming bits are sampled with the rising edge of the clock (SCL) line. The value of register SSPSR<7:1> is compared to the value of the SSPADD register. The address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match, and the BF and SSPOV bits are clear, the following events occur:

- The SSPSR register value is loaded into the SSPBUF register on the falling edge of the 8th SCL pulse.
- The buffer full bit, BF, is set on the falling edge of the 8th SCL pulse.
- An  $\overline{\text{ACK}}$  pulse is generated.
- SSP interrupt flag bit, SSPIF (PIR1<3>), is set (interrupt is generated if enabled) on the falling edge of the 9th SCL pulse.

In 10-bit address mode, two address bytes need to be received by the slave. The five Most Significant bits (MSBs) of the first address byte specify if this is a 10-bit address. Bit R/W (SSPSTAT<2>) must specify a write so the slave device will receive the second address byte.

For a 10-bit address, the first byte would equal '1111 0 A9 A8 0', where A9 and A8 are the two MSBs of the address. The sequence of events for a 10-bit address is as follows, with steps 7-9 for slave-transmitter:

- Receive first (high) byte of Address (bits SSPIF, BF and UA (SSPSTAT<1>) are set).
- Update the SSPADD register with the second (low) byte of Address (clears bit UA and releases the SCL line).
- Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
- Receive second (low) byte of Address (bits SSPIF, BF and UA are set).
- Update the SSPADD register with the first (high) byte of Address. This will clear bit UA and release the SCL line.
- Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
- Receive Repeated Start condition.
- Receive first (high) byte of Address (bits SSPIF and BF are set).
- Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.

**Note:** Following the Repeated START condition (step 7) in 10-bit mode, the user only needs to match the first 7-bit address. The user does not update the SSPADD for the second half of the address.

### 9.2.1.2 Slave Reception

When the R/W bit of the address byte is clear and an address match occurs, the R/W bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register.

When the address byte overflow condition exists, then no Acknowledge ( $\overline{\text{ACK}}$ ) pulse is given. An overflow condition is defined as either bit BF (SSPSTAT<0>) is set, or bit SSPOV (SSPCON<6>) is set. This is an error condition due to user firmware.

An SSP interrupt is generated for each data transfer byte. Flag bit SSPIF (PIR1<3>) must be cleared in software. The SSPSTAT register is used to determine the status of the received byte.

**Note:** The SSPBUF will be loaded if the SSPOV bit is set and the BF flag is cleared. If a read of the SSPBUF was performed, but the user did not clear the state of the SSPOV bit before the next receive occurred, the  $\overline{\text{ACK}}$  is not sent and the SSPBUF is updated.

# PIC16F87X

**TABLE 10-3: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 0)**

BAUD RATE (K)	Fosc = 20 MHz			Fosc = 16 MHz			Fosc = 10 MHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	-	-	-	-	-	-	-	-	-
1.2	1.221	1.75	255	1.202	0.17	207	1.202	0.17	129
2.4	2.404	0.17	129	2.404	0.17	103	2.404	0.17	64
9.6	9.766	1.73	31	9.615	0.16	25	9.766	1.73	15
19.2	19.531	1.72	15	19.231	0.16	12	19.531	1.72	7
28.8	31.250	8.51	9	27.778	3.55	8	31.250	8.51	4
33.6	34.722	3.34	8	35.714	6.29	6	31.250	6.99	4
57.6	62.500	8.51	4	62.500	8.51	3	52.083	9.58	2
HIGH	1.221	-	255	0.977	-	255	0.610	-	255
LOW	312.500	-	0	250.000	-	0	156.250	-	0

BAUD RATE (K)	Fosc = 4 MHz			Fosc = 3.6864 MHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	0.300	0	207	0.3	0	191
1.2	1.202	0.17	51	1.2	0	47
2.4	2.404	0.17	25	2.4	0	23
9.6	8.929	6.99	6	9.6	0	5
19.2	20.833	8.51	2	19.2	0	2
28.8	31.250	8.51	1	28.8	0	1
33.6	-	-	-	-	-	-
57.6	62.500	8.51	0	57.6	0	0
HIGH	0.244	-	255	0.225	-	255
LOW	62.500	-	0	57.6	-	0

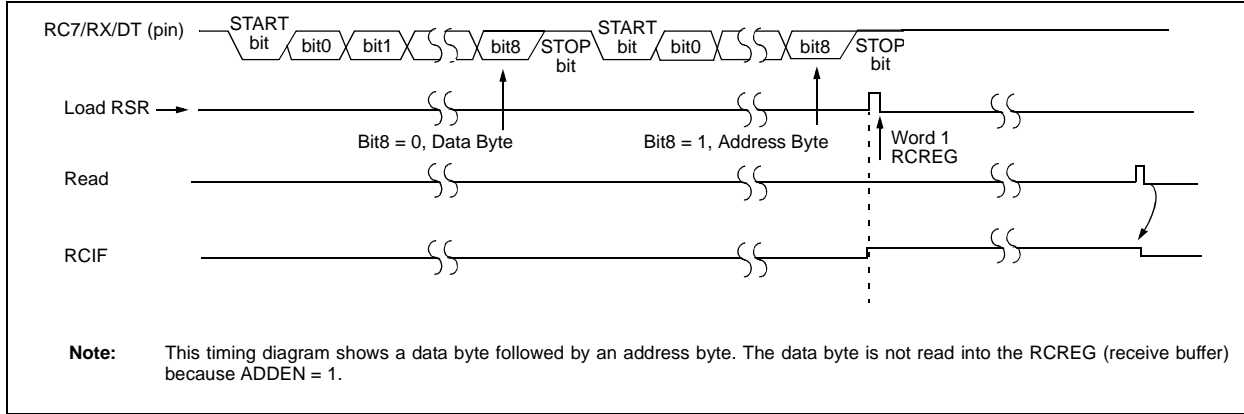
**TABLE 10-4: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 1)**

BAUD RATE (K)	Fosc = 20 MHz			Fosc = 16 MHz			Fosc = 10 MHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	-	-	-	-	-	-	-	-	-
1.2	-	-	-	-	-	-	-	-	-
2.4	-	-	-	-	-	-	2.441	1.71	255
9.6	9.615	0.16	129	9.615	0.16	103	9.615	0.16	64
19.2	19.231	0.16	64	19.231	0.16	51	19.531	1.72	31
28.8	29.070	0.94	42	29.412	2.13	33	28.409	1.36	21
33.6	33.784	0.55	36	33.333	0.79	29	32.895	2.10	18
57.6	59.524	3.34	20	58.824	2.13	16	56.818	1.36	10
HIGH	4.883	-	255	3.906	-	255	2.441	-	255
LOW	1250.000	-	0	1000.000	-	0	625.000	-	0

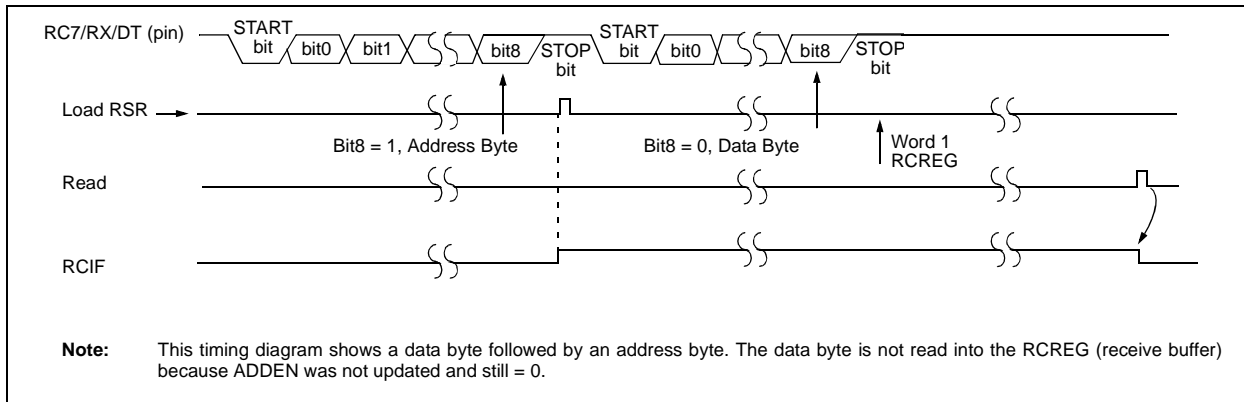
BAUD RATE (K)	Fosc = 4 MHz			Fosc = 3.6864 MHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	-	-	-	-	-	-
1.2	1.202	0.17	207	1.2	0	191
2.4	2.404	0.17	103	2.4	0	95
9.6	9.615	0.16	25	9.6	0	23
19.2	19.231	0.16	12	19.2	0	11
28.8	27.798	3.55	8	28.8	0	7
33.6	35.714	6.29	6	32.9	2.04	6
57.6	62.500	8.51	3	57.6	0	3
HIGH	0.977	-	255	0.9	-	255
LOW	250.000	-	0	230.4	-	0

# PIC16F87X

**FIGURE 10-7: ASYNCHRONOUS RECEPTION WITH ADDRESS DETECT**



**FIGURE 10-8: ASYNCHRONOUS RECEPTION WITH ADDRESS BYTE FIRST**



**TABLE 10-7: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh, 8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	R0IF	0000 000x	0000 000u
0Ch	PIR1	PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
1Ah	RCREG	USART Receive Register								0000 0000	0000 0000
8Ch	PIE1	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for asynchronous reception.

**Note 1:** Bits PSPIE and PSPIF are reserved on PIC16F873/876 devices; always maintain these bits clear.



# PIC16F87X

## REGISTER 11-2: ADCON1 REGISTER (ADDRESS 9Fh)

U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	—	—	PCFG3	PCFG2	PCFG1	PCFG0

bit 7

bit 0

bit 7

**ADFM:** A/D Result Format Select bit

1 = Right justified. 6 Most Significant bits of ADRESH are read as '0'.

0 = Left justified. 6 Least Significant bits of ADRESL are read as '0'.

bit 6-4

**Unimplemented:** Read as '0'

bit 3-0

**PCFG3:PCFG0:** A/D Port Configuration Control bits:

PCFG3: PCFG0	AN7 <sup>(1)</sup> RE2	AN6 <sup>(1)</sup> RE1	AN5 <sup>(1)</sup> RE0	AN4 RA5	AN3 RA3	AN2 RA2	AN1 RA1	AN0 RA0	VREF+	VREF-	CHAN/ Refs <sup>(2)</sup>
0000	A	A	A	A	A	A	A	A	VDD	VSS	8/0
0001	A	A	A	A	VREF+	A	A	A	RA3	VSS	7/1
0010	D	D	D	A	A	A	A	A	VDD	VSS	5/0
0011	D	D	D	A	VREF+	A	A	A	RA3	VSS	4/1
0100	D	D	D	D	A	D	A	A	VDD	VSS	3/0
0101	D	D	D	D	VREF+	D	A	A	RA3	VSS	2/1
011x	D	D	D	D	D	D	D	D	VDD	VSS	0/0
1000	A	A	A	A	VREF+	VREF-	A	A	RA3	RA2	6/2
1001	D	D	A	A	A	A	A	A	VDD	VSS	6/0
1010	D	D	A	A	VREF+	A	A	A	RA3	VSS	5/1
1011	D	D	A	A	VREF+	VREF-	A	A	RA3	RA2	4/2
1100	D	D	D	A	VREF+	VREF-	A	A	RA3	RA2	3/2
1101	D	D	D	D	VREF+	VREF-	A	A	RA3	RA2	2/2
1110	D	D	D	D	D	D	D	A	VDD	VSS	1/0
1111	D	D	D	D	VREF+	VREF-	D	A	RA3	RA2	1/2

A = Analog input    D = Digital I/O

**Note 1:** These channels are not available on PIC16F873/876 devices.

**2:** This column indicates the number of analog channels available as A/D inputs and the number of analog channels used as voltage reference inputs.

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

The ADRESH:ADRESL registers contain the 10-bit result of the A/D conversion. When the A/D conversion is complete, the result is loaded into this A/D result register pair, the GO/DONE bit (ADCON0<2>) is cleared and the A/D interrupt flag bit ADIF is set. The block diagram of the A/D module is shown in Figure 11-1.

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as inputs.

To determine sample time, see Section 11.1. After this acquisition time has elapsed, the A/D conversion can be started.

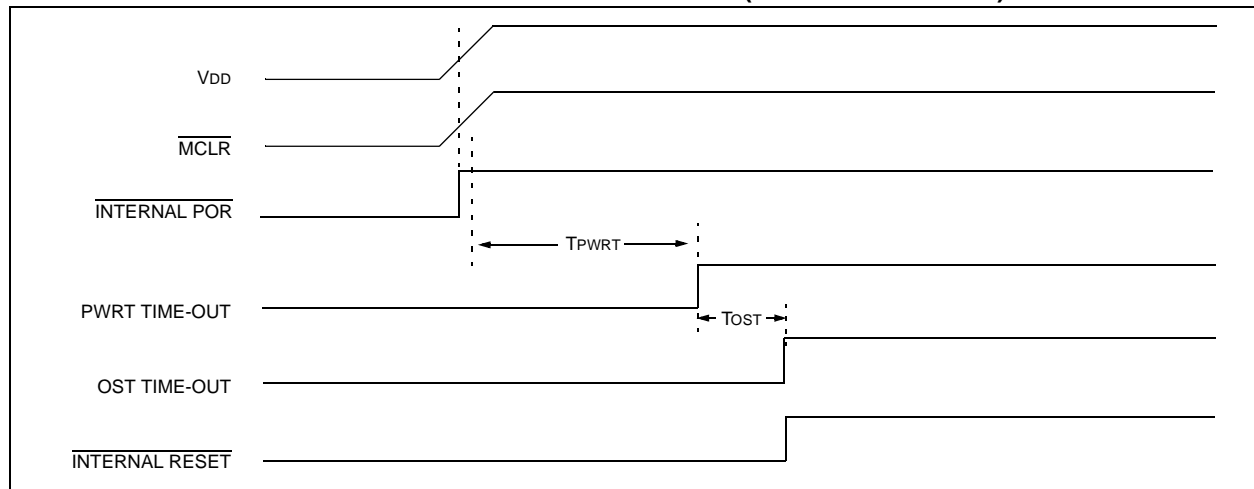
**TABLE 12-6: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)**

Register	Devices				Power-on Reset, Brown-out Reset	MCLR Resets, WDT Reset	Wake-up via WDT or Interrupt
PIE2	873	874	876	877	-r-0 0--0	-r-0 0--0	-r-u u--u
PCON	873	874	876	877	---- --qq	---- --uu	---- --uu
PR2	873	874	876	877	1111 1111	1111 1111	1111 1111
SSPADD	873	874	876	877	0000 0000	0000 0000	uuuu uuuu
SSPSTAT	873	874	876	877	--00 0000	--00 0000	--uu uuuu
TXSTA	873	874	876	877	0000 -010	0000 -010	uuuu -uuu
SPBRG	873	874	876	877	0000 0000	0000 0000	uuuu uuuu
ADRESL	873	874	876	877	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON1	873	874	876	877	0--- 0000	0--- 0000	u--- uuuu
EEDATA	873	874	876	877	0--- 0000	0--- 0000	u--- uuuu
EEADR	873	874	876	877	xxxx xxxx	uuuu uuuu	uuuu uuuu
EEDATH	873	874	876	877	xxxx xxxx	uuuu uuuu	uuuu uuuu
EEADRH	873	874	876	877	xxxx xxxx	uuuu uuuu	uuuu uuuu
EECON1	873	874	876	877	x--- x000	u--- u000	u--- uuuu
EECON2	873	874	876	877	---- ----	---- ----	---- ----

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition, r = reserved, maintain clear

- Note 1:** One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).  
**Note 2:** When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).  
**Note 3:** See Table 12-5 for RESET value for specific condition.

**FIGURE 12-5: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD)**



**TABLE 14-1: DEVELOPMENT TOOLS FROM MICROCHIP**

	PIC12CXXX	PIC14000	PIC16C5X	PIC16C6X	PIC16CXXX	PIC16F62X	PIC16C7X	PIC16C7XX	PIC16C8X	PIC16F8XX	PIC16C9XX	PIC17C4X	PIC17C7XX	PIC18CXX2	24CXX/ 25CXX/ 93CXX	HCSXX	MCRFXXX	MCP2510
<b>Tools</b>	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓				
<b>Software Tools</b>	MPLAB® Integrated Development Environment																	
<b>Software Tools</b>	MPLAB® C17 C Compiler																	
<b>Software Tools</b>	MPLAB® C18 C Compiler																	
<b>Software Tools</b>	MPASM™ Assembler/ MPLINK™ Object Linker	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
<b>Software Tools</b>	MPLAB® ICE In-Circuit Emulator	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
<b>Software Tools</b>	ICEPIC™ In-Circuit Emulator	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
<b>Debugger</b>	MPLAB® ICD In-Circuit Debugger			✓*			✓*			✓								
<b>Programmers</b>	PICSTART® Plus Entry Level Development Programmer	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
<b>Programmers</b>	PRO MATE® II Universal Device Programmer	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
<b>Demo Boards and Eval Kits</b>	PICDEM™ 1 Demonstration Board		✓				†		✓			✓						
<b>Demo Boards and Eval Kits</b>	PICDEM™ 2 Demonstration Board				†		†							✓				
<b>Demo Boards and Eval Kits</b>	PICDEM™ 3 Demonstration Board										✓							
<b>Demo Boards and Eval Kits</b>	PICDEM™ 14A Demonstration Board	✓																
<b>Demo Boards and Eval Kits</b>	PICDEM™ 17 Demonstration Board											✓						
<b>Demo Boards and Eval Kits</b>	KEELOQ® Evaluation Kit															✓		
<b>Demo Boards and Eval Kits</b>	KEELOQ® Transponder Kit															✓		
<b>Demo Boards and Eval Kits</b>	microID™ Programmer's Kit																✓	
<b>Demo Boards and Eval Kits</b>	125 kHz microID™ Developer's Kit																✓	
<b>Demo Boards and Eval Kits</b>	125 kHz Anticollision microID™ Developer's Kit																✓	
<b>Demo Boards and Eval Kits</b>	13.56 MHz Anticollision microID™ Developer's Kit																✓	
<b>Demo Boards and Eval Kits</b>	MCP2510 CAN Developer's Kit																✓	✓

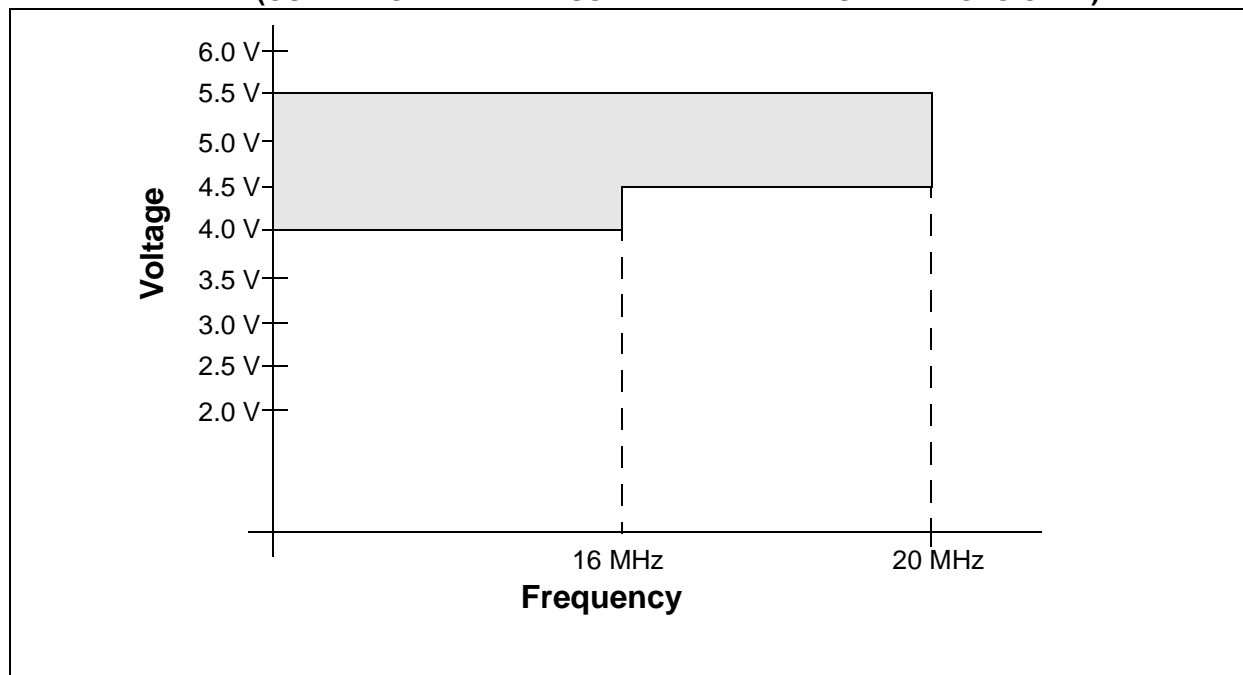
\* Contact the Microchip Technology Inc. web site at [www.microchip.com](http://www.microchip.com) for information on how to use the MPLAB® ICD In-Circuit Debugger (DV164001) with PIC16C62, 63, 64, 65, 72, 73, 74, 76, 77.

\*\* Contact Microchip Technology Inc. for availability date.

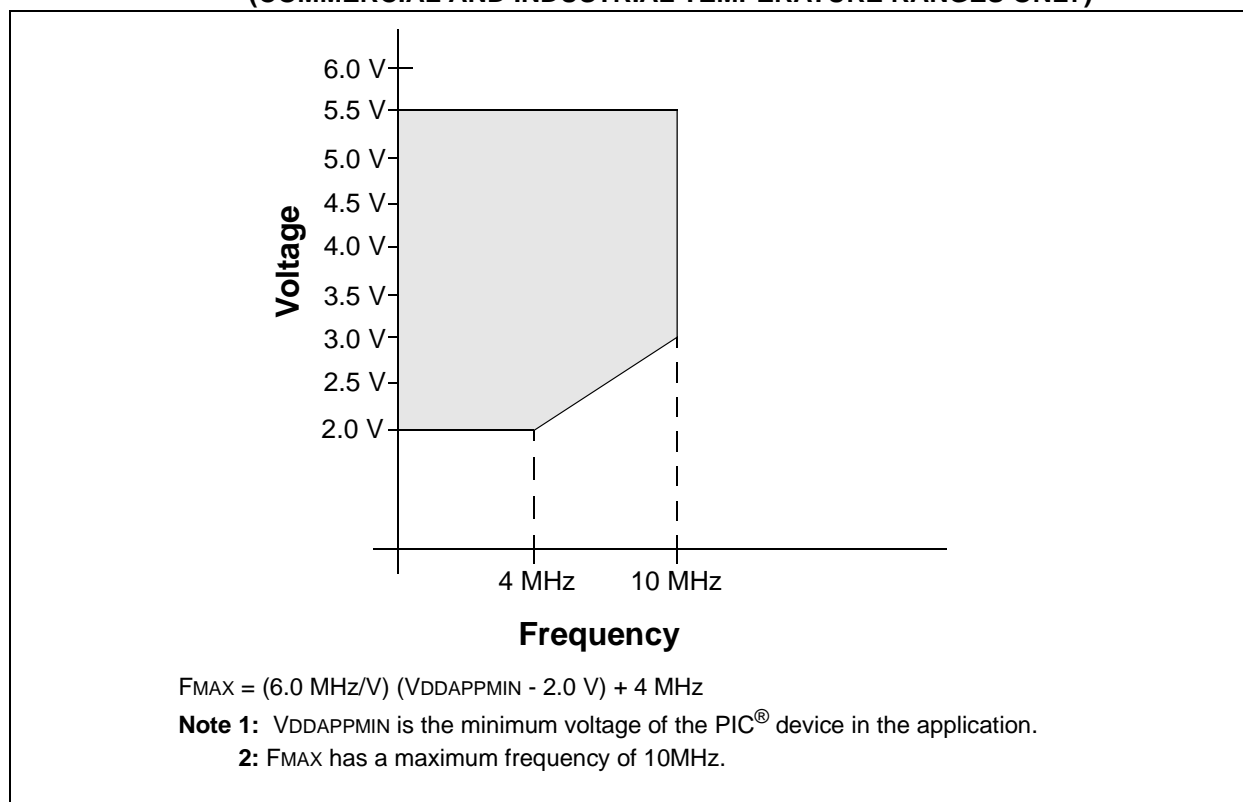
† Development tool is available on select devices.

# PIC16F87X

**FIGURE 15-1: PIC16F87X-20 VOLTAGE-FREQUENCY GRAPH  
(COMMERCIAL AND INDUSTRIAL TEMPERATURE RANGES ONLY)**

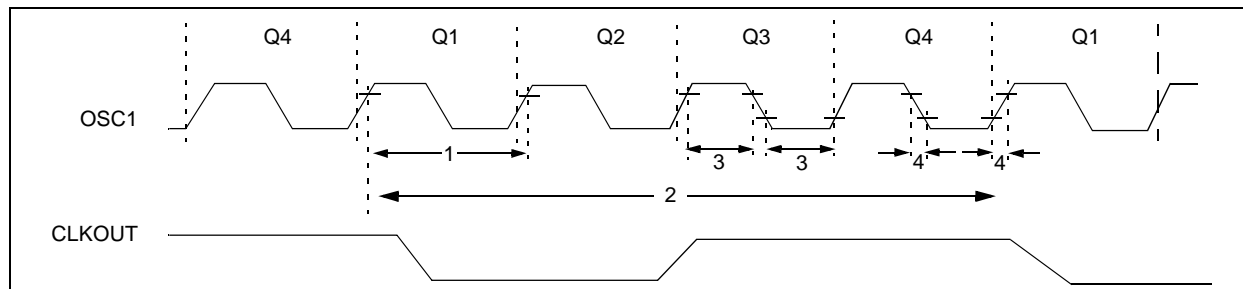


**FIGURE 15-2: PIC16LF87X-04 VOLTAGE-FREQUENCY GRAPH  
(COMMERCIAL AND INDUSTRIAL TEMPERATURE RANGES ONLY)**



# PIC16F87X

**FIGURE 15-6: EXTERNAL CLOCK TIMING**



**TABLE 15-1: EXTERNAL CLOCK TIMING REQUIREMENTS**

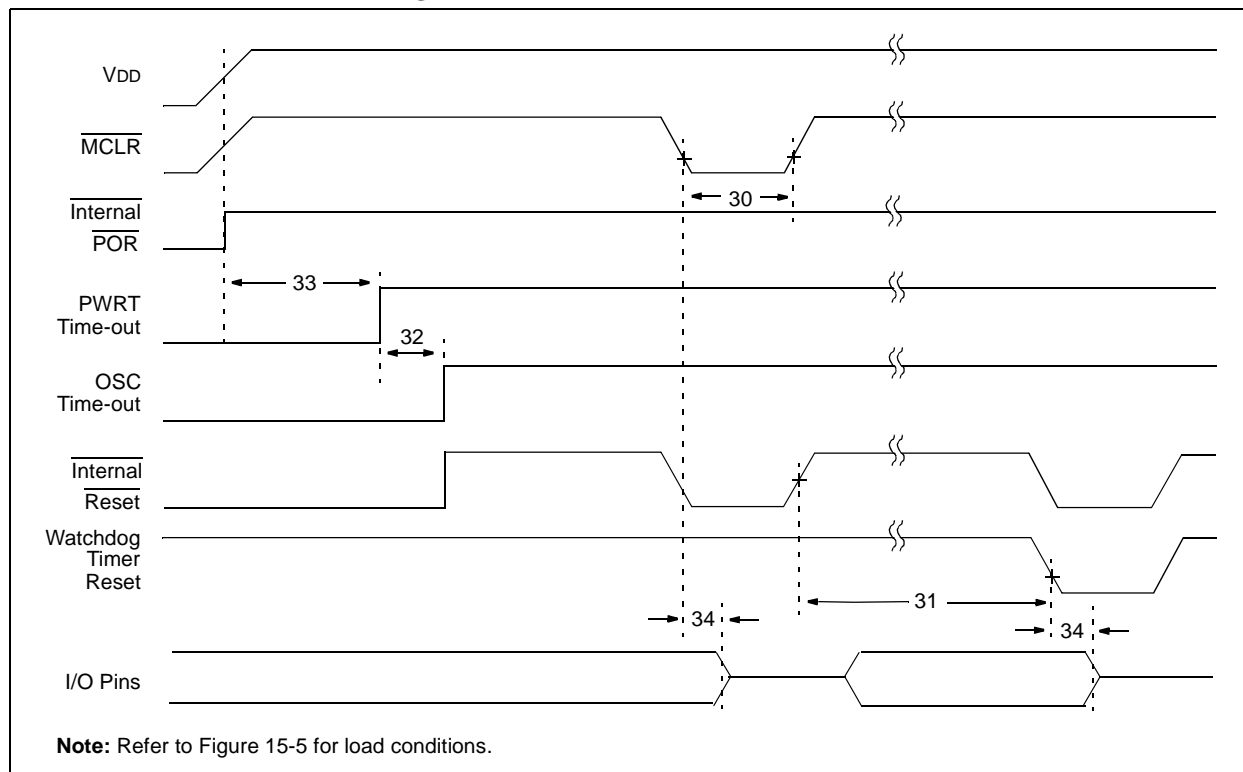
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fosc	External CLKIN Frequency (Note 1)	DC	—	4	MHz	XT and RC osc mode
			DC	—	4	MHz	HS osc mode (-04)
			DC	—	10	MHz	HS osc mode (-10)
			DC	—	20	MHz	HS osc mode (-20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency (Note 1)	DC	—	4	MHz	RC osc mode
			0.1	—	4	MHz	XT osc mode
			4	—	10	MHz	HS osc mode (-10)
			4	—	20	MHz	HS osc mode (-20)
			5	—	200	kHz	LP osc mode
1	Tosc	External CLKIN Period (Note 1)	250	—	—	ns	XT and RC osc mode
			250	—	—	ns	HS osc mode (-04)
			100	—	—	ns	HS osc mode (-10)
			50	—	—	ns	HS osc mode (-20)
			5	—	—	μs	LP osc mode
		Oscillator Period (Note 1)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	—	ns	HS osc mode (-04)
			100	—	250	ns	HS osc mode (-10)
			50	—	250	ns	HS osc mode (-20)
2	Tcy	Instruction Cycle Time (Note 1)	200	Tcy	DC	ns	Tcy = 4/Fosc
			100	—	—	ns	XT oscillator
			2.5	—	—	μs	LP oscillator
3	TosL, TosH	External Clock in (OSC1) High or Low Time	15	—	—	ns	HS oscillator
			—	—	25	ns	XT oscillator
			—	—	50	ns	LP oscillator
4	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	15	ns	HS oscillator
			—	—	—	—	—
			—	—	—	—	—

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

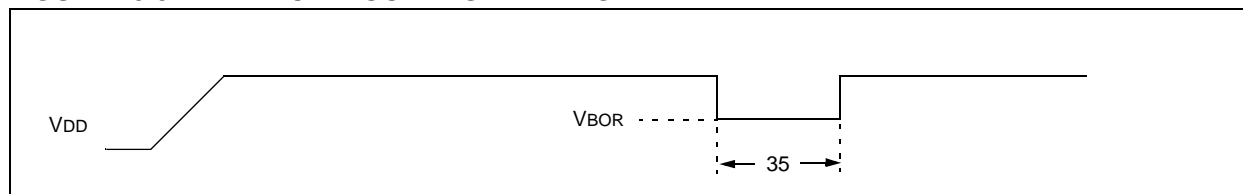
**Note 1:** Instruction cycle period (Tcy) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions, with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "max." cycle time limit is "DC" (no clock) for all devices.

# PIC16F87X

**FIGURE 15-8: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING**



**FIGURE 15-9: BROWN-OUT RESET TIMING**



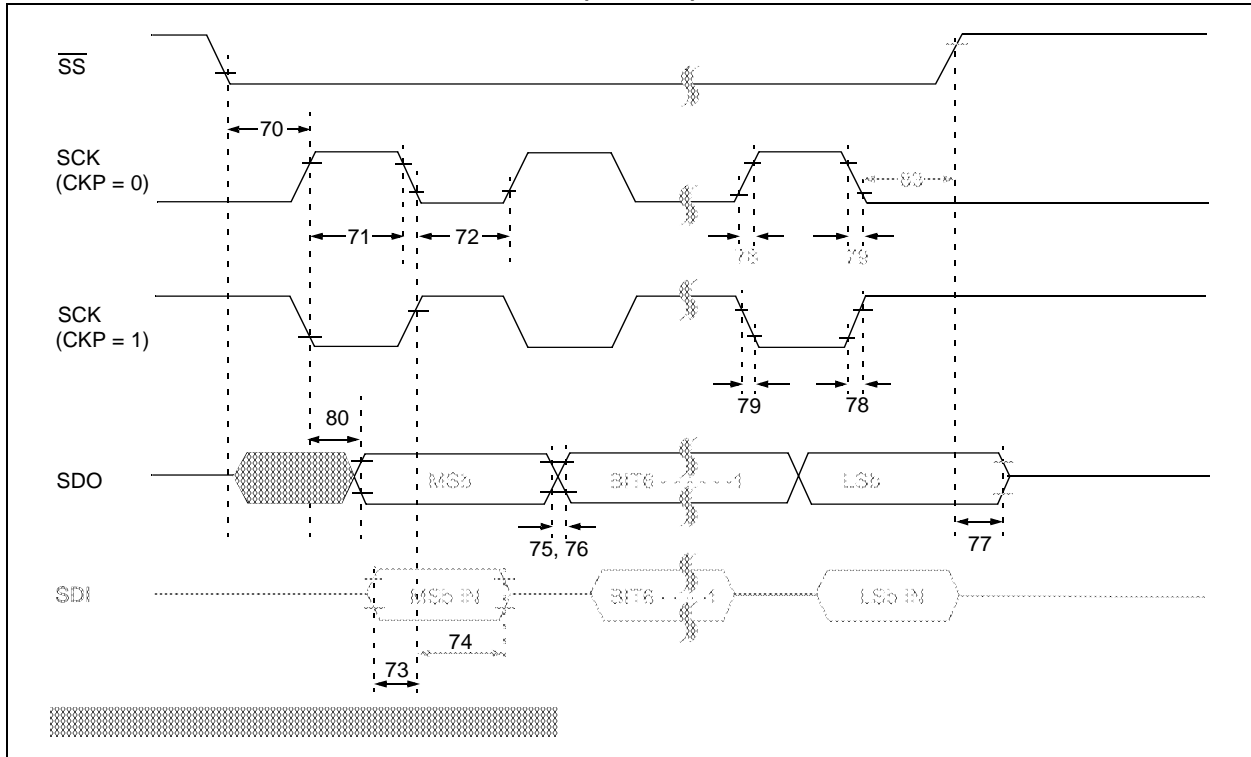
**TABLE 15-3: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS**

Parameter No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
30	Tmcl	MCLR Pulse Width (low)	2	—	—	μs	VDD = 5V, -40°C to +85°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +85°C
32	Tost	Oscillation Start-up Timer Period	—	1024 TOSC	—	—	TOSC = OSC1 period
33*	Tpwrt	Power-up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +85°C
34	Tioz	I/O Hi-impedance from MCLR Low or Watchdog Timer Reset	—	—	2.1	μs	
35	TBOR	Brown-out Reset pulse width	100	—	—	μs	VDD ≤ VBOR (D005)

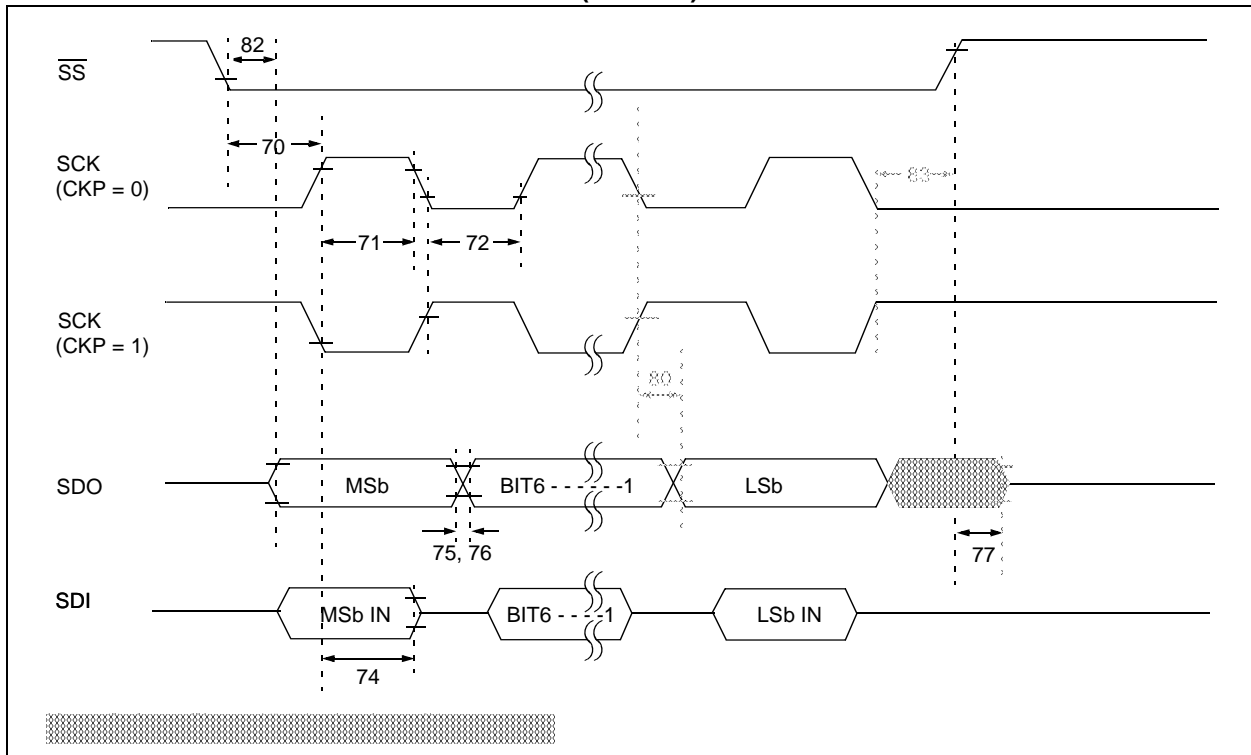
\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

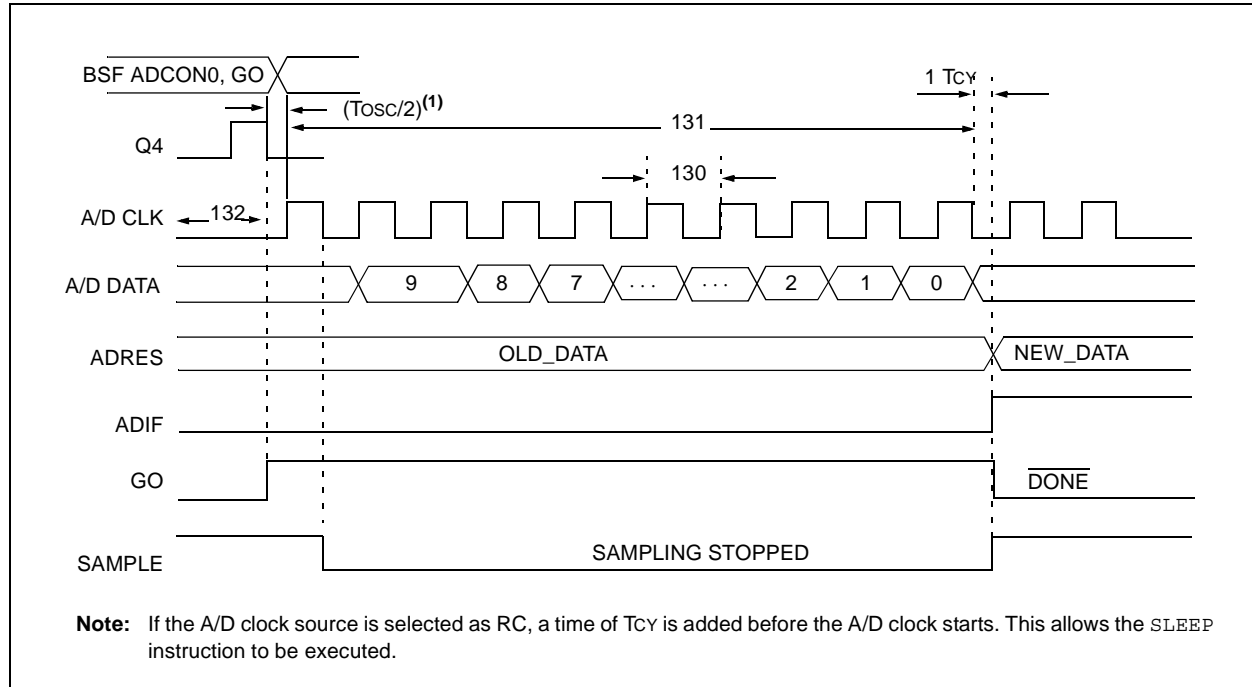
**FIGURE 15-15: SPI SLAVE MODE TIMING (CKE = 0)**



**FIGURE 15-16: SPI SLAVE MODE TIMING (CKE = 1)**



**FIGURE 15-21: A/D CONVERSION TIMING**



**TABLE 15-13: A/D CONVERSION REQUIREMENTS**

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
130	TAD	A/D clock period	Standard(F)	1.6	—	—	μs	TOSC based, VREF ≥ 3.0V
			Extended(LF)	3.0	—	—	μs	TOSC based, VREF ≥ 2.0V
			Standard(F)	2.0	4.0	6.0	μs	A/D RC mode
			Extended(LF)	3.0	6.0	9.0	μs	A/D RC mode
131	TCNV	Conversion time (not including S/H time) (Note 1)			—	12	TAD	
132	TACQ	Acquisition time		(Note 2)	40	—	μs	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1 LSB (i.e., 20.0 mV @ 5.12V) from the last sampled voltage (as stated on CHOLD).
				10*	—	—	μs	
134	TGO	Q4 to A/D clock start		—	TOSC/2 §	—	—	If the A/D clock source is selected as RC, a time of $T_{CY}$ is added before the A/D clock starts. This allows the <b>SLEEP</b> instruction to be executed.

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

**Note 1:** ADRES register may be read on the following  $T_{CY}$  cycle.

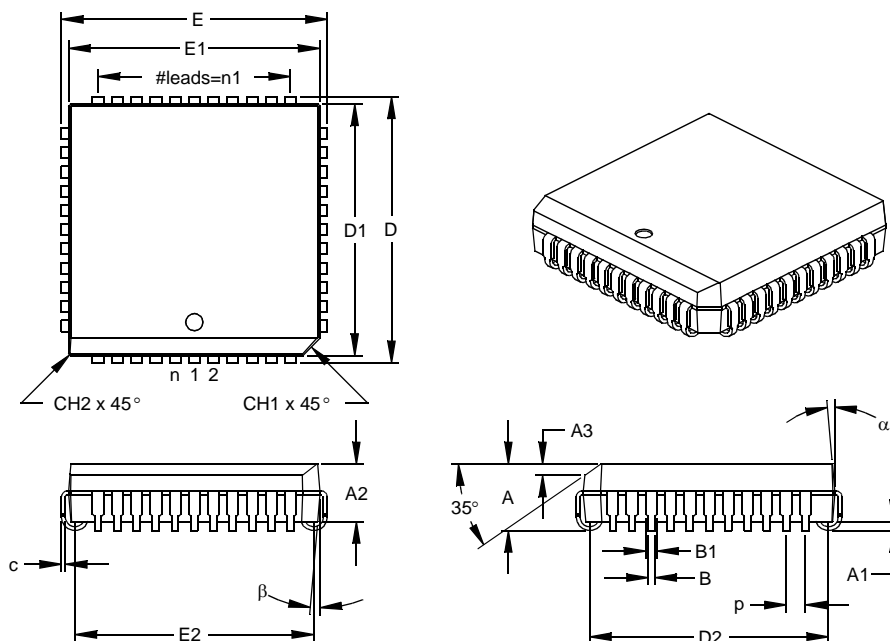
**2:** See Section 11.1 for minimum conditions.



# PIC16F87X

## 44-Lead Plastic Leaded Chip Carrier (L) – Square (PLCC)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		44			44	
Pitch	p		.050			1.27	
Pins per Side	n1		11			11	
Overall Height	A	.165	.173	.180	4.19	4.39	4.57
Molded Package Thickness	A2	.145	.153	.160	3.68	3.87	4.06
Standoff §	A1	.020	.028	.035	0.51	0.71	0.89
Side 1 Chamfer Height	A3	.024	.029	.034	0.61	0.74	0.86
Corner Chamfer 1	CH1	.040	.045	.050	1.02	1.14	1.27
Corner Chamfer (others)	CH2	.000	.005	.010	0.00	0.13	0.25
Overall Width	E	.685	.690	.695	17.40	17.53	17.65
Overall Length	D	.685	.690	.695	17.40	17.53	17.65
Molded Package Width	E1	.650	.653	.656	16.51	16.59	16.66
Molded Package Length	D1	.650	.653	.656	16.51	16.59	16.66
Footprint Width	E2	.590	.620	.630	14.99	15.75	16.00
Footprint Length	D2	.590	.620	.630	14.99	15.75	16.00
Lead Thickness	c	.008	.011	.013	0.20	0.27	0.33
Upper Lead Width	B1	.026	.029	.032	0.66	0.74	0.81
Lower Lead Width	B	.013	.020	.021	0.33	0.51	0.53
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

\* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-047

Drawing No. C04-048

PORTE .....	9, 17
Analog Port Pins .....	9, 36, 38
Associated Registers .....	36
Block Diagram .....	36
Input Buffer Full Status (IBF Bit) .....	37
Input Buffer Overflow (IBOV Bit) .....	37
Output Buffer Full Status (OBF Bit) .....	37
PORTE Register .....	15, 36
PSP Mode Select (PSPMODE Bit) .....	35, 36, 37, 38
RE0/RD/AN5 Pin .....	9, 36, 38
RE1/WR/AN6 Pin .....	9, 36, 38
RE2/CS/AN7 Pin .....	9, 36, 38
TRISE Register .....	36
Postscaler, WDT .....	
Assignment (PSA Bit) .....	19
Rate Select (PS2:PS0 Bits) .....	19
Power-down Mode. <i>See</i> SLEEP .....	
Power-on Reset (POR) .....	119, 123, 124, 125, 126
Oscillator Start-up Timer (OST) .....	119, 124
POR Status ( $\overline{\text{POR}}$ Bit) .....	25
Power Control (PCON) Register .....	124
Power-down ( $\overline{\text{PD}}$ Bit) .....	18, 123
Power-up Timer (PWRT) .....	119, 124
Time-out ( $\overline{\text{TO}}$ Bit) .....	18, 123
Time-out Sequence on Power-up .....	127, 128
PR2 Register .....	16, 55
Prescaler, Timer0 .....	
Assignment (PSA Bit) .....	19
Rate Select (PS2:PS0 Bits) .....	19
PRO MATE II Universal Device Programmer .....	145
Program Counter .....	
RESET Conditions .....	125
Program Memory .....	11
Interrupt Vector .....	11
Paging .....	11, 26
Program Memory Map .....	11
RESET Vector .....	11
Program Verification .....	133
Programming Pin (VPP) .....	7, 8
Programming, Device Instructions .....	135
PSP. <i>See</i> Parallel Slave Port. ....	38
Pulse Width Modulation. <i>See</i> Capture/Compare/PWM, PWM Mode. ....	
PUSH .....	26
<b>R</b> .....	
R/W .....	66
R/W bit .....	74
R/W bit .....	74
RAM. <i>See</i> Data Memory .....	
RCREG .....	17
RCSTA Register .....	17, 96
ADDEN Bit .....	96
CREN Bit .....	96
FERR Bit .....	96
OERR Bit .....	96
RX9 Bit .....	96
RX9D Bit .....	96
SPEN Bit .....	95, 96
SREN Bit .....	96
Read/Write bit, R/W .....	66
Reader Response .....	208
Receive Enable bit .....	68
Receive Overflow Indicator bit, SSPOV .....	67
Register File .....	12
Register File Map .....	13, 14

Registers .....	
ADCON0 (A/D Control 0) .....	111
ADCON1 (A/D Control 1) .....	112
CCP1CON (CCP Control 1) .....	58
EECON2 .....	41
FSR .....	27
INTCON .....	20
OPTION_REG .....	19, 48
PCON (Power Control) .....	25
PIE1 (Peripheral Interrupt Enable 1) .....	21
PIE2 (Peripheral Interrupt Enable 2) .....	23
PIR1 (Peripheral Interrupt Request 1) .....	22
PIR2 (Peripheral Interrupt Request 2) .....	24
RCSTA (Receive Status and Control) .....	96
Special Function, Summary .....	15
SSPCON2 (Sync Serial Port Control 2) .....	68
STATUS .....	18
T1CON (Timer1 Control) .....	51
T2CON (Timer 2 Control) .....	
Timer2 .....	
T2CON Register .....	55
TRISE .....	37
TXSTA (Transmit Status and Control) .....	95
Repeated START Condition Enable bit .....	68
RESET .....	119, 123
Block Diagram .....	123
MCLR Reset. <i>See</i> MCLR .....	
RESET .....	
Brown-out Reset (BOR). <i>See</i> Brown-out Reset (BOR) .....	
Power-on Reset (POR). <i>See</i> Power-on Reset (POR) .....	
RESET Conditions for PCON Register .....	125
RESET Conditions for Program Counter .....	125
RESET Conditions for STATUS Register .....	125
WDT Reset. <i>See</i> Watchdog Timer (WDT) .....	
Revision History .....	197
<b>S</b> .....	
S (START bit) .....	66
Sales and Support .....	209
SCI. <i>See</i> USART .....	
SCK .....	69
SCL .....	74
SDA .....	74
SDI .....	69
SDO .....	69
Serial Clock, SCK .....	69
Serial Clock, SCL .....	74
Serial Communication Interface. <i>See</i> USART .....	
Serial Data Address, SDA .....	74
Serial Data In, SDI .....	69
Serial Data Out, SDO .....	69
Slave Select, $\overline{\text{SS}}$ .....	69
SLEEP .....	119, 123, 132
SMP .....	66
Software Simulator (MPLAB SIM) .....	144
SPBRG Register .....	16
Special Features of the CPU .....	119
Special Function Registers .....	15
Special Function Registers (SFRs) .....	15
Data EEPROM and FLASH Program Memory .....	41
Speed, Operating .....	1

# PIC16F87X

SPI		
Master Mode	70	
Master Mode Timing	70	
Serial Clock	69	
Serial Data In	69	
Serial Data Out	69	
Serial Peripheral Interface (SPI)	65	
Slave Mode Timing	71	
Slave Mode Timing Diagram	71	
Slave Select	69	
SPI Clock	70	
SPI Mode	69	
SPI Clock Edge Select, CKE	66	
SPI Data Input Sample Phase Select, SMP	66	
SPI Mode		
Associated Registers	72	
SPI Module		
Slave Mode	71	
SS	69	
SSP	65	
Block Diagram (SPI Mode)	69	
RA5/ $\overline{\text{SS}}$ /AN4 Pin	7, 8	
RC3/SCK/SCL Pin	7, 9	
RC4/SDI/SDA Pin	7, 9	
RC5/SDO Pin	7, 9	
SPI Mode	69	
SSPADD	73, 74	
SSPBUF	70, 73	
SSPCON2	68	
SSPSR	70, 74	
SSPSTAT	73	
SSP I <sup>2</sup> C		
SSP I <sup>2</sup> C Operation	73	
SSP Module		
SPI Master Mode	70	
SPI Slave Mode	71	
SSPCON1 Register	73	
SSP Overflow Detect bit, SSPOV	74	
SSPADD Register	16	
SSPBUF	17, 73, 74	
SSPBUF Register	15	
SSPCON Register	15	
SSPCON1	73	
SSPCON2 Register	68	
SSPEN	67	
SSPIF	22, 74	
SSPM3:SSPM0	67	
SSPOV	67, 74, 84	
SSPSTAT	73	
SSPSTAT Register	16	
Stack	26	
Overflows	26	
Underflow	26	
START bit (S)	66	
START Condition Enable bit	68	
STATUS Register	18	
C Bit	18	
DC Bit	18	
IRP Bit	18	
PD Bit	18, 123	
RP1:RP0 Bits	18	
TO Bit	18, 123	
Z Bit	18	
STOP bit (P)	66	
STOP Condition Enable bit	68	
Synchronous Serial Port	65	
Synchronous Serial Port Enable bit, SSPEN	67	
Synchronous Serial Port Interrupt	22	
Synchronous Serial Port Mode Select bits, SSPM3:SSPM0	67	
T		
T1CKPS0 bit	51	
T1CKPS1 bit	51	
T1CON	17	
T1CON Register	17	
T1OSCEN bit	51	
T1SYNC bit	51	
T2CKPS0 bit	55	
T2CKPS1 bit	55	
T2CON Register	17, 55	
TAD	115	
Time-out Sequence	124	
Timer0	47	
Associated Registers	49	
Clock Source Edge Select (T0SE Bit)	19	
Clock Source Select (T0CS Bit)	19	
External Clock	48	
Interrupt	47	
Overflow Enable (T0IE Bit)	20	
Overflow Flag (T0IF Bit)	20, 130	
Overflow Interrupt	130	
Prescaler	48	
RA4/T0CKI Pin, External Clock	7, 8	
T0CKI	48	
WDT Prescaler Block Diagram	47	
Timer1	51	
Associated Registers	54	
Asynchronous Counter Mode	53	
Reading and Writing to	53	
Block Diagram	52	
Counter Operation	52	
Operation in Timer Mode	52	
Oscillator	53	
Capacitor Selection	53	
Prescaler	54	
RC0/T1OSO/T1CKI Pin	7, 9	
RC1/T1OSI/CCP2 Pin	7, 9	
Resetting of Timer1 Registers	54	
Resetting Timer1 using a CCP Trigger Output	53	
Synchronized Counter Mode	52	
T1CON	51	
T1CON Register	51	
TMR1H	53	
TMR1L	53	
Timer2	55	
Associated Registers	56	
Block Diagram	55	
Output	56	
Postscaler	55	
Prescaler	55	
T2CON	55	
Timing Diagrams		
A/D Conversion	175	
Acknowledge Sequence Timing	86	
Baud Rate Generator with Clock Arbitration	80	
BRG Reset Due to SDA Collision	91	
Brown-out Reset	164	
Bus Collision		
START Condition Timing	90	

Bus Collision During a Repeated START Condition (Case 1) .....	92
Bus Collision During a Repeated START Condition (Case2) .....	92
Bus Collision During a START Condition (SCL = 0) .....	91
Bus Collision During a STOP Condition .....	93
Bus Collision for Transmit and Acknowledge .....	89
Capture/Compare/PWM .....	166
CLKOUT and I/O .....	163
I <sup>2</sup> C Bus Data .....	171
I <sup>2</sup> C Bus START/STOP bits .....	170
I <sup>2</sup> C Master Mode First START Bit Timing .....	80
I <sup>2</sup> C Master Mode Reception Timing .....	85
I <sup>2</sup> C Master Mode Transmission Timing .....	83
Master Mode Transmit Clock Arbitration .....	88
Power-up Timer .....	164
Repeat START Condition .....	81
RESET .....	164
SPI Master Mode .....	70
SPI Slave Mode (CKE = 1) .....	71
SPI Slave Mode Timing (CKE = 0) .....	71
Start-up Timer .....	164
STOP Condition Receive or Transmit .....	87
Time-out Sequence on Power-up .....	127, 128
Timer0 .....	165
Timer1 .....	165
USART Asynchronous Master Transmission .....	100
USART Asynchronous Reception .....	102
USART Synchronous Receive .....	173
USART Synchronous Reception .....	108
USART Synchronous Transmission .....	106, 173
USART, Asynchronous Reception .....	104
Wake-up from SLEEP via Interrupt .....	133
Watchdog Timer .....	164
TMR0 .....	17
TMR0 Register .....	15
TMR1CS bit .....	51
TMR1H .....	17
TMR1H Register .....	15
TMR1L .....	17
TMR1L Register .....	15
TMR1ON bit .....	51
TMR2 .....	17
TMR2 Register .....	15
TMR2ON bit .....	55
TOUTPS0 bit .....	55
TOUTPS1 bit .....	55
TOUTPS2 bit .....	55
TOUTPS3 bit .....	55
TRISA Register .....	16
TRISB Register .....	16
TRISC Register .....	16
TRISD Register .....	16
TRISE Register .....	16, 36, 37
IBF Bit .....	37
IBOV Bit .....	37
OBF Bit .....	37
PSPMODE Bit .....	35, 36, 37, 38
TXREG .....	17

TXSTA Register .....	95
BRGH Bit .....	95
CSRC Bit .....	95
SYNC Bit .....	95
TRMT Bit .....	95
TX9 Bit .....	95
TX9D Bit .....	95
TXEN Bit .....	95

## U

UA .....	66
Universal Synchronous Asynchronous Receiver Transmitter. See USART	
Update Address, UA .....	66
USART .....	95
Address Detect Enable (ADDEN Bit) .....	96
Asynchronous Mode .....	99
Asynchronous Receive .....	101
Associated Registers .....	102
Block Diagram .....	101
Asynchronous Receive (9-bit Mode) .....	103
Associated Registers .....	104
Block Diagram .....	103
Timing Diagram .....	104
Asynchronous Receive with Address Detect. See Asynchronous Receive (9-bit Mode).	
Asynchronous Reception .....	102
Asynchronous Transmitter .....	99
Baud Rate Generator (BRG) .....	97
Baud Rate Formula .....	97
Baud Rates, Asynchronous Mode (BRGH=0) ...	98
High Baud Rate Select (BRGH Bit) .....	95
Sampling .....	97
Clock Source Select (CSRC Bit) .....	95
Continuous Receive Enable (CREN Bit) .....	96
Framing Error (FERR Bit) .....	96
Mode Select (SYNC Bit) .....	95
Overrun Error (OERR Bit) .....	96
RC6/TX/CK Pin .....	7, 9
RC7/RX/DT Pin .....	7, 9
RCSTA Register .....	96
Receive Data, 9th bit (RX9D Bit) .....	96
Receive Enable, 9-bit (RX9 Bit) .....	96
Serial Port Enable (SPEN Bit) .....	95, 96
Single Receive Enable (SREN Bit) .....	96
Synchronous Master Mode .....	105
Synchronous Master Reception .....	107
Associated Registers .....	107
Synchronous Master Transmission .....	105
Associated Registers .....	106
Synchronous Slave Mode .....	108
Synchronous Slave Reception .....	109
Associated Registers .....	109
Synchronous Slave Transmit .....	108
Associated Registers .....	108
Transmit Block Diagram .....	99
Transmit Data, 9th Bit (TX9D) .....	95
Transmit Enable (TXEN Bit) .....	95
Transmit Enable, Nine-bit (TX9 Bit) .....	95
Transmit Shift Register Status (TRMT Bit) .....	95
TXSTA Register .....	95

---

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

---

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

#### **Trademarks**

The Microchip name and logo, the Microchip logo, dsPIC, FlashFlex, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC<sup>32</sup> logo, rPIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MTP, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

Analog-for-the-Digital Age, Application Maestro, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniscent Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICTail, REAL ICE, rLAB, Select Mode, SQL, Serial Quad I/O, Total Endurance, TSHARC, UniWinDriver, WiperLock, ZENA and Z-Scale are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

GestIC and ULPP are registered trademarks of Microchip Technology Germany II GmbH & Co. & KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 1998-2013, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

Printed on recycled paper.

ISBN: 9781620769294

**QUALITY MANAGEMENT SYSTEM**  
**CERTIFIED BY DNV**  
**== ISO/TS 16949 ==**

*Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*