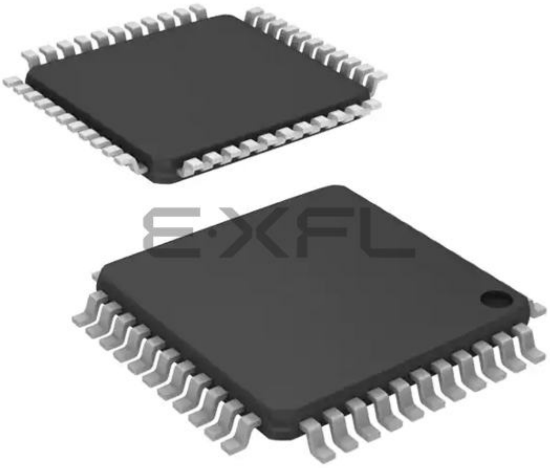


Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	368 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf877t-04i-pt

FIGURE 2-4: PIC16F874/873 REGISTER FILE MAP

Bank 0	File Address	Bank 1	File Address	Bank 2	File Address	Bank 3	File Address
Indirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h	▨	105h	▨	185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
PORTC	07h	TRISC	87h	▨	107h	▨	187h
PORTD(1)	08h	TRISD(1)	88h	▨	108h	▨	188h
PORTE(1)	09h	TRISE(1)	89h	▨	109h	▨	189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	EEDATA	10Ch	EECON1	18Ch
PIR2	0Dh	PIE2	8Dh	EEADR	10Dh	EECON2	18Dh
TMR1L	0Eh	PCON	8Eh	EEDATH	10Eh	Reserved(2)	18Eh
TMR1H	0Fh	▨	8Fh	EEADRH	10Fh	Reserved(2)	18Fh
T1CON	10h	▨	90h	▨	110h	▨	190h
TMR2	11h	SSPCON2	91h				
T2CON	12h	PR2	92h				
SSPBUF	13h	SSPADD	93h				
SSPCON	14h	SSPSTAT	94h				
CCPR1L	15h	▨	95h				
CCPR1H	16h	▨	96h				
CCP1CON	17h	▨	97h				
RCSTA	18h	TXSTA	98h				
TXREG	19h	SPBRG	99h				
RCREG	1Ah	▨	9Ah				
CCPR2L	1Bh	▨	9Bh				
CCPR2H	1Ch	▨	9Ch				
CCP2CON	1Dh	▨	9Dh				
ADRESH	1Eh	ADRESL	9Eh				
ADCON0	1Fh	ADCON1	9Fh				
General Purpose Register 96 Bytes	20h 7Fh	General Purpose Register 96 Bytes	A0h FFh	accesses 20h-7Fh	120h 16Fh 170h 17Fh	accesses A0h - FFh	1A0h 1EFh 1F0h 1FFh

▨ Unimplemented data memory locations, read as '0'.

* Not a physical register.

Note 1: These registers are not implemented on the PIC16F873.

2: These registers are reserved, maintain these registers clear.

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page:
Bank 2											
100h(3)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								`0000 0000`	27
101h	TMR0	Timer0 Module Register								`xxxx xxxx`	47
102h(3)	PCL	Program Counter's (PC) Least Significant Byte								`0000 0000`	26
103h(3)	STATUS	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	`0001 1xxx`	18
104h(3)	FSR	Indirect Data Memory Address Pointer								`xxxx xxxx`	27
105h	—	Unimplemented								—	—
106h	PORTB	PORTB Data Latch when written: PORTB pins when read								`xxxx xxxx`	31
107h	—	Unimplemented								—	—
108h	—	Unimplemented								—	—
109h	—	Unimplemented								—	—
10Ah(1,3)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					`---0 0000`	26
10Bh(3)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	`0000 000x`	20
10Ch	EEDATA	EEPROM Data Register Low Byte								`xxxx xxxx`	41
10Dh	EEADR	EEPROM Address Register Low Byte								`xxxx xxxx`	41
10Eh	EEDATH	—	—	EEPROM Data Register High Byte						`xxxx xxxx`	41
10Fh	EEADRH	—	—	—	EEPROM Address Register High Byte					`xxxx xxxx`	41
Bank 3											
180h(3)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								`0000 0000`	27
181h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	`1111 1111`	19
182h(3)	PCL	Program Counter (PC) Least Significant Byte								`0000 0000`	26
183h(3)	STATUS	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	`0001 1xxx`	18
184h(3)	FSR	Indirect Data Memory Address Pointer								`xxxx xxxx`	27
185h	—	Unimplemented								—	—
186h	TRISB	PORTB Data Direction Register								`1111 1111`	31
187h	—	Unimplemented								—	—
188h	—	Unimplemented								—	—
189h	—	Unimplemented								—	—
18Ah(1,3)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					`---0 0000`	26
18Bh(3)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	`0000 000x`	20
18Ch	EECON1	EEPGD	—	—	—	WRERR	WREN	WR	RD	`x--- x000`	41, 42
18Dh	EECON2	EEPROM Control Register2 (not a physical register)								`---- ----`	41
18Eh	—	Reserved maintain clear								`0000 0000`	—
18Fh	—	Reserved maintain clear								`0000 0000`	—

Legend: `x` = unknown, `u` = unchanged, `q` = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

2: Bits PSPIE and PSPIF are reserved on PIC16F873/876 devices; always maintain these bits clear.

3: These registers can be addressed from any bank.

4: PORTD, PORTE, TRISD, and TRISE are not physically implemented on PIC16F873/876 devices; read as '0'.

5: PIR2<6> and PIE2<6> are reserved on these devices; always maintain these bits clear.

2.2.2.3 INTCON Register

The INTCON Register is a readable and writable register, which contains various enable and flag bits for the TMR0 register overflow, RB Port change and External RB0/INT pin interrupts.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-3: INTCON REGISTER (ADDRESS 0Bh, 8Bh, 10Bh, 18Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
bit 7							bit 0

bit 7 **GIE:** Global Interrupt Enable bit

`1` = Enables all unmasked interrupts
`0` = Disables all interrupts

bit 6 **PEIE**: Peripheral Interrupt Enable bit

`1` = Enables all unmasked peripheral interrupts
`0` = Disables all peripheral interrupts

bit 5 **T0IE**: TMR0 Overflow Interrupt Enable bit

`1` = Enables the TMR0 interrupt
`0` = Disables the TMR0 interrupt

bit 4 **INTE**: RB0/INT External Interrupt Enable bit

`1` = Enables the RB0/INT external interrupt
`0` = Disables the RB0/INT external interrupt

bit 3 **RBIE**: RB Port Change Interrupt Enable bit

`1` = Enables the RB port change interrupt
`0` = Disables the RB port change interrupt

bit 2 **T0IF**: TMR0 Overflow Interrupt Flag bit

`1` = TMR0 register has overflowed (must be cleared in software)
`0` = TMR0 register did not overflow

bit 1 **INTF**: RB0/INT External Interrupt Flag bit

`1` = The RB0/INT external interrupt occurred (must be cleared in software)
`0` = The RB0/INT external interrupt did not occur

bit 0 **RBIF**: RB Port Change Interrupt Flag bit

`1` = At least one of the RB7:RB4 pins changed state; a mismatch condition will continue to set the bit. Reading PORTB will end the mismatch condition and allow the bit to be cleared (must be cleared in software).
`0` = None of the RB7:RB4 pins have changed state

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

NOTES:

4.9 FLASH Program Memory Write Protection

The configuration word contains a bit that write protects the FLASH program memory, called WRT. This bit can only be accessed when programming the PIC16F87X device via ICSP. Once write protection is enabled, only an erase of the entire device will disable it. When enabled, write protection prevents any writes to FLASH program memory. Write protection does not affect program memory reads.

TABLE 4-1: READ/WRITE STATE OF INTERNAL FLASH PROGRAM MEMORY

Configuration Bits			Memory Location	Internal Read	Internal Write	ICSP Read	ICSP Write
CP1	CP0	WRT					
`0`	`0`	`x`	All program memory	Yes	No	No	No
`0`	`1`	`0`	Unprotected areas	Yes	No	Yes	No
`0`	`1`	`0`	Protected areas	Yes	No	No	No
`0`	`1`	`1`	Unprotected areas	Yes	Yes	Yes	No
`0`	`1`	`1`	Protected areas	Yes	No	No	No
`1`	`0`	`0`	Unprotected areas	Yes	No	Yes	No
`1`	`0`	`0`	Protected areas	Yes	No	No	No
`1`	`0`	`1`	Unprotected areas	Yes	Yes	Yes	No
`1`	`0`	`1`	Protected areas	Yes	No	No	No
`1`	`1`	`0`	All program memory	Yes	No	Yes	Yes
`1`	`1`	`1`	All program memory	Yes	Yes	Yes	Yes

TABLE 4-2: REGISTERS ASSOCIATED WITH DATA EEPROM/PROGRAM FLASH

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	`0000 000x`	`0000 000u`
10Dh	EEADR	EEPROM Address Register, Low Byte								`xxxx xxxx`	`uuuu uuuu`
10Fh	EEADRH	—	—	—	EEPROM Address, High Byte					`xxxx xxxx`	`uuuu uuuu`
10Ch	EEDATA	EEPROM Data Register, Low Byte								`xxxx xxxx`	`uuuu uuuu`
10Eh	EEDATH	—	—	EEPROM Data Register, High Byte						`xxxx xxxx`	`uuuu uuuu`
18Ch	EECON1	EEPGD	—	—	—	WRERR	WREN	WR	RD	`x--- x000`	`x--- u000`
18Dh	EECON2	EEPROM Control Register2 (not a physical register)								—	—
8Dh	PIE2	—	**(1)**	—	EEIE	BCLIE	—	—	CCP2IE	`-r-0 0--0`	`-r-0 0--0`
0Dh	PIR2	—	**(1)**	—	EEIF	BCLIF	—	—	CCP2IF	`-r-0 0--0`	`-r-0 0--0`

Legend: `x` = unknown, `u` = unchanged, `r` = reserved, `-` = unimplemented, read as '0'.
Shaded cells are not used during FLASH/EEPROM access.

Note 1: These bits are reserved; always maintain these bits clear.

TABLE 8-5: REGISTERS ASSOCIATED WITH PWM AND TIMER2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh,8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	`0000 000x`	`0000 000u`
0Ch	PIR1	PSPIF[(1)]	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	`0000 0000`	`0000 0000`
0Dh	PIR2	—	—	—	—	—	—	—	CCP2IF	`---- ---0`	`---- ---0`
8Ch	PIE1	PSPIE[(1)]	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	`0000 0000`	`0000 0000`
8Dh	PIE2	—	—	—	—	—	—	—	CCP2IE	`---- ---0`	`---- ---0`
87h	TRISC	PORTC Data Direction Register								`1111 1111`	`1111 1111`
11h	TMR2	Timer2 Module's Register								`0000 0000`	`0000 0000`
92h	PR2	Timer2 Module's Period Register								`1111 1111`	`1111 1111`
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	`-000 0000`	`-000 0000`
15h	CCPR1L	Capture/Compare/PWM Register1 (LSB)								`xxxx xxxx`	`uuuu uuuu`
16h	CCPR1H	Capture/Compare/PWM Register1 (MSB)								`xxxx xxxx`	`uuuu uuuu`
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	`--00 0000`	`--00 0000`
1Bh	CCPR2L	Capture/Compare/PWM Register2 (LSB)								`xxxx xxxx`	`uuuu uuuu`
1Ch	CCPR2H	Capture/Compare/PWM Register2 (MSB)								`xxxx xxxx`	`uuuu uuuu`
1Dh	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	`--00 0000`	`--00 0000`

Legend: `x` = unknown, `u` = unchanged, `-` = unimplemented, read as '0'. Shaded cells are not used by PWM and Timer2.

Note 1: Bits PSPIE and PSPIF are reserved on the PIC16F873/876; always maintain these bits clear.

REGISTER 9-1: SSPSTAT: SYNC SERIAL PORT STATUS REGISTER (ADDRESS: 94h)

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE	D/$\overline{\text{A}}$	P	S	R/$\overline{\text{W}}$	UA	BF
bit 7							bit 0

bit 7 **SMP:** Sample bit
SPI Master mode:
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time
SPI Slave mode:
SMP must be cleared when SPI is used in slave mode
In I^{2}C Master or Slave mode:
1 = Slew rate control disabled for standard speed mode (100 kHz and 1 MHz)
0 = Slew rate control enabled for high speed mode (400 kHz)

bit 6 **CKE**: SPI Clock Edge Select (Figure 9-2, Figure 9-3 and Figure 9-4)
SPI mode:
For CKP = 0
1 = Data transmitted on rising edge of SCK
0 = Data transmitted on falling edge of SCK
For CKP = 1
1 = Data transmitted on falling edge of SCK
0 = Data transmitted on rising edge of SCK
In I^{2}C Master or Slave mode:
1 = Input levels conform to SMBus spec
0 = Input levels conform to I^{2}C specs

bit 5 **D/A**: Data/$\overline{\text{Address}}$ bit (I^{2}C mode only)
1 = Indicates that the last byte received or transmitted was data
0 = Indicates that the last byte received or transmitted was address

bit 4 **P**: STOP bit
(I^{2}C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.)
1 = Indicates that a STOP bit has been detected last (this bit is '0' on RESET)
0 = STOP bit was not detected last

bit 3 **S**: START bit
(I^{2}C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.)
1 = Indicates that a START bit has been detected last (this bit is '0' on RESET)
0 = START bit was not detected last

bit 2 **R/W**: Read/Write bit Information (I^{2}C mode only)
This bit holds the R/W bit information following the last address match. This bit is only valid from the address match to the next START bit, STOP bit or not $\overline{\text{ACK}}$ bit.
In I^{2}C Slave mode:
1 = Read
0 = Write
In I^{2}C Master mode:
1 = Transmit is in progress
0 = Transmit is not in progress
Logical OR of this bit with SEN, RSEN, PEN, RCEN, or ACKEN will indicate if the MSSP is in IDLE mode.

bit 1 **UA**: Update Address (10-bit I^{2}C mode only)
1 = Indicates that the user needs to update the address in the SSPADD register
0 = Address does not need to be updated

bit **BF**: Buffer Full Status bit
Receive (SPI and I^{2}C modes):
1 = Receive complete, SSPBUF is full
0 = Receive not complete, SSPBUF is empty
Transmit (I^{2}C mode only):
1 = Data transmit in progress (does not include the $\overline{\text{ACK}}$ and STOP bits), SSPBUF is full
0 = Data transmit complete (does not include the $\overline{\text{ACK}}$ and STOP bits), SSPBUF is empty

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

9.2.11 I^{2}C MASTER MODE TRANSMISSION

Transmission of a data byte, a 7-bit address, or either half of a 10-bit address, is accomplished by simply writing a value to SSPBUF register. This action will set the Buffer Full flag (BF) and allow the baud rate generator to begin counting and start the next transmission. Each bit of address/data will be shifted out onto the SDA pin after the falling edge of SCL is asserted (see data hold time spec). SCL is held low for one baud rate generator rollover count (TBRG). Data should be valid before SCL is released high (see data setup time spec). When the SCL pin is released high, it is held that way for TBRG. The data on the SDA pin must remain stable for that duration and some hold time after the next falling edge of SCL. After the eighth bit is shifted out (the falling edge of the eighth clock), the BF flag is cleared and the master releases SDA allowing the slave device being addressed to respond with an $\overline{\text{ACK}}$ bit during the ninth bit time, if an address match occurs or if data was received properly. The status of $\overline{\text{ACK}}$ is read into the ACKDT on the falling edge of the ninth clock. If the master receives an Acknowledge, the Acknowledge Status bit (ACKSTAT) is cleared. If not, the bit is set. After the ninth clock, the SSPIF is set and the master clock (baud rate generator) is suspended until the next data byte is loaded into the SSPBUF, leaving SCL low and SDA unchanged (Figure 9-14).

After the write to the SSPBUF, each bit of address will be shifted out on the falling edge of SCL, until all seven address bits and the R/$\overline{\text{W}}$ bit are completed. On the falling edge of the eighth clock, the master will de-assert the SDA pin, allowing the slave to respond with an Acknowledge. On the falling edge of the ninth clock, the master will sample the SDA pin to see if the address was recognized by a slave. The status of the ACK bit is loaded into the ACKSTAT status bit (SSPCON2<6>). Following the falling edge of the ninth clock transmission of the address, the SSPIF is set, the BF flag is cleared, and the baud rate generator is turned off until another write to the SSPBUF takes place, holding SCL low and allowing SDA to float.

9.2.11.1 BF Status Flag

In Transmit mode, the BF bit (SSPSTAT<0>) is set when the CPU writes to SSPBUF and is cleared when all 8 bits are shifted out.

9.2.11.2 WCOL Status Flag

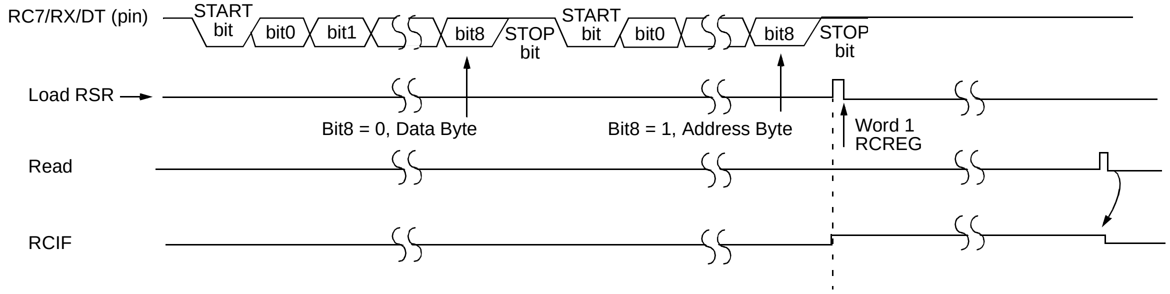
If the user writes the SSPBUF when a transmit is already in progress (i.e., SSPSR is still shifting out a data byte), then WCOL is set and the contents of the buffer are unchanged (the write doesn’t occur).

WCOL must be cleared in software.

9.2.11.3 ACKSTAT Status Flag

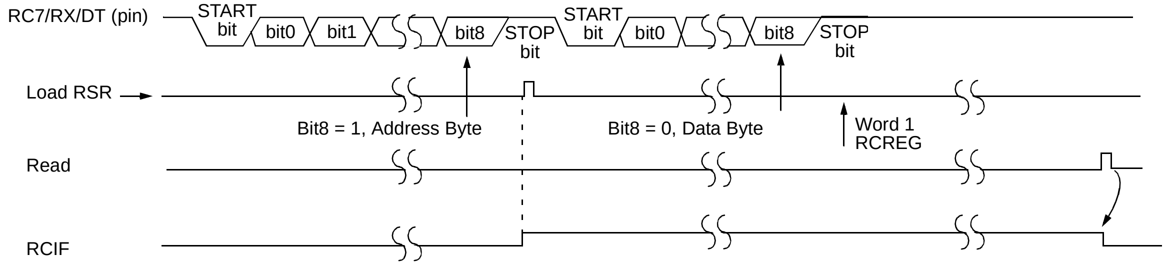
In Transmit mode, the ACKSTAT bit (SSPCON2<6>) is cleared when the slave has sent an Acknowledge ($\overline{\text{ACK}}$ = 0), and is set when the slave does not Acknowledge ($\overline{\text{ACK}}$ = 1). A slave sends an Acknowledge when it has recognized its address (including a general call), or when the slave has properly received its data.

FIGURE 10-7: ASYNCHRONOUS RECEPTION WITH ADDRESS DETECT



Note: This timing diagram shows a data byte followed by an address byte. The data byte is not read into the RCREG (receive buffer) because ADDEN = 1.

FIGURE 10-8: ASYNCHRONOUS RECEPTION WITH ADDRESS BYTE FIRST



Note: This timing diagram shows a data byte followed by an address byte. The data byte is not read into the RCREG (receive buffer) because ADDEN was not updated and still = 0.

TABLE 10-7: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh, 8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	R0IF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
1Ah	RCREG	USART Receive Register								0000 0000	0000 0000
8Ch	PIE1	PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for asynchronous reception.

Note 1: Bits PSPIE and PSPIF are reserved on PIC16F873/876 devices; always maintain these bits clear.

15.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Ambient temperature under bias	-55 to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to V_{SS} (except V_{DD}, $\overline{MCLR}$. and RA4)	-0.3 V to (V_{DD} + 0.3 V)
Voltage on V_{DD} with respect to V_{SS}	-0.3 to +7.5 V
Voltage on $\overline{MCLR}$ with respect to V_{SS} **(Note 2)**	0 to +14 V
Voltage on RA4 with respect to Vss	0 to +8.5 V
Total power dissipation **(Note 1)**	1.0 W
Maximum current out of V_{SS} pin	300 mA
Maximum current into V_{DD} pin	250 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	± 20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by PORTA, PORTB, and PORTE (combined) **(Note 3)**	200 mA
Maximum current sourced by PORTA, PORTB, and PORTE (combined) **(Note 3)**	200 mA
Maximum current sunk by PORTC and PORTD (combined) **(Note 3)**	200 mA
Maximum current sourced by PORTC and PORTD (combined) **(Note 3)**	200 mA

Note 1: Power dissipation is calculated as follows: $Pdis = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{Ol} \times I_{OL})$

2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin, rather than pulling this pin directly to V_{SS}.

3: PORTD and PORTE are not implemented on PIC16F873/876 devices.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

15.1 DC Characteristics: PIC16F873/874/876/877-04 (Commercial, Industrial)
PIC16F873/874/876/877-20 (Commercial, Industrial)
PIC16LF873/874/876/877-04 (Commercial, Industrial) (Continued)

PIC16LF873/874/876/877-04 (Commercial, Industrial)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial 0°C ≤ TA ≤ +70°C for commercial				
PIC16F873/874/876/877-04 **PIC16F873/874/876/877-20** (Commercial, Industrial)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Symbol**	**Characteristic/ Device**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	IDD	**Supply Current[(2,5)]**					
D010		16LF87X	—	0.6	2.0	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 3.0V
D010		16F87X	—	1.6	4	mA	RC osc configurations FOSC = 4 MHz, VDD = 5.5V
D010A		16LF87X	—	20	35	µA	LP osc configuration FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D013		16F87X	—	7	15	mA	HS osc configuration, FOSC = 20 MHz, VDD = 5.5V
D015	ΔIBOR	**Brown-out Reset Current[(6)]**	—	85	200	µA	BOR enabled, VDD = 5.0V

Legend: Rows with standard voltage device data only are shaded for improved readability.

† Data in “Typ” column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading, switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

$\underline{\text{OSC1}}$ = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD;
$\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

7: When BOR is enabled, the device will operate correctly until the VBOR voltage trip point is reached.

15.1 DC Characteristics: PIC16F873/874/876/877-04 (Commercial, Industrial)
PIC16F873/874/876/877-20 (Commercial, Industrial)
PIC16LF873/874/876/877-04 (Commercial, Industrial) (Continued)

PIC16LF873/874/876/877-04 (Commercial, Industrial)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial 0°C ≤ TA ≤ +70°C for commercial				
PIC16F873/874/876/877-04 **PIC16F873/874/876/877-20** (Commercial, Industrial)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Symbol**	**Characteristic/ Device**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	IPD	**Power-down Current(3,5)**					
D020		16LF87X	—	7.5	30	µA	VDD = 3.0V, WDT enabled, -40°C to +85°C
D020		16F87X	—	10.5	42	µA	VDD = 4.0V, WDT enabled, -40°C to +85°C
D021		16LF87X	—	0.9	5	µA	VDD = 3.0V, WDT enabled, 0°C to +70°C
D021		16F87X	—	1.5	16	µA	VDD = 4.0V, WDT enabled, -40°C to +85°C
D021A		16LF87X		0.9	5	µA	VDD = 3.0V, WDT enabled, -40°C to +85°C
D021A		16F87X		1.5	19	µA	VDD = 4.0V, WDT enabled, -40°C to +85°C
D023	ΔIBOR	**Brown-out Reset Current(6)**	—	85	200	µA	BOR enabled, VDD = 5.0V

Legend: Rows with standard voltage device data only are shaded for improved readability.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading, switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

$\overline{\text{OSC1}}$ = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD;

$\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

7: When BOR is enabled, the device will operate correctly until the VBOR voltage trip point is reached.

15.3 DC Characteristics: PIC16F873/874/876/877-04 (Extended)
PIC16F873/874/876/877-10 (Extended)

PIC16F873/874/876/877-04 **PIC16F873/874/876/877-20** (Extended)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +125°C				
Param No.	**Symbol**	**Characteristic/ Device**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VDD	**Supply Voltage**					
D001			4.0	—	5.5	V	LP, XT, RC osc configuration
D001A			4.5		5.5	V	HS osc configuration
D001A			VBOR		5.5	V	BOR enabled, FMAX = 10 MHz(7)
D002	VDR	**RAM Data Retention Voltage(1)**	—	1.5	—	V	
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	VSS	—	V	See section on Power-on Reset for details
D004	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See section on Power-on Reset for details
D005	VBOR	**Brown-out Reset Voltage**	3.7	4.0	4.35	V	BODEN bit in configuration word enabled

† Data is “Typ” column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading, switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD;
$\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

7: When BOR is enabled, the device will operate correctly until the VBOR voltage trip point is reached.

15.3 DC Characteristics: PIC16F873/874/876/877-04 (Extended) PIC16F873/874/876/877-10 (Extended) (Continued)

PIC16F873/874/876/877-04 **PIC16F873/874/876/877-20** (Extended)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ T_A ≤ +125°C				
Param No.	**Symbol**	**Characteristic/ Device**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	I_{DD}	**Supply Current[(2,5)]**					
D010			—	1.6	4	mA	RC osc configurations F_{OSC} = 4 MHz, V_{DD} = 5.5V
D013			—	7	15	mA	HS osc configuration, F_{OSC} = 10 MHz, V_{DD} = 5.5V
D015	ΔI_{BOR}	**Brown-out Reset Current[(6)]**	—	85	200	μA	BOR enabled, V_{DD} = 5.0V
	I_{PD}	**Power-down Current[(3,5)]**					
D020A				10.5	60	μA	V_{DD} = 4.0V, WDT enabled
D021B				1.5	30	μA	V_{DD} = 4.0V, WDT disabled
D023	ΔI_{BOR}	**Brown-out Reset Current[(6)]**	—	85	200	μA	BOR enabled, V_{DD} = 5.0V

† Data is “Typ” column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which V_{DD} can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading, switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.

The test conditions for all I_{DD} measurements in active operation mode are:

$\overline{\text{OSC1}}$ = external square wave, from rail to rail; all I/O pins tri-stated, pulled to V_{DD};
$\overline{\text{MCLR}}$ = V_{DD}; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V_{DD} and V_{SS}.

4: For RC osc configuration, current through R_{EXT} is not included. The current through the resistor can be estimated by the formula Ir = $V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in kOhm.

5: Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base I_{DD} or I_{PD} measurement.

7: When BOR is enabled, the device will operate correctly until the V_{BOR} voltage trip point is reached.

15.4 DC Characteristics: PIC16F873/874/876/877-04 (Extended)
PIC16F873/874/876/877-10 (Extended) (Continued)

DC CHARACTERISTICS	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ T_A ≤ +125°C Operating voltage V_{DD} range as described in DC specification (Section 15.1)

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	V_{OL}	**Output Low Voltage**					
D080A		I/O ports	—	—	0.6	V	I_{OL} = 7.0 mA, V_{DD} = 4.5V
D083A		OSC2/CLKOUT (RC osc config)	—	—	0.6	V	I_{OL} = 1.2 mA, V_{DD} = 4.5V
	V_{OH}	**Output High Voltage**					
D090A		I/O ports[(3)]	V_{DD} - 0.7	—	—	V	I_{OH} = -2.5 mA, V_{DD} = 4.5V
D092A		OSC2/CLKOUT (RC osc config)	V_{DD} - 0.7	—	—	V	I_{OH} = -1.0 mA, V_{DD} = 4.5V
D150*	V_{OD}	**Open Drain High Voltage**	—	—	8.5	V	RA4 pin
		Capacitive Loading Specs on Output Pins					
D100	C_{OSC2}	OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101	C_{IO}	All I/O pins and OSC2 (RC mode)	—	—	50	pF	
D102	C_B	SCL, SDA (I^2C mode)	—	—	400	pF	
		Data EEPROM Memory					
D120	E_D	Endurance	100K	—	—	E/W	25°C at 5V
D121	V_{DRW}	V_{DD} for read/write	V_{MIN}	—	5.5	V	Using EECON to read/write V_{MIN} = min. operating voltage
D122	T_{DEW}	Erase/write cycle time	—	4	8	ms	
		Program FLASH Memory					
D130	E_P	Endurance	1000	—	—	E/W	25°C at 5V
D131	V_{PR}	V_{DD} for read	V_{MIN}	—	5.5	V	V_{MIN} = min operating voltage
D132A		V_{DD} for erase/write	V_{MIN}	—	5.5	V	Using EECON to read/write, V_{MIN} = min. operating voltage
D133	T_{PEW}	Erase/Write cycle time	—	4	8	ms	

* These parameters are characterized but not tested.

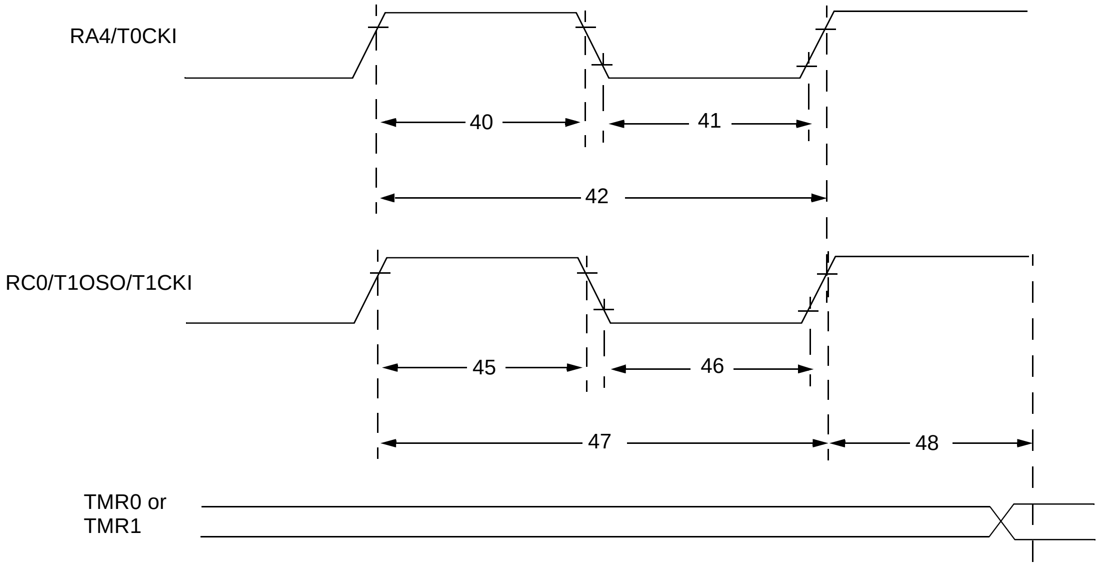
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16F87X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

FIGURE 15-10: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS



Note: Refer to Figure 15-5 for load conditions.

TABLE 15-4: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param No.	Symbol	Characteristic			Min	Typ†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse Width		No Prescaler	0.5TCY + 20	—	—	ns	Must also meet parameter 42
				With Prescaler	10	—	—	ns	
41*	Tt0L	T0CKI Low Pulse Width		No Prescaler	0.5TCY + 20	—	—	ns	Must also meet parameter 42
				With Prescaler	10	—	—	ns	
42*	Tt0P	T0CKI Period		No Prescaler	TCY + 40	—	—	ns	
				With Prescaler	Greater of: 20 or $\frac{\mathrm{TCY} + 40}{N}$	—	—	ns	N = prescale value (2, 4,..., 256)
45*	Tt1H	T1CKI High Time	Synchronous, Prescaler = 1		0.5TCY + 20	—	—	ns	Must also meet parameter 47
			Synchronous, Prescaler = 2,4,8	Standard(**F**)	15	—	—	ns	
				Extended(**LF**)	25	—	—	ns	
			Asynchronous	Standard(**F**)	30	—	—	ns	
				Extended(**LF**)	50	—	—	ns	
46*	Tt1L	T1CKI Low Time	Synchronous, Prescaler = 1		0.5TCY + 20	—	—	ns	Must also meet parameter 47
			Synchronous, Prescaler = 2,4,8	Standard(**F**)	15	—	—	ns	
				Extended(**LF**)	25	—	—	ns	
			Asynchronous	Standard(**F**)	30	—	—	ns	
				Extended(**LF**)	50	—	—	ns	
47*	Tt1P	T1CKI input period	Synchronous	Standard(**F**)	Greater of: 30 OR $\frac{\mathrm{TCY} + 40}{N}$	—	—	ns	N = prescale value (1, 2, 4, 8)
				Extended(**LF**)	Greater of: 50 OR $\frac{\mathrm{TCY} + 40}{N}$				N = prescale value (1, 2, 4, 8)
			Asynchronous	Standard(**F**)	60	—	—	ns	
				Extended(**LF**)	100	—	—	ns	
	Ft1	Timer1 oscillator input frequency range (oscillator enabled by setting bit T1OSCEN)			DC	—	200	kHz	
48	TCKEZtmr1	Delay from external clock edge to timer increment			2TOSC	—	7TOSC	—	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 16-15: AVERAGE WDT PERIOD vs. VDD OVER TEMPERATURE (-40°C TO 125°C)

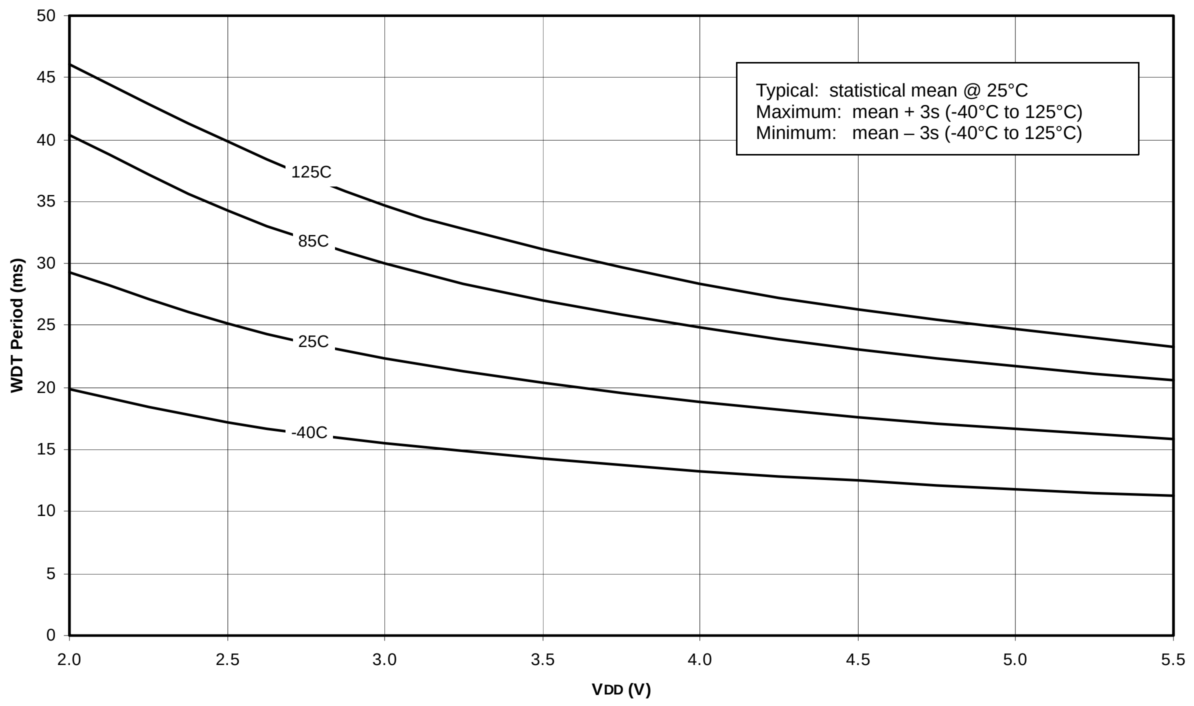
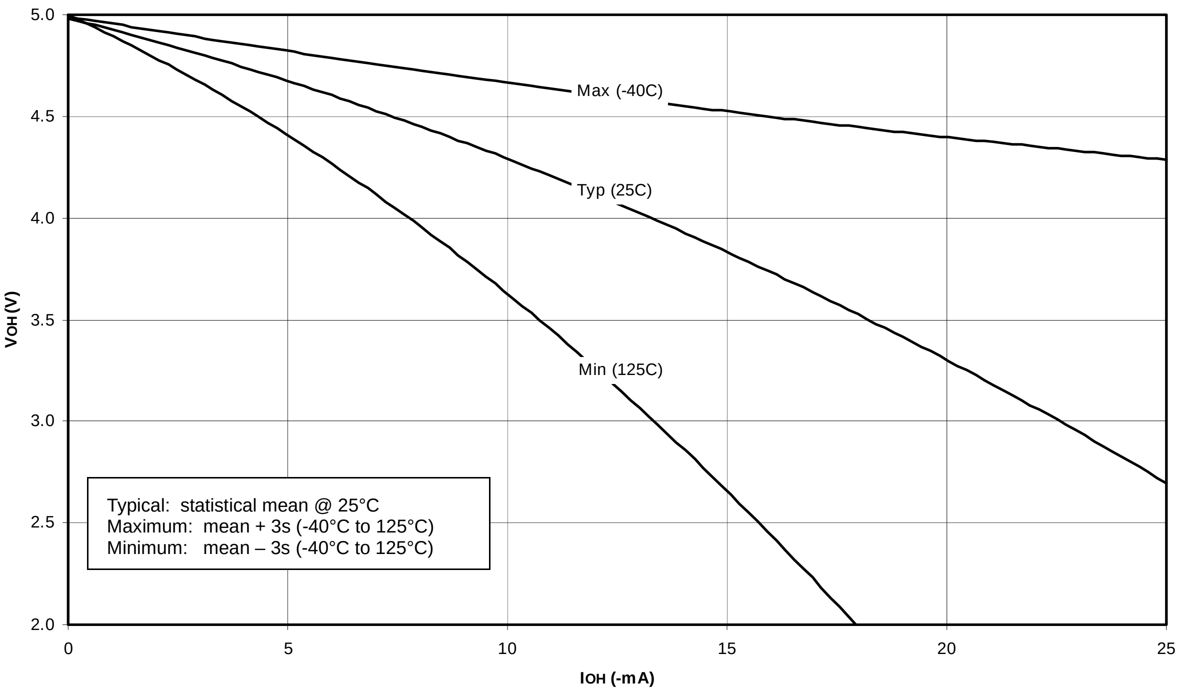


FIGURE 16-16: TYPICAL, MINIMUM AND MAXIMUM VOH vs. IOH (VDD=5V, -40°C TO 125°C)



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