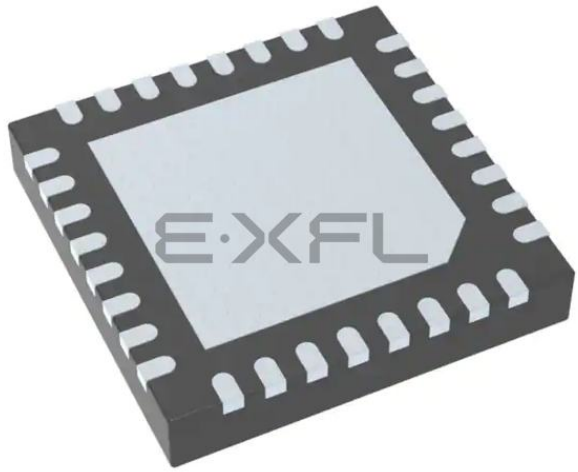

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	16MHz
Connectivity	SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	20
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 11x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at90pwm161-16mn

When using the SEI instruction to enable interrupts, the instruction following SEI will be executed before any pending interrupts, as shown in this example.

Assembly code example

```
sei  ; set Global Interrupt Enable
sleep; enter sleep, waiting for interrupt
; note: will enter sleep before any pending
; interrupt(s)
```

C code example

```
_SEI(); /* set Global Interrupt Enable */
_SLEEP(); /* enter sleep, waiting for interrupt */
/* note: will enter sleep before any pending interrupt(s) */
```

3.8.2 Interrupt Response Time

The interrupt execution response for all the enabled AVR interrupts is four clock cycles minimum. After four clock cycles the program vector address for the actual interrupt handling routine is executed. During this four clock cycle period, the Program Counter is pushed onto the Stack. The vector is normally a jump to the interrupt routine, and this jump takes three clock cycles. If an interrupt occurs during execution of a multi-cycle instruction, this instruction is completed before the interrupt is served. If an interrupt occurs when the MCU is in sleep mode, the interrupt execution response time is increased by four clock cycles. This increase comes in addition to the start-up time from the selected sleep mode.

A return from an interrupt handling routine takes four clock cycles. During these four clock cycles, the Program Counter (two bytes) is popped back from the Stack, the Stack Pointer is incremented by two, and the I-bit in SREG is set.

The switch between 8MHz and 1MHz is done by the CKRC81 bit in MCUCR register. See "MCUCR - MCU Control Register" on page 42 for more details.The RC oscillator can be accessed by two CKSEL or CSEL configurations. At reset, the CKRC81 bit is initialised with the value compatible with CKSEL value (1 for CKSEL3..0 = 0110, 0 for all other values).

The RC oscillator is active for any CKSEL3..0 or CSEL3..0 configuration where it is used as system clock or PLL source clock. The RC oscillator is diabled in the following CKSEL3..0 or CSEL3..0 cases:

- 0011 (128k oscillator)
- 0100, 0101 (PLL/4 system clock driven by external clock or oscillator)
- 1100, 1101 (External oscillator)

The device is shipped with the CKDIV8 Fuse programmed. See "System Clock Prescaler" on page 39 for more details. This clock may be selected as the system clock by programming the CKSEL Fuses or CSEL field as shown in Table 5-1 on page 28. If selected, it will operate with no external components. During reset, hardware loads the calibration byte into the OSCCAL Register and thereby automatically calibrates the RC Oscillator. The accuracy of this calibration is shown as Factory calibration in Table 22-1 on page 270.

By changing the OSCCAL register from SW, see "OSCCAL – Oscillator Calibration Register" on page 39, it is possible to get a higher calibration accuracy than by using the factory calibration. The accuracy of this calibration is shown as User calibration in Table 22-1 on page 270.

When this Oscillator is used as the chip clock, the Watchdog Oscillator will still be used for the Watchdog Timer and for the Reset Time-out. For more information on the pre-programmed calibration value, see the section "Calibration Byte" on page 252.

Table 5-3. Internal calibrated RC oscillator operating modes (1)(3).

Frequency range (2) (MHz)	CKSEL3..0
7.6 - 8.4	0010
0.95 - 1.05 (4)	0010

Notes: 1. The device is shipped with this option selected.
2. The frequency ranges are preliminary values. Actual values are TBD.
3. If 8MHz frequency exceeds the specification of the device (depends on V_{CC}), the CKDIV8 Fuse can be programmed in order to divide the internal frequency by 8.
4. Switch between 8MHz and 1MHz is done by CKRC81 bit in MCUCR register.

When this oscillator is selected, start-up times are determined by the SUT Fuses as shown in Table 5-4 on page 30.

Table 5-4. Start-up times for the internal calibrated RC Oscillator clock selection.

Power conditions	Start-up time from power-down	Additional delay from reset (V_{CC} = 5.0V)	SUT1..0
BOD enabled	6CK	14CK (1)	00
Fast rising power	6CK	14CK + 4.1ms	01
Slowly rising power	6CK	14CK + 65ms (2)	10
Reserved			11

Note: 1. If the RSTDISBL fuse is programmed, this start-up time will be increased to 14CK + 4.1ms to ensure programming mode can be entered.
2. The device is shipped with this option selected.

Figure 7-2. MCU start-up, $\overline{\text{RESET}}$ tied to V_{CC}.

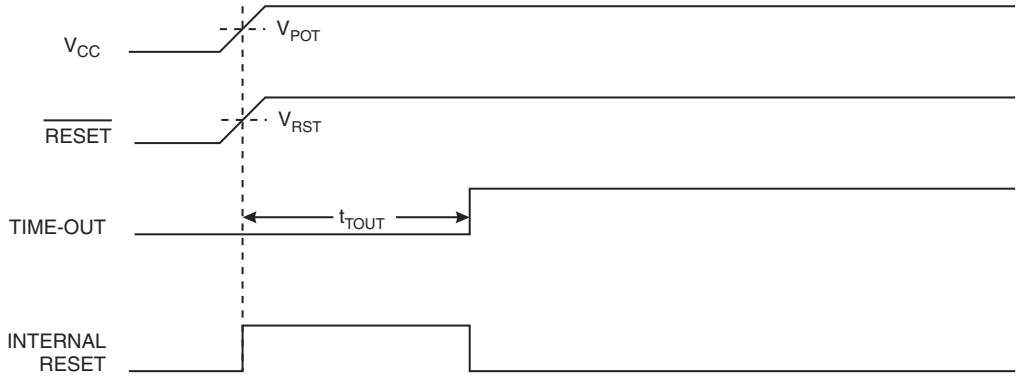
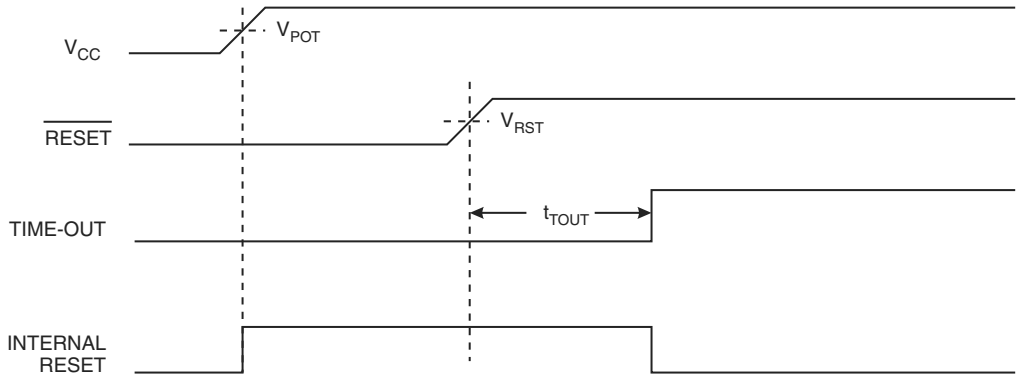


Figure 7-3. MCU start-up, $\overline{\text{RESET}}$ extended externally.



7.1.4 External Reset

An External Reset is generated by a low level on the $\overline{\text{RESET}}$ pin. Reset pulses longer than the minimum pulse width (see Table 7-1 on page 51) will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset. When the applied signal reaches the Reset Threshold Voltage – V_{RST} – on its positive edge, the delay counter starts the MCU after the Time-out period – t_{TOUT} – has expired.

Figure 7-4. External reset during operation.

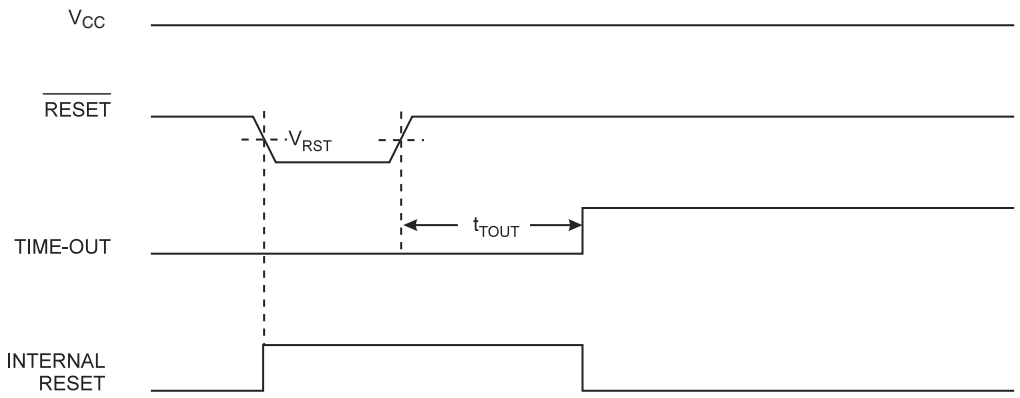


Table 7-6. Watchdog timer prescaler select.

WDP3	WDP2	WDP1	WDP0	Number of WDT oscillator cycles	Typical time-out at V_{CC} = 5.0V
0	0	0	0	2K (2048) cycles	16ms
0	0	0	1	4K (4096) cycles	32ms
0	0	1	0	8K (8192) cycles	64ms
0	0	1	1	16K (16384) cycles	0.125s
0	1	0	0	32K (32768) cycles	0.25s
0	1	0	1	64K (65536) cycles	0.5s
0	1	1	0	128K (131072) cycles	1.0s
0	1	1	1	256K (262144) cycles	2.0s
1	0	0	0	512K (524288) cycles	4.0s
1	0	0	1	1024K (1048576) cycles	8.0s
1	0	1	0	1K (1024) cycles	8ms
1	0	1	1	512 cycles	4ms
1	1	0	0	256 cycles	2ms
1	1	0	1	128 cycles	1ms
1	1	1	0	Reserved	
1	1	1	1		

The following code examples show how to do an atomic read of the TCNT1 Register contents. Reading any of the OCR1A/B or ICR1 Registers can be done by using the same principle.

Assembly code example (1)

```
TIM16_ReadTCNT1:
  ; Save global interrupt flag
  in  r18,SREG
  ; Disable interrupts
  cli
  ; Read TCNT1 into r17:r16
  in  r16,TCNT1L
  in  r17,TCNT1H
  ; Restore global interrupt flag
  out SREG,r18
  ret
```

C code example (1)

```
unsigned int TIM16_ReadTCNT1( void )
{
  unsigned char sreg;
  unsigned int i;
  /* Save global interrupt flag */
  sreg = SREG;
  /* Disable interrupts */
  _CLI();
  /* Read TCNT1 into i */
  i = TCNT1;
  /* Restore global interrupt flag */
  SREG = sreg;
  return i;
}
```

Note: 1. The example code assumes that the part specific header file is included.
For I/O Registers located in extended I/O map, “IN”, “OUT”, “SBIS”, “SBIC”, “CBI”, and “SBI” instructions must be replaced with instructions that allow access to extended I/O. Typically “LDS” and “STS” combined with “SBRS”, “SBRC”, “SBR”, and “CBR”.

The assembly code example returns the TCNT1 value in the r17:r16 register pair.

- In 2- or 4-ramp mode, PSCn Input A is taken into account only during Dead-Time0 and On-Time0 period (respectively Dead-Time1 and On-Time1 for PSCn Input B).

- In 1-ramp-mode PSC Input A or PSC Input B act on the whole ramp.

12.8.4.3 Input Mode Operation

Thanks to 4 configuration bits (PRFM3:0), it's possible to define the mode of the PSC input. Thanks to four configuration bits (PRFM3:0), it is possible to define all the modes of the PSCR input. These modes are listed in Table 12-7.

Table 12-7. PSC input mode operation.

	PRFM3:0	Description
0	0000b	PSCn input has no action on PSC output
1	0001b	See "PSC Input Mode 1: Stop signal, Jump to Opposite Dead-Time and Wait" on page 121.
2	0010b	See "PSC Input Mode 2: Stop signal, Execute Opposite Pulse and Wait" on page 122.
3	0011b	See "PSC Input Mode 3: Stop signal, Execute Opposite Pulse while Fault active" on page 123.
4	0100b	See "PSC Input Mode 4: Deactivate outputs without changing timing" on page 124.
5	0101b	See "PSC Input Mode 5: Stop signal and Insert Dead-Time" on page 124.
6	0110b	See "PSC Input Mode 6: Stop signal, Jump to Opposite Dead-Time and Wait" on page 125.
7	0111b	See "PSC Input Mode 7: Halt PSC and Wait for Software Action" on page 125.
8	1000b	See "PSC Input Mode 8: Edge Retrigger PSC" on page 126.
9	1001b	See "PSC Input Mode 9: Fixed Frequency Edge Retrigger PSC" on page 127.
10	1010b	Reserved: Do not use
11	1011b	
12	1100b	
13	1101b	
14	1110b	See "PSC Input Mode 14: Fixed Frequency Edge Retrigger PSC and Deactivate Output" on page 128.
15	1111b	Reserved: Do not use

Note: All following examples are given with rising edge or high level active inputs.

12.24 Interrupts

This section describes the specifics of the interrupt handling as performed in AT90PWM81/161.

12.24.1 List of Interrupt Vector

Each PSC provides three interrupt vectors

- **PSCn EC (End of Cycle**): When enabled and when a match with OCRnRB occurs
- **PSCn EEC (End of Enhanced Cycle**): When enabled and when a match with OCRnRB occurs at the 15th enhanced cycle
- **PSCn CAPT (Capture Event)**: When enabled and one of the two following events occurs: retrigger, capture of the PSC counter or Synchro Error.

See “PIM2 - PSC2 Interrupt Mask Register” on page 143.

12.25 PSC Register Definition

Registers are explained for PSC0. They are identical for PSC1. For PSC2 only different registers are described.

12.25.1 PSOC2 - PSC 2 Synchro and Output Configuration

Bit	7	6	5	4	3	2	1	0	
	POS23	POS22	PSYNC21	PSYNC20	POEN2D	POEN2B	POEN2C	POEN2A	PSOC2
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – POS23: PSCOUT23 Selection (PSC2 only)**

When this bit is clear, PSCOUT23 outputs the waveform generated by Waveform Generator B.

When this bit is set, PSCOUT23 outputs the waveform generated by Waveform Generator A.

- **Bit 6 – POS22: PSCOUT22 Selection (PSC2 only)**

When this bit is clear, PSCOUT22 outputs the waveform generated by Waveform Generator A.

When this bit is set, PSCOUT22 outputs the waveform generated by Waveform Generator B.

- **Bit 5:4 – PSYNCn1:0: Synchronization Out for ADC Selection**

Select the polarity and signal source for generating a signal which will be sent to the ADC for synchronization.

Table 12-11. Synchronization source description in one/two/four ramp modes.

PSYNCn1	PSYNCn0	Description
0	0	Send signal on leading edge of PSCOUTn0 (match with OCRnSA)
0	1	Send signal on trailing edge of PSCOUTn0 (match with OCRnRA or fault/retrigger on part A)
1	0	Send signal on leading edge of PSCOUTn1 (match with OCRnSB)
1	1	Send signal on trailing edge of PSCOUTn1 (match with OCRnRB or fault/retrigger on part B)

Table 12-22. PSC n ramp number description.

PRNn1	PRNn0	Description
0	0	The last event which has generated an interrupt occurred during ramp 1
0	1	The last event which has generated an interrupt occurred during ramp 2
1	0	The last event which has generated an interrupt occurred during ramp 3
1	1	The last event which has generated an interrupt occurred during ramp 4

- **Bit 0 – PEOPn: End Of PSC n Interrupt**

This bit is set by hardware when PSC n achieves its whole cycle.

Must be cleared by software by writing a one to its location.

12.26.4 PSC Output Behavior During Reset

For external component safety reason, the state of PSC outputs during Reset can be programmed by fuses PSCRV, PSCRRB & PSC2RB.

These fuses are located in the Extended Fuse Byte:

Table 12-23. Extended Low Fuse byte.

Extended fuse byte	Bit No	Description	Default value
PSC2RB	7	PSC2 reset behavior	1
PSC2RBA	6	PSC2 reset behavior for OUT22 & 23	1
PSCRRB	5	PSC reduced reset behavior	1
PSCRV	4	PSCOUT & PSCOUTR reset value	1
PSCINRB	3	PSC & PSCR inputs reset behavior	1
BODLEVEL2 (1)	2	Brown-out detector trigger level	1 (unprogrammed)
BODLEVEL1 (1)	1	Brown-out detector trigger level	0 (programmed)
BODLEVEL0 (1)	0	Brown-out detector trigger level	1 (unprogrammed)

Notes: 1. See Table 7-2 on page 53 for BODLEVEL Fuse decoding.

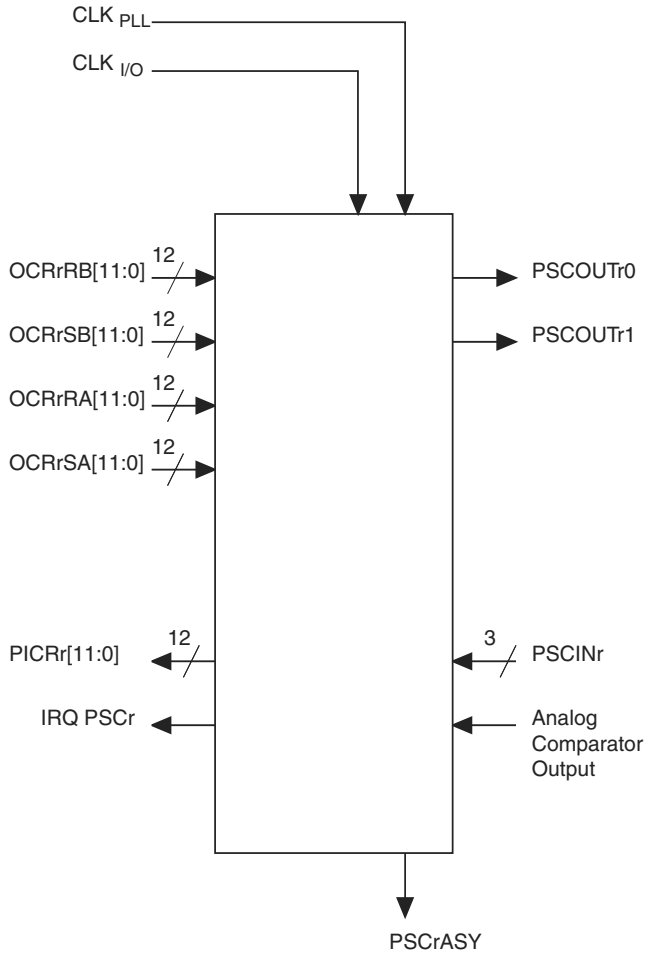
PSCRV gives the state low or high which will be forced on PSC outputs selected by PSC0RB & PSC2RB fuses.

If PSCRV fuse equals 0 (programmed), the selected PSC outputs will be forced to low state. If PSCRV fuse equals 1 (unprogrammed), the selected PSC outputs will be forced to high state.

If PSCRRB fuse equals 1 (unprogrammed), PSCOUTR0 & PSCOUTR1 keep a standard port behavior. If PSC0RB fuse equals 0 (programmed), PSCOUTR0 & PSCOUTR1 are forced at reset to low level or high level according to PSCRV fuse bit. In this second case, PSCOUTR0 & PSCOUTR1 keep the forced state until PSOC0 register is written.

13.4 Signal Description

Figure 13-2. PSCR external block view.

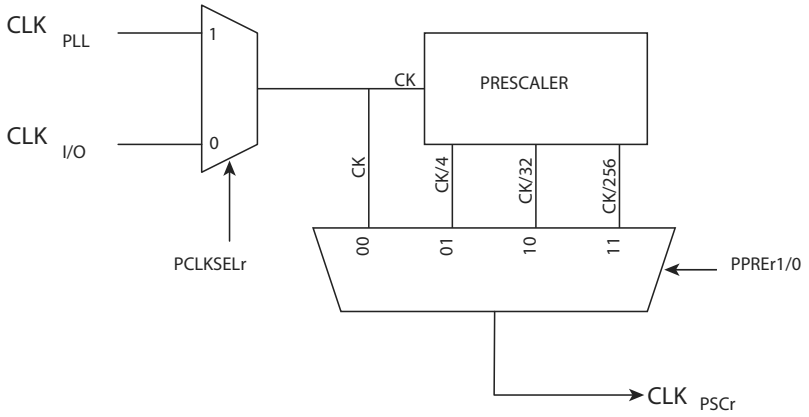


13.4.1 Input Description

Table 13-1. Internal inputs.

Name	Description	Type width
OCRrRB[11:0]	Compare value which reset signal on Part B (PSCOUTr1)	Register 12 bits
OCRrSB[11:0]	Compare value which set signal on Part B (PSCOUTr1)	Register 12 bits
OCRrRA[11:0]	Compare value which reset signal on Part A (PSCOUTr0)	Register 12 bits
OCRrSA[11:0]	Compare value which set signal on Part A (PSCOUTr0)	Register 12 bits
CLK I/O	Clock input from I/O clock	Signal
CLK PLL	Clock input from PLL	Signal

Figure 13-32. Clock selection.



PCLKSELr bit in PSCR Configuration register (PCNFr) is used to select the clock source.

PPREr1/0 bits in PSCR Control Register (PCTLr) are used to select the divide factor of the clock.

Table 13-7. Output clock versus selection and prescaler.

PCLKSELr	PPREr1	PPREr0	CLKPSCr output
0	0	0	CLK I/O
0	0	1	CLK I/O / 4
0	1	0	CLK I/O / 32
0	1	1	CLK I/O / 256
1	0	0	CLK PLL
1	0	1	CLK PLL / 4
1	1	0	CLK PLL / 32
1	1	1	CLK PLL / 256

13.22 Interrupts

This section describes the specifics of the interrupt handling as performed in AT90PWM81/161.

13.22.1 List of Interrupt Vector

The PSCR provides 3 interrupt vectors:

- **PSC0EC (End of Cycle**): When enabled and when a match with OCRrRB occurs
- **PSC0EEC (End of Enhanced Cycle**): When enabled and when a match with OCRrRB occurs at the 15th enhanced cycle
- **PSC0CAPT (Capture Event)**: When enabled and one of the two following events occurs : retrigger, capture of the PSCR counter or Synchro Error

See PSC0 Interrupt Mask Register page 177 and PSC0 Interrupt Flag Register page 178.

When this bit is set, I/O pin affected to PSCOUT01 is connected to the PSCR waveform generator B output and is set and clear according to the PSCR operation.

- **Bit 1 – Reserved**

- **Bit 0 – POEN0A: PSCR OUT Part A Output Enable**

When this bit is clear, I/O pin affected to PSCOUT00 acts as a standard port.

When this bit is set, I/O pin affected to PSCOUT00 is connected to the PSCR waveform generator A output and is set and clear according to the PSCR operation.

13.23.2 OCR0SAH and OCR0SAL - Output Compare SA Register

Bit	7	6	5	4	3	2	1	0	
	–	–	–	–	OCR0SA[11:8]				OCR0SAH
	OCR0SA[7:0]								OCR0SAL
Read/Write	W	W	W	W	W	W	W	W	
Initial Value	0	0	0	0	0	0	0	0	

13.23.3 OCR0RAH and OCR0RAL - Output Compare RA Register

Bit	7	6	5	4	3	2	1	0	
	–	–	–	–	OCR0RA[11:8]				OCR0RAH
	OCR0RA[7:0]								OCR0RAL
Read/Write	W	W	W	W	W	W	W	W	
Initial Value	0	0	0	0	0	0	0	0	

13.23.4 OCR0SBH and OCR0SBL - Output Compare SB Register

Bit	7	6	5	4	3	2	1	0	
	–	–	–	–	OCR0SB[11:8]				OCR0SBH
	OCR0SB[7:0]								OCR0SBL
Read/Write	W	W	W	W	W	W	W	W	
Initial Value	0	0	0	0	0	0	0	0	

13.23.5 OCR0RBH and OCR0RBL - Output Compare RB Register

Bit	7	6	5	4	3	2	1	0	
	OCR0RB[15:12]				OCR0RB[11:8]				OCR0RBH
	OCR0RB[7:0]								OCR0RBL
Read/Write	W	W	W	W	W	W	W	W	
Initial Value	0	0	0	0	0	0	0	0	

The Output Compare Registers RA, RB, SA and SB contain a 12-bit value that is continuously compared with the PSCR counter value. A match can be used to generate an Output Compare interrupt, or to generate a waveform output on the associated pin.

The Output Compare Registers RB contains also a 4-bit value that is used for the flank width modulation.

The Output Compare Registers are 12-bit in size. To ensure that both the high and low bytes are written simultaneously when the CPU writes to these registers, the access is performed using an 8-bit temporary high byte register (TEMP). This temporary register is shared by all the other 16-bit registers.

17. Analog to Digital Converter - ADC

17.1 Features

- **10-bit resolution**
- **0.5LSB integral non-linearity**
- **±2LSB absolute accuracy**
- **8µs - 250µs conversion time**
- **Up to 120kSPS at maximum resolution**
- **11 multiplexed single ended input channels**
- **One differential input channels with accurate (5%) programmable gain 5, 10, 20, and 40**
- **Optional left adjustment for ADC result readout**
- **0 - V_{CC} ADC input voltage range**
- **Selectable 2.56V ADC reference voltage**
- **Free running or single conversion mode**
- **ADC start conversion by auto triggering on interrupt sources**
- **Interrupt on ADC conversion complete**
- **Sleep mode noise canceler**
- **Temperature sensor**

The AT90PWM81/161 features a 10-bit successive approximation ADC. The ADC is connected to an 15-channel Analog Multiplexer which allows eleven single-ended input. The single-ended voltage inputs refer to 0V (GND).

The device also supports 2 differential voltage input combinations which are equipped with a programmable gain stage, providing amplification steps of 14dB (5×), 20dB (10×), 26dB (20×), or 32dB (40×) on the differential input voltage before the A/D conversion. On the amplified channels, 8-bit resolution can be expected.

The ADC contains a Sample and Hold circuit which ensures that the input voltage to the ADC is held at a constant level during conversion. A block diagram of the ADC is shown in Figure 17-1 on page 204.

The ADC has a separate analog supply voltage pin, AV_{CC}. AV_{CC} must not differ more than ±0.3V from V_{CC}. See the paragraph “ADC Noise Canceler” on page 210 on how to connect this pin.

Internal reference voltages of nominally 2.56V or AV_{CC} are provided On-chip. The voltage reference may be externally decoupled at the AREF pin by a capacitor for better noise performance.

Figure 17-1. Analog to digital converter block schematic.

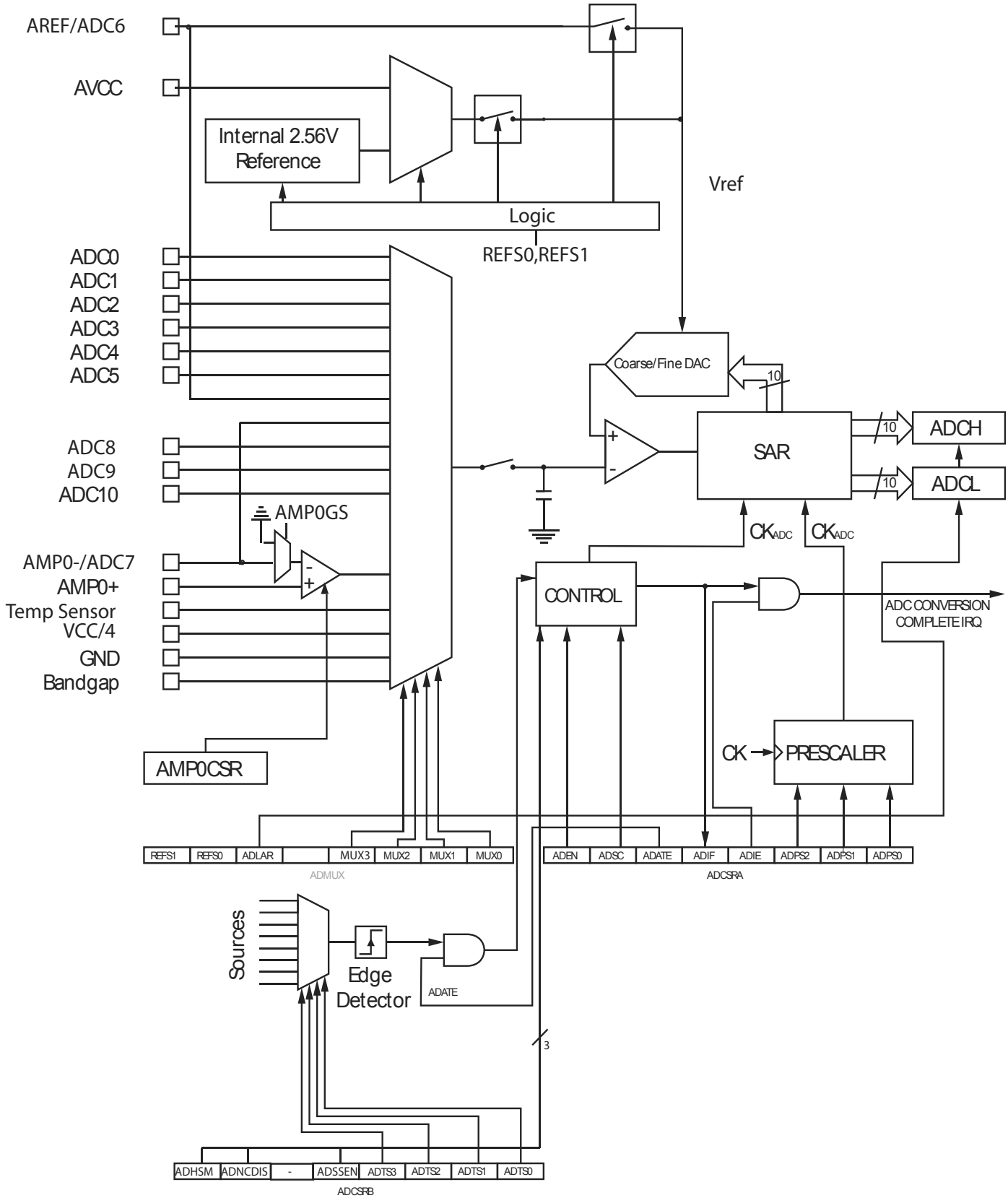
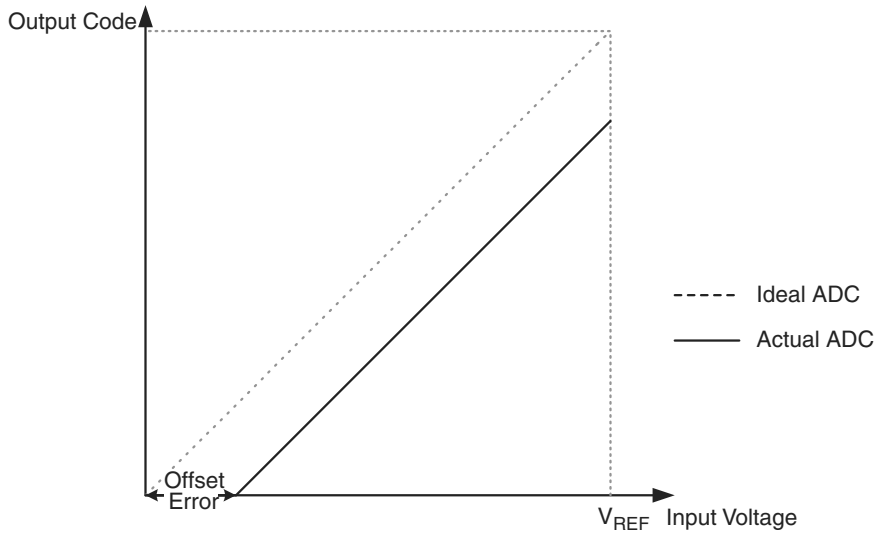
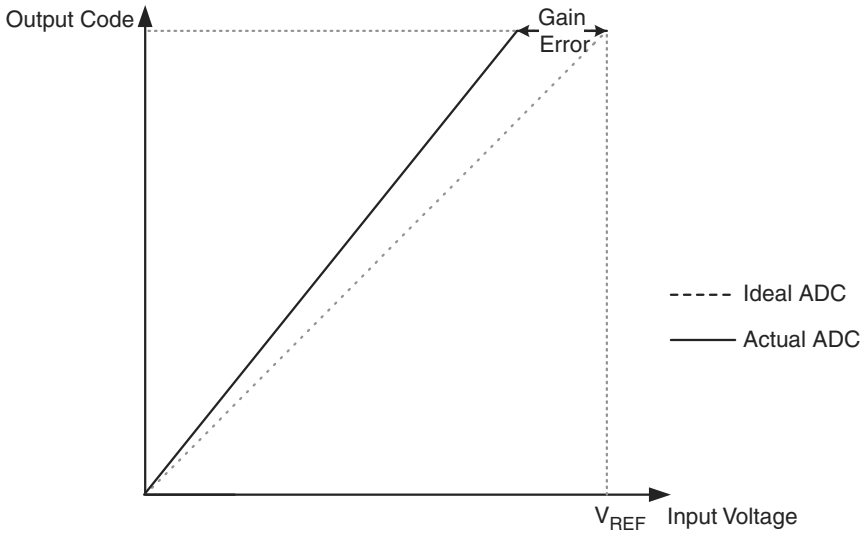


Figure 17-10. Offset error.



- Gain Error: After adjusting for offset, the Gain Error is found as the deviation of the last transition (0x3FE to 0x3FF) compared to the ideal transition (at 1.5LSB below maximum). Ideal value: 0LSB

Figure 17-11. Gain error.



- Integral Non-linearity (INL): After adjusting for offset and gain error, the INL is the maximum deviation of an actual transition compared to an ideal transition for any code. Ideal value: 0LSB

Figure 17-15. Amplifier synchronization timing diagram with change on analog input signal.

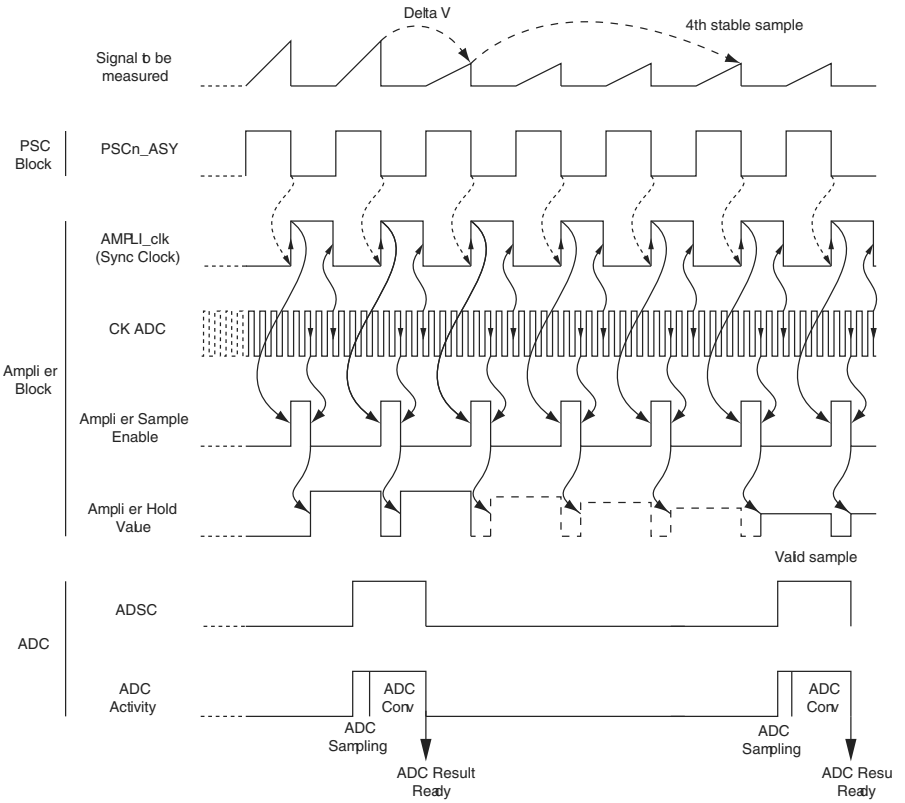
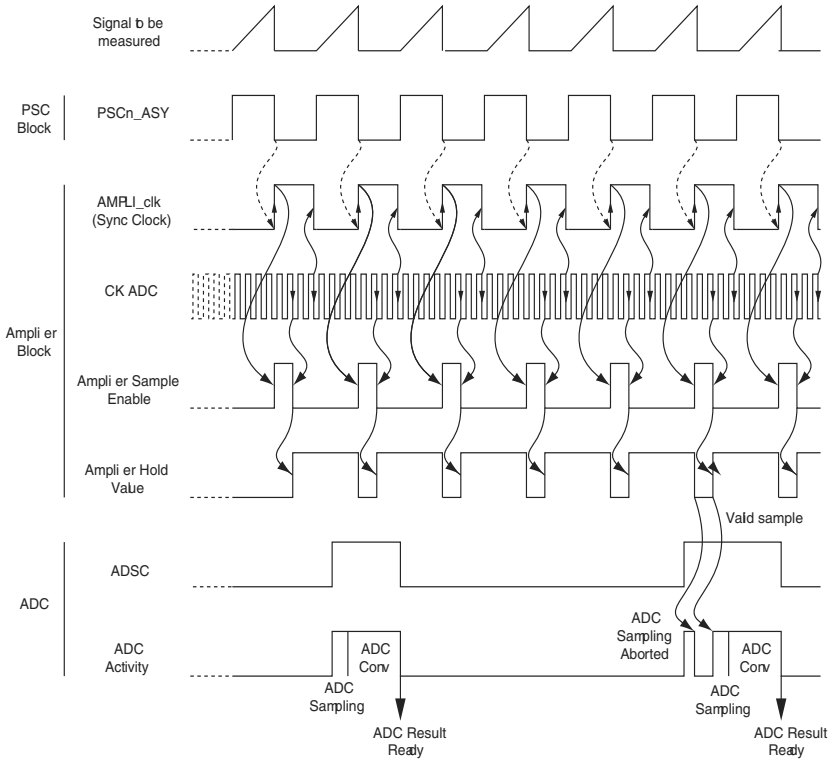
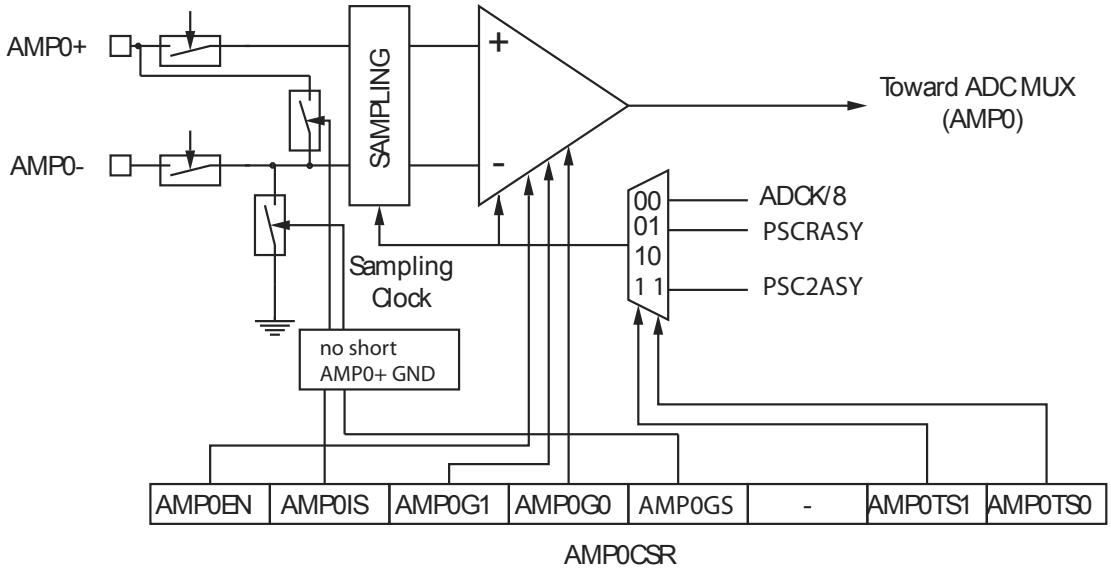


Figure 17-16. Amplifier synchronization timing diagram: behavior when ADSC is set when the amplifier output is changing.



The block diagram of the two amplifiers is shown on Figure 17-17.

Figure 17-17. Amplifiers block diagram.



If APMP0GS bit is set, the AMP0- input is open and PD5/AMP0- pin is free for another use. At the same time the negative input of the Amplifier is internally grounded.

17.10 Amplifier Control Registers

The configuration of the amplifier is controlled via the register AMP0CSR. Then the start of conversion is done via the ADC control and status registers.

The conversion result is stored on ADCH and ADCL register which contain respectively the most significant bits and the least significant bits.

17.10.1 AMP0CSR - Amplifier 0 Control and Status register

Bit	7	6	5	4	3	2	1	0	
	AMP0EN	**AMP0IS**	**AMP0G1**	**AMP0G0**	**AMP0GS**	**-**	**AMP0TS1**	**AMP0TS0**	**AMP0CSR**
Read/Write	R/W	R/W	R/W	R/W	-	-	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – AMP0EN: Amplifier 0 Enable Bit**

Set this bit to enable the Amplifier 0.
Clear this bit to disable the Amplifier 0.
Clearing this bit while a conversion is running will take effect at the end of the conversion.

- **Bit 6– AMP0IS: Amplifier 0 Input Shunt**

Set this bit to short-circuit the Amplifier 0 input. If AMP0GS is set, the ground switch is released during shunt of inputs.
Clear this bit to normally use the Amplifier 0.

Table 21-8. Pin name mapping. (Continued)

Signal name in programming mode	Pin name	I/O	Function
XA1/BS2	PD6	I	XTAL Action Bit 1 Byte Select 2 (“0” selects Low byte, “1” selects 2’nd High byte)
PAGEL/BS1	PE2	I	Program memory and EEPROM Data Page Load Byte Select 1 (“0” selects Low byte, “1” selects High byte)
DATA	PB[7:0]	I/O	Bi-directional Data bus (Output when $\overline{OE}$ is low)

Table 21-9. Pin Values Used to Enter Programming Mode.

Pin	Symbol	Value
XA1/BS2	Prog_enable[3]	0
XA0	Prog_enable[2]	0
$\overline{OE}$	Prog_enable[1]	0
$\overline{WR}$	Prog_enable[0]	0

Table 21-10. XA1 and XA0 coding.

XA1	XA0	Action when XTAL1 is pulsed
0	0	Load flash or EEPROM address (high or low address byte determined by BS1)
0	1	Load data (high or low data byte for flash determined by BS1)
1	0	Load command
1	1	No action, idle

Table 21-11. Command byte bit coding.

Command byte	Command executed
1000 0000	Chip Erase
0100 0000	Write Fuse bits
0010 0000	Write Lock bits
0001 0000	Write Flash
0001 0001	Write EEPROM
0000 1000	Read Signature Bytes and Calibration byte
0000 0100	Read Fuse and Lock bits
0000 0010	Read Flash
0000 0011	Read EEPROM

T_A = -40°C to +105°C, V_{CC} = 2.7V to 5.5V (unless otherwise noted). (Continued)

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Units
I_{CC}	Power supply current	Active 8MHz, V_{CC} = 3V, RC osc., PRR = 0xFF		3.5	5	mA
		Active 16MHz, V_{CC} = 5V, Ext Clock, PRR = 0xFF		10.5	15	
		Idle 8MHz, V_{CC} = 3V, RC Osc		1.5	2	
		Idle 16MHz, V_{CC} = 5V, Ext Clock		4.5	7	
	Power-down mode (5)	WDT enabled,V_{CC} = 3V 25°C		7		µA
		WDT enabled, V_{CC} = 3V 105°C			30	
		WDT enabled, V_{CC} = 5V 25°C		10		µA
		WDT enabled, V_{CC} = 5V 105°C			50	
		WDT disabled, V_{CC} = 3V 25°C		0.5		µA
		WDT disabled, V_{CC} = 3V 105°C			25	
		WDT disabled, V_{CC} = 5V 25°C		1		
		WDT disabled, V_{CC} = 5V 105°C			40	µA
V_{REF}	Internal voltage reference (7)	@25°C	2.46	2.56	2.66	V
	Analog comparator input common mode range		0.1		V_{CC} - 0.1	
V_{ACIO}	Analog comparator input offset voltage	Input offset voltage $0.1<V_{IN}<V_{CC}$ - 0.1V		±1.5	±10	mV
		With ±10mV hysteresis $0.1<V_{IN}<V_{CC}$ - 0.1V		±10	±20	
		With ± 25mV hysteresis $0.1<V_{IN}<V_{CC}$ - 0.1V		±25	±60	
I_{ACLK}	Analog comparator input leakage current	V_{CC} = 5V V_{IN} = V_{CC}/2	-50		50	nA
t_{ACID}	Analog comparator propagation delay	V_{CC} = 2.7V V_{CC} = 5.0V		50 (6)		ns

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Units
I_{CC}	Power supply current	Active 8MHz, V_{CC} = 3V, RC osc, PRR = 0xFF		3.5	5	mA
		Active 16MHz, V_{CC} = 5V, Ext Clock, PRR = 0xFF		10.5	15	
		Idle 8MHz, V_{CC} = 3V, RC Osc		1.5	2	
		Idle 16MHz, V_{CC} = 5V, Ext Clock		4.5	7	
	Power-down mode (5)	WDT enabled, V_{CC} = 3V 25°C		7		µA
		WDT enabled, V_{CC} = 3V 125°C			70	
		WDT enabled, V_{CC} = 5V 25°C		10		
		WDT enabled, V_{CC} = 5V 125°C			110	
		WDT disabled, V_{CC} = 3V 25°C		0.5		
		WDT disabled, V_{CC} = 3V 125°C			35	
		WDT disabled, V_{CC} = 5V 25°C		1		
		WDT disabled, V_{CC} = 5V 125°C			55	
V_{REF}	Internal voltage reference (7)	@25°C	2.46	2.56	2.66	V
	Analog comparator input common mode range		0.1		V_{CC} - 0.1	
V_{ACIO}	Analog comparator input offset voltage	Input offset voltage $0.1<V_{IN}<V_{CC}$ - 0.1V		±1.5	±10	mV
		With ±10mV Hysteresis $0.1<V_{IN}<V_{CC}$ - 0.1V		±10	±20	
		With ±25mV Hysteresis $0.1<V_{IN}<V_{CC}$ - 0.1V		±25	±60	
I_{ACLK}	Analog comparator input leakage current	V_{CC} = 5V V_{IN} = V_{CC}/2	-50		50	nA
t_{ACID}	Analog comparator propagation delay	V_{CC} = 2.7V V_{CC} = 5.0V		50 (6)		ns

Note: 1. “Maximum” means the highest value where the pin is guaranteed to be read as low.

2. “Minimum” means the lowest value where the pin is guaranteed to be read as high.

3. Although each I/O port can sink more than the test conditions (20mA at V_{CC} = 5V, 10mA at V_{CC} = 3V) under steady state conditions (non-transient), the following must be observed:
SO20 and TQFN Package:
1] The sum of all I_{OL}, for all ports, should not exceed 400mA.
2] The sum of all I_{OL}, for ports B6 - B7, D0 - D3, E0 should not exceed 100mA.
3] The sum of all I_{OL}, for ports B0 - B1, D4, E1 - E2 should not exceed 100mA.

5. Flash and EEPROM programming failure if CPU clock is switched

If Clock switching is used in the Application, the memory programming is only possible when the internal RC oscillator is selected as System clock.

If the Application requires a memory programming on a clock source different from the internal RC oscillator, do not switch to this clock source.

Work around:

- Use internal RC oscillator when programming Flash and EEPROM,

or

- Do not use clock switching.

6. ADC AMPlifier measurement is unstable

When switching from a single-ended ADC channel to an Amplified channel, noise can appear on ADC conversion.

Work around:

After switching from a single ended to an amplified channel, discard the first ADC conversion.

7. ADC measurement reports abnormal values with PSC2-synchronized conversions

When using ADC in synchronized mode, an unexpected extra Single ended conversion can spuriously re-start.This can occur when the End of conversion and the Trigger event occur at the same time.

Work around:

No workaround

8. Over-consumption in power down sleep mode.

In Power-down mode, an extra power consumption up to 500µA may occur.

Work around:

No workaround

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- **Clock Switch disable**
- **Crystal oscillator control with Clock Switch**
- **BOD disable fuse**
- **PSC output at Reset**
- **Flash and EEPROM programming failure if CPU clock is switched**
- **ADC AMPlifier measurement is unstable**
- **ADC measurement reports abnormal values with PSC2-synchronized conversions**
- **Over-consumption in power down sleep mode**