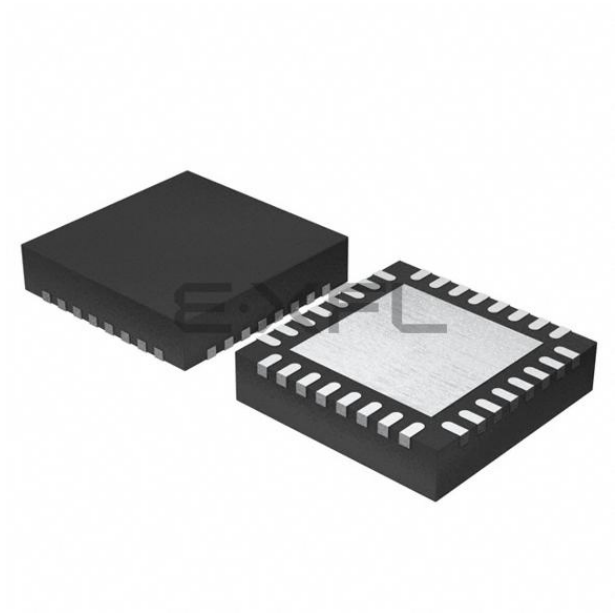

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	16MHz
Connectivity	SPI
Peripherals	Brown-out Detect/Reset, PWM, WDT
Number of I/O	20
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 11x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at90pwm81-16mf

  - **Power-on reset and programmable brown-out detection**
  - **Flag array in bit-programmable I/O space (three bytes)**
  - **In-system programmable via SPI port**
  - **Internal low power calibrated RC oscillator (8MHz or 1MHz, low jitter)**
  - **On chip PLL for fast PWM (32MHz, 48MHz, 64MHz) and CPU (12MHz, 16MHz); PLL source RC & XTAL**
  - **Dynamic clock switch**
  - **Temperature sensor**
- **Operating voltage: 2.7V - 5.5V**
- **Operating temperature:**
  - **-40°C to +105°C or -40°C to +125°C**
- **Operating speed**
  - **5V: 16MHz core, 64MHz PLL**
  - **3.3V: 12MHz core, 48MHz PLL**

1. Products Configuration

The different product configurations are described per Table 1-1.

Table 1-1. PWM81/PWM161 configurations.

Package	**SO20**	**QFN32**
Pins	20	32
Flash size	8/16K (1)	8/16K (1)
EEPROM size	512	512
RAM size	256/1024 (2)	256/1024 (2)
PSC 12 bits with extended features	1	1
PSC 12 bits	1	1
Timer 8 bits	-	-
Timer 16 bits	1	1
ADC inputs	8	11
Amplifiers for ADC	1	1
Temperature sensor	1	1
Analog Comparators	3	3
DAC	1	1
DAC amplifiers	-	-
UART/DALI	-	-
SPI	1	1

Notes: 1. Flash size is 8Kbytes for AT90PWM81 and 16Kbytes for AT90PWM161.
2. RAM size is 256 bytes for AT90PWM81 and 1024 bytes for AT90PWM161.

4. Memories

This section describes the different memories in the Atmel AT90PWM81/161. The AVR architecture has two main memory spaces, the Data Memory and the Program Memory space. In addition, the AT90PWM81/161 features an EEPROM Memory for data storage. All three memory spaces are linear and regular.

4.1 In-System Reprogrammable Flash Program Memory

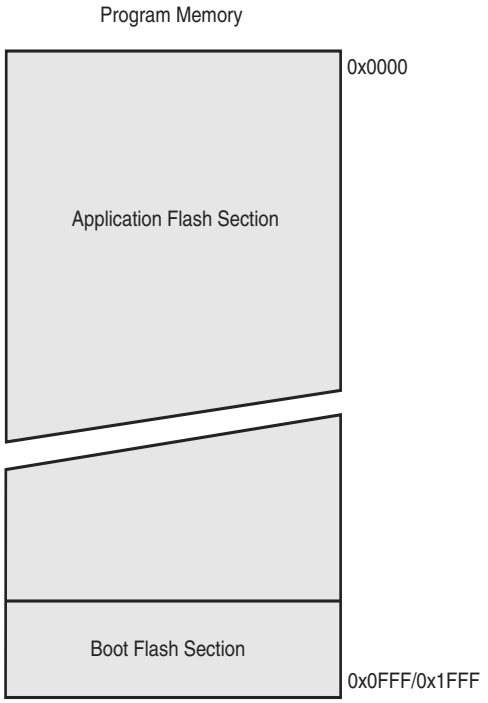
The AT90PWM81/161 contains 8/16Kbytes On-chip In-System Reprogrammable Flash memory for program storage. Since all AVR instructions are 16 or 32 bits wide, the Flash is organized as 4K × 16bits for the AT90PWM81, and 8K × 16bits for the AT90PWM161. For software security, the Flash Program memory space is divided into two sections, Boot Program section and Application Program section.

The Flash memory has an endurance of at least 10,000 write/erase cycles. The AT90PWM81 Program Counter (PC) is 12 bits wide, thus addressing the 8Kbytes program memory locations. The AT90PWM161 Program Counter (PC) is 13 bits wide, thus addressing the 16Kbytes program memory locations. The operation of Boot Program section and associated Boot Lock bits for software protection are described in detail in “Boot Loader Support – Read-While-Write Self-Programming” on page 233. “Memory Programming” on page 248 contains a detailed description on Flash programming in SPI or Parallel programming mode.

Constant tables can be allocated within the entire program memory address space (see the description of LPM – Load Program Memory in “Instruction Set Summary” on page 301).

Timing diagrams for instruction fetch and execution are presented in “Instruction Execution Timing” on page 12.

Figure 4-1. Program memory map.



If PORTxn is written logic one when the pin is configured as an output pin, the port pin is driven high (one). If PORTxn is written logic zero when the pin is configured as an output pin, the port pin is driven low (zero).

9.2.2 Toggling the Pin

Writing a logic one to PINxn toggles the value of PORTxn, independent on the value of DDRxn. Note that the SBI instruction can be used to toggle one single bit in a port.

9.2.3 Switching Between Input and Output

When switching between tri-state ({DDxn, PORTxn} = 0b00) and output high ({DDxn, PORTxn} = 0b11), an intermediate state with either pull-up enabled {DDxn, PORTxn} = 0b01) or output low ({DDxn, PORTxn} = 0b10) must occur. Normally, the pull-up enabled state is fully acceptable, as a high-impedant environment will not notice the difference between a strong high driver and a pull-up. If this is not the case, the PUD bit in the MCUCR Register can be set to disable all pull-ups in all ports.

Switching between input with pull-up and output low generates the same problem. The user must use either the tri-state ({DDxn, PORTxn} = 0b00) or the output high state ({DDxn, PORTxn} = 0b11) as an intermediate step.

Table 9-1 summarizes the control signals for the pin value.

Table 9-1. Port pin configurations.

DDxn	PORTxn	PUD (in MCUCR)	I/O	Pull-up	Comment
0	0	X	Input	No	Default configuration after reset. Tri-state (Hi-Z)
0	1	0	Input	Yes	Pxn will source current if ext. pulled low
0	1	1	Input	No	Tri-state (Hi-Z)
1	0	X	Output	No	Output low (Sink)
1	1	X	Output	No	Output high (Source)

9.2.4 Reading the Pin Value

Independent of the setting of Data Direction bit DDxn, the port pin can be read through the PINxn Register bit. As shown in Figure 9-2 on page 69, the PINxn Register bit and the preceding latch constitute a synchronizer. This is needed to avoid metastability if the physical pin changes value near the edge of the internal clock, but it also introduces a delay. Figure 9-3 on page 71 shows a timing diagram of the synchronization when reading an externally applied pin value. The maximum and minimum propagation delays are denoted $t_{pd,max}$ and $t_{pd,min}$ respectively.

Figure 11-6. Timer/counter timing diagram, no prescaling.

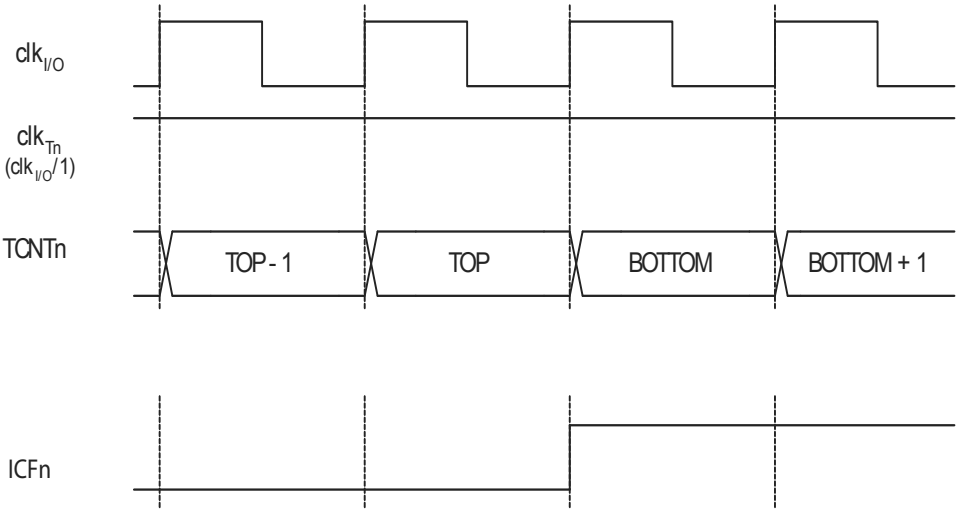
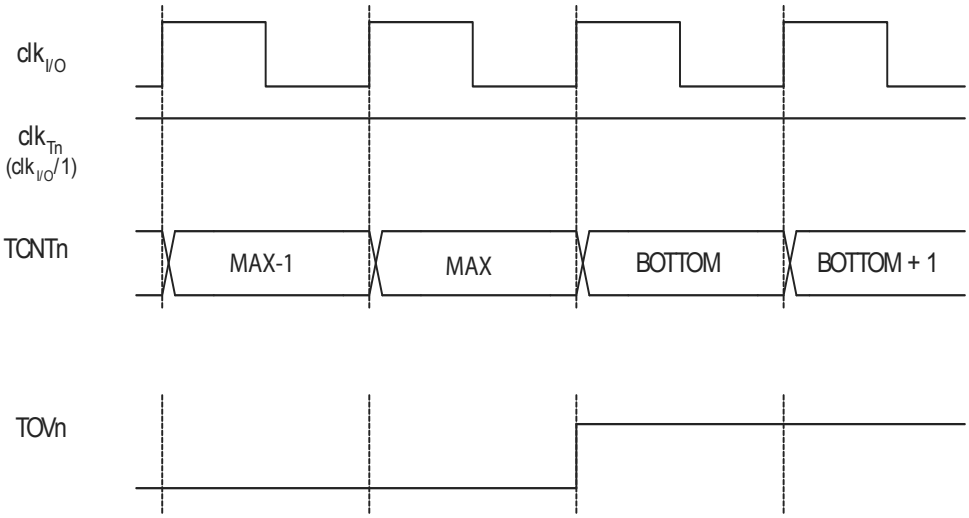


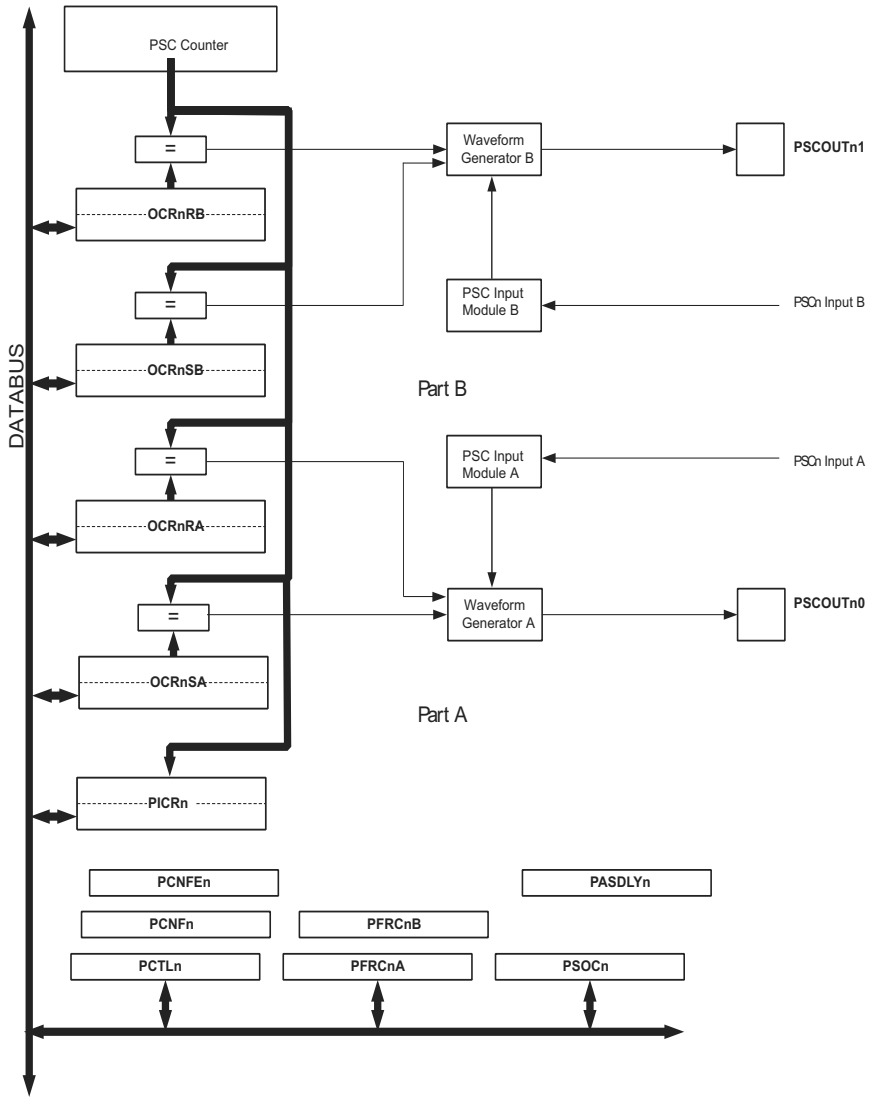
Figure 11-7 shows the count sequence close to MAX in various modes.

Figure 11-7. Timer/counter timing diagram, no prescaling.



12.3 PSC Description

Figure 12-1. Power Stage Controller 0 or 1 block diagram.



Note: n = 0, 1.

The principle of the PSC is based on the use of a counter (PSC counter). This counter is able to count up and count down from and to values stored in registers according to the selected running mode.

The PSC is seen as two symmetrical entities. One part named part A which generates the output PSCOUTn0 and the second one named part B which generates the PSCOUTn1 output.

Each part A or B has its own PSC Input Module to manage selected input.

- **Bit 5 – PLOCKn: PSC n Lock**

When this bit is set, the Output Compare Registers RA, RB, SA, SB, the Output Matrix POM2 and the PSC Output Configuration PSOCn can be written without disturbing the PSC cycles. The update of the PSC internal registers will be done if the LOCK bit is released to zero.

- **Bit 4:3 – PMODEn1: 0: PSC n Mode**

Select the mode of PSC.

Table 12-13. PSC n mode selection.

PMODEn1	PMODEn0	Description
0	0	One Ramp mode
0	1	Two Ramp mode
1	0	Four Ramp mode
1	1	Center Aligned mode

- **Bit 2 – POPn: PSC n Output Polarity**

If this bit is cleared, the PSC outputs are active Low.

If this bit is set, the PSC outputs are active High.

- **Bit 1 – PCLKSELn: PSC n Input Clock Select**

This bit is used to select between CLKPF or CLKPS clocks.

Set this bit to select the fast clock input (CLKPF).

Clear this bit to select the slow clock input (CLKPS).

- **Bit 0 – POME2: PSC 2 Output Matrix Enable (PSC2 only)**

Set this bit to enable the Output Matrix feature on PSC2 outputs. See “PSC2 Outputs” on page 129.

When Output Matrix is used, the PSC n Output Polarity POPn has no action on the outputs.

12.25.7 PCNFE2 - PSC 2 Extended Configuration Register

Bit	7	6	5	4	3	2	1	0	
	PASDLKn2	PASDLKn1	PASDLKn0	PBFMn1	PELEVnA1	PELEVnB1	PISELnA1	PISELnB1	PCNFE2
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The PSC n Extended Configuration Register is used to configure the running mode of the PSC.

- **Bit 7, 6, 5– PASDLKn(2:0): Analog Synchronization Output Delay or Input Blanking select**

Defines the modes for Analog signal synchronization delay or Input Blanking.

Table 12-21. Level sensitivity and Fault Mode operation. (Continued)

PRFMnx3:0	Description
0100b	“PSC Input Mode 4: Deactivate outputs without changing timing”, page 124
0101b	“PSC Input Mode 5: Stop signal and Insert Dead-Time”, page 124
0110b	“PSC Input Mode 6: Stop signal, Jump to Opposite Dead-Time and Wait”, page 125
0111b	“PSC Input Mode 7: Halt PSC and Wait for Software Action”, page 125
1000b	“PSC Input Mode 8: Edge Retrigger PSC”, page 126
1001b	“PSC Input Mode 9: Fixed Frequency Edge Retrigger PSC”, page 127
1010b	Reserved (do not use)
1011b	
1100b	
1101b	
1110b	“PSC Input Mode 14: Fixed Frequency Edge Retrigger PSC and Deactivate Output”, page 128
1111b	Reserved (do not use)

12.25.12 PICR2H and PICR2L - PSC 2 Input Capture Register

Bit	7	6	5	4	3	2	1	0	
	PCST2	–	–	–	PICR2[11:8]				PICR2H
	PICR2[7:0]								PICR2L
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – PCSTn: PSC Capture Software Trig bit**

Set this bit to trigger off a capture of the PSC counter. When reading, if this bit is set it means that the capture operation was triggered by PCSTn setting otherwise it means that the capture operation was triggered by a PSC input.

The Input Capture is updated with the PSC counter value each time an event occurs on the enabled PSC input pin (or optionally on the Analog Comparator output) if the capture function is enabled (bit PCAEnx in PFRCnx register is set).

The Input Capture Register is 12-bit in size. To ensure that both the high and low bytes are read simultaneously when the CPU accesses these registers, the access is performed using an 8-bit temporary high byte register (TEMP). This temporary register is shared by all the other 16-bit or 12-bit registers.

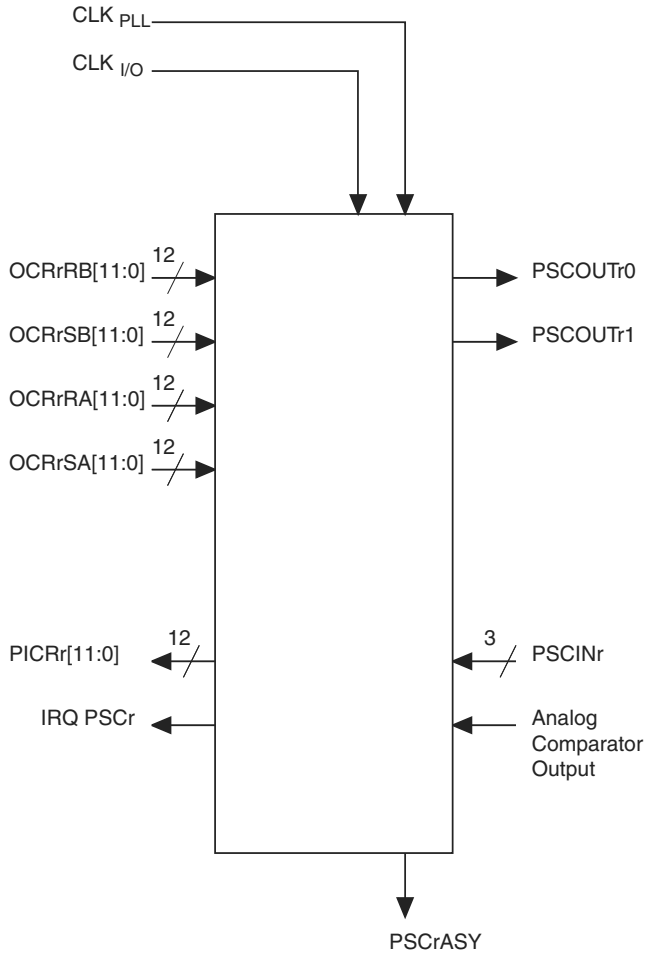
12.26 PSC2 Specific Register

12.26.1 POM2 - PSC 2 Output Matrix

Bit	7	6	5	4	3	2	1	0	
	POMV2B3	POMV2B2	POMV2B1	POMV2B0	POMV2A3	POMV2A2	POMV2A1	POMV2A0	POM2
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

13.4 Signal Description

Figure 13-2. PSCR external block view.



13.4.1 Input Description

Table 13-1. Internal inputs.

Name	Description	Type width
OCRrRB[11:0]	Compare value which reset signal on Part B (PSCOUTr1)	Register 12 bits
OCRrSB[11:0]	Compare value which set signal on Part B (PSCOUTr1)	Register 12 bits
OCRrRA[11:0]	Compare value which reset signal on Part A (PSCOUTr0)	Register 12 bits
OCRrSA[11:0]	Compare value which set signal on Part A (PSCOUTr0)	Register 12 bits
CLK I/O	Clock input from I/O clock	Signal
CLK PLL	Clock input from PLL	Signal

When this bit is set, I/O pin affected to PSCOUT01 is connected to the PSCR waveform generator B output and is set and clear according to the PSCR operation.

- **Bit 1 – Reserved**

- **Bit 0 – POEN0A: PSCR OUT Part A Output Enable**

When this bit is clear, I/O pin affected to PSCOUT00 acts as a standard port.

When this bit is set, I/O pin affected to PSCOUT00 is connected to the PSCR waveform generator A output and is set and clear according to the PSCR operation.

13.23.2 OCR0SAH and OCR0SAL - Output Compare SA Register

Bit	7	6	5	4	3	2	1	0	
	–	–	–	–	OCR0SA[11:8]				OCR0SAH
	OCR0SA[7:0]								OCR0SAL
Read/Write	W	W	W	W	W	W	W	W	
Initial Value	0	0	0	0	0	0	0	0	

13.23.3 OCR0RAH and OCR0RAL - Output Compare RA Register

Bit	7	6	5	4	3	2	1	0	
	–	–	–	–	OCR0RA[11:8]				OCR0RAH
	OCR0RA[7:0]								OCR0RAL
Read/Write	W	W	W	W	W	W	W	W	
Initial Value	0	0	0	0	0	0	0	0	

13.23.4 OCR0SBH and OCR0SBL - Output Compare SB Register

Bit	7	6	5	4	3	2	1	0	
	–	–	–	–	OCR0SB[11:8]				OCR0SBH
	OCR0SB[7:0]								OCR0SBL
Read/Write	W	W	W	W	W	W	W	W	
Initial Value	0	0	0	0	0	0	0	0	

13.23.5 OCR0RBH and OCR0RBL - Output Compare RB Register

Bit	7	6	5	4	3	2	1	0	
	OCR0RB[15:12]				OCR0RB[11:8]				OCR0RBH
	OCR0RB[7:0]								OCR0RBL
Read/Write	W	W	W	W	W	W	W	W	
Initial Value	0	0	0	0	0	0	0	0	

The Output Compare Registers RA, RB, SA and SB contain a 12-bit value that is continuously compared with the PSCR counter value. A match can be used to generate an Output Compare interrupt, or to generate a waveform output on the associated pin.

The Output Compare Registers RB contains also a 4-bit value that is used for the flank width modulation.

The Output Compare Registers are 12-bit in size. To ensure that both the high and low bytes are written simultaneously when the CPU writes to these registers, the access is performed using an 8-bit temporary high byte register (TEMP). This temporary register is shared by all the other 16-bit registers.

- **Bit 1– PEOEPE0: PSCR End Of Enhanced Cycle Interrupt Enable**

When this bit is set, an interrupt is generated when PSC reduced reaches the end of the 15th PSC cycle. This allows to update the PSCR values in the interrupt routine and to start a new enhanced cycle with the new values at the next PSCR cycle end.

- **Bit 0 – PEOPE0: PSCR End Of Cycle Interrupt Enable**

When this bit is set, an interrupt is generated when PSCR reaches the end of the whole cycle.

13.23.12 PIFR0 - PSCR Interrupt Flag Register

Bit	7	6	5	4	3	2	1	0	
	POAC0B	POAC0A	-	PEV0B	PEV0A	PRN01	PRN00	PEOP0	PIFR0
Read/Write	R	R	R	R/W	R/W	R	R	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – POAC0B: PSCR Output B Activity**

This bit is set by hardware each time the output PSCOUT01 changes from 0 to 1 or from 1 to 0.

Must be cleared by software by writing a one to its location.

This feature is useful to detect that a PSCR output doesn't change due to a frozen external input signal.

- **Bit 6 – POAC0A: PSCR Output A Activity**

This bit is set by hardware each time the output PSCOUT00 changes from 0 to 1 or from 1 to 0.

Must be cleared by software by writing a one to its location.

This feature is useful to detect that a PSCR output doesn't change due to a freezen external input signal.

- **Bit 5 – Reserved**

- **Bit 4 – PEV0B: PSCR External Event B Interrupt**

This bit is set by hardware when an external event which can generates a capture or a retrigger from Retrigger/Fault block B occurs.

Must be cleared by software by writing a one to its location.

This bit can be read even if the corresponding interrupt is not enabled (PEVE0B bit = 0).

- **Bit 3 – PEV0A: PSCR External Event A Interrupt**

This bit is set by hardware when an external event which can generates a capture or a retrigger from Retrigger/Fault block A occurs.

Must be cleared by software by writing a one to its location.

This bit can be read even if the corresponding interrupt is not enabled (PEVE0A bit = 0).

- **Bit 2:1 – PRN01:0 : PSCR Ramp Number**

Memorization of the ramp number when the last PEV0A or PEV0B occurred.

16.4.3 AC3CON - Analog Comparator 3 Control Register

Bit	7	6	5	4	3	2	1	0	
	AC3EN	AC3IE	AC3IS1	AC3IS0	AC3OEA	AC3M2	AC3M1	AC3M0	AC3CON
Read/Write	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7– AC3EN: Analog Comparator 3 Enable Bit**

Set this bit to enable the analog comparator 3.
Clear this bit to disable the analog comparator 3.

- **Bit 6– AC3IE: Analog Comparator 3 Interrupt Enable bit**

Set this bit to enable the analog comparator 3 interrupt.
Clear this bit to disable the analog comparator 3 interrupt.

- **Bit 5, 4– AC3IS1, AC3IS0: Analog Comparator 3 Interrupt Select bit**

These 2 bits determine the sensitivity of the interrupt trigger.
The different setting are shown in Table 16-5.

Table 16-5. Interrupt sensitivity selection.

AC3IS1	AC3IS0	Description
0	0	Comparator interrupt on output toggle
0	1	Reserved
1	0	Comparator interrupt on output falling edge
1	1	Comparator interrupt on output rising edge

- **Bit 3– AC3OEA: Analog Comparator 3 Alternate Output Enable**

Set this bit to enable the analog comparator 3 alternate output pin.
Clear this bit to disable the analog comparator 3 alternate output pin.

- **Bit 2, 1, 0– AC3M2, AC3M1, AC3M0: Analog Comparator 3 Multiplexer register**

These 3 bits determine the input of the negative input of the analog comparator.
The different setting are shown in Table 16-6.

Table 16-6. Analog Comparator 2 negative input selection.

AC3M2	AC3M1	AC3M0	Description
0	0	0	"V_{REF}"/6.40
0	0	1	"V_{REF}"/3.20
0	1	0	"V_{REF}"/2.13
0	1	1	"V_{REF}"/1.60
1	0	0	Band gap voltage
1	0	1	DAC result
1	1	0	Analog comparator negative input (ACMPM3 pin)
1	1	1	Analog comparator negative input (ACMPM pin)

Figure 17-5. ADC timing diagram, single conversion.

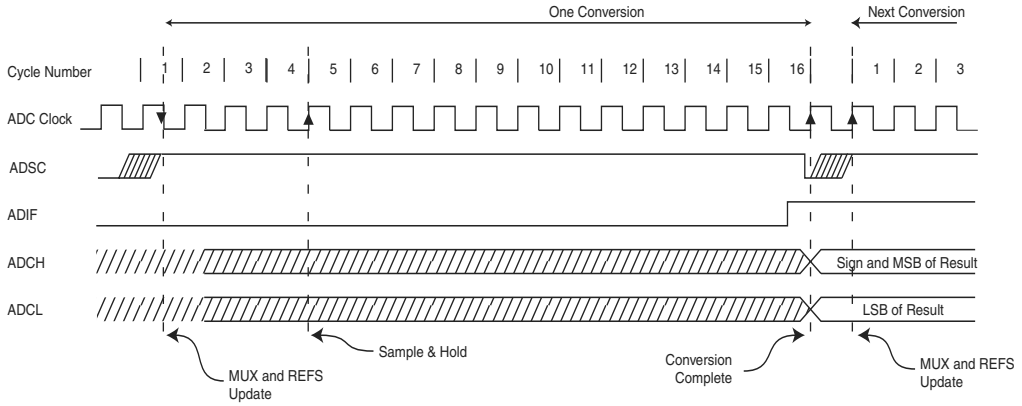


Figure 17-6. ADC timing diagram, auto triggered conversion.

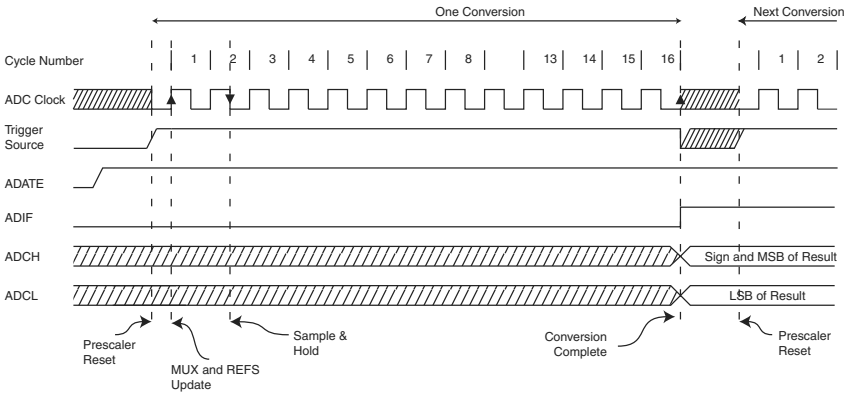
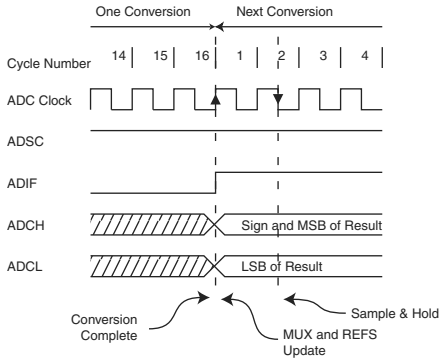


Figure 17-7. ADC timing diagram, free running conversion.



completed, the user software must clear the RWWSB by writing the RWWSRE. See “Simple Assembly Code Example for a Boot Loader” on page 245 for an example.

20.7.7 Setting the Boot Loader Lock Bits by SPM

To set the Boot Loader Lock bits, write the desired data to R0, write “X0001001” to SPMCSR and execute SPM within four clock cycles after writing SPMCSR. The only accessible Lock bits are the Boot Lock bits that may prevent the Application and Boot Loader section from any software update by the MCU.

Bit	7	6	5	4	3	2	1	0
R0	1	1	BLB12	BLB11	BLB02	BLB01	1	1

See Table 20-2 on page 237 and Table 20-3 on page 237 for how the different settings of the Boot Loader bits affect the Flash access.

If bits 5..2 in R0 are cleared (zero), the corresponding Boot Lock bit will be programmed if an SPM instruction is executed within four cycles after BLBSET and SPMEN are set in SPMCSR. The Z-pointer is don’t care during this operation, but for future compatibility it is recommended to load the Z-pointer with 0x0001 (same as used for reading the lO_{ck} bits). For future compatibility it is also recommended to set bits 7, 6, 1, and 0 in R0 to “1” when writing the Lock bits. When programming the Lock bits the entire Flash can be read during the operation.

20.7.8 EEPROM Write Prevents Writing to SPMCSR

Note that an EEPROM write operation will block all software programming to Flash. Reading the Fuses and Lock bits from software will also be prevented during the EEPROM write operation. It is recommended that the user checks the status bit (EEPE) in the EECR Register and verifies that the bit is cleared before writing to the SPMCSR Register.

20.7.9 Reading the Fuse and Lock Bits from Software

It is possible to read both the Fuse and Lock bits from software. To read the Lock bits, load the Z-pointer with 0x0001 and set the BLBSET and SPMEN bits in SPMCSR. When an LPM instruction is executed within three CPU cycles after the BLBSET and SPMEN bits are set in SPMCSR, the value of the Lock bits will be loaded in the destination register. The BLBSET and SPMEN bits will auto-clear upon completion of reading the Lock bits or if no LPM instruction is executed within three CPU cycles or no SPM instruction is executed within four CPU cycles. When BLBSET and SPMEN are cleared, LPM will work as described in the Instruction set Manual.

Bit	7	6	5	4	3	2	1	0
Rd	–	–	BLB12	BLB11	BLB02	BLB01	LB2	LB1

The algorithm for reading the Fuse Low byte is similar to the one described above for reading the Lock bits. To read the Fuse Low byte, load the Z-pointer with 0x0000 and set the BLBSET and SPMEN bits in SPMCSR. When an LPM instruction is executed within three cycles after the BLBSET and SPMEN bits are set in the SPMCSR, the value of the Fuse Low byte (FLB) will be loaded in the destination register as shown below. Refer to Table 21-4 on page 249 for a detailed description and mapping of the Fuse Low byte.

Bit	7	6	5	4	3	2	1	0
Rd	FLB7	FLB6	FLB5	FLB4	FLB3	FLB2	FLB1	FLB0

Similarly, when reading the Fuse High byte, load 0x0003 in the Z-pointer. When an LPM instruction is executed within three cycles after the BLBSET and SPMEN bits are set in the SPMCSR,

For AT90PWM161.

Table 20-8. Boot size configuration.

BOOTSZ1	BOOTSZ0	Boot size	Pages	Application flash section	Boot loader flash section	End application section	Boot reset address (start boot loader section)
1	1	256 words	4	0x000 - 0x1EFF	0x1F00 - 0x1FFF	0x1EFF	0x1F00
1	0	512 words	8	0x000 - 0x1DFF	0x1E00 - 0x1FFF	0x1DFF	0x1E00
0	1	1024 words	16	0x000 - 0x1BFF	0x1C00 - 0x1FFF	0x1BFF	0x1C00
0	0	2048 words	32	0x000 - 0x17FF	0x1800 - 0x1FFF	0x17FF	0x1800

The different BOOTSZ Fuse configurations are shown in Figure 20-2 on page 236.

Table 20-9. Read-while-write limit.

Section	Pages	Address
Read-while-write section (RWW)	96	0x000 - 0x17FF
No read-while-write section (NRWW)	32	0x1800 - 0x1FFF

For details about these two section, see “NRWW – No Read-While-Write Section” on page 234 and “RWW – Read-While-Write Section” on page 234.

Table 20-10. Explanation of different variables used in Figure 20-3 on page 240 and the mapping to the Z-pointer.

Variable	AT90PWM81	AT90PWM81 corresponding Z-value (1)	AT90PWM161	AT90PWM161 corresponding Z-value (1)	Description
PCMSB	11		12		Most significant bit in the Program Counter. (The Program Counter is 12 bits PC[11:0])
PAGEMSB	4		4		Most significant bit which is used to address the words within one page (32 words in a page requires 5 bits PC [4:0])
ZPCMSB		Z12		Z12	Bit in Z-register that is mapped to PCMSB. Because Z0 is not used, the ZPCMSB equals PCMSB + 1
ZPAGEMSB		Z5		Z5	Bit in Z-register that is mapped to PAGEMSB. Because Z0 is not used, the ZPAGEMSB equals PAGEMSB + 1
PCPAGE	PC[11:5]	Z12:Z6	PC[12:6]	Z12:Z6	Program counter page address: Page select, for page erase and page write
PCWORD	PC[4:0]	Z5:Z1	PC[5:0]	Z5:Z1	Program counter word address: Word select, for filling temporary buffer (must be zero during page write operation)

Note: 1. Z15:Z13: always ignored.
Z0: should be zero for all SPM commands, byte select for the LPM instruction.
See “Addressing the Flash During Self-Programming” on page 239 for details about the use of Z-pointer during Self-Programming.

T_A = -40°C to +125°C, V_{CC} = 2.7V to 5.5V (unless otherwise noted). (Continued)

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Units
V_{IL}	Input low voltage	Port B & D and XTAL1, XTAL2 pins as I/O	-0.5		$0.2V_{CC}$ (1)	V
V_{IH}	Input high voltage	Port B D and XTAL1, XTAL2 pins as I/O	$0.6V_{CC}$ (2)		V_{CC}+0.5	
V_{IL1}	Input low voltage	XTAL1 pin, External Clock selected	-0.5		$0.1V_{CC}$ (1)	
V_{IH1}	Input high voltage	XTAL1 pin, External Clock selected	$0.7V_{CC}$ (2)		V_{CC}+0.5	
V_{IL2}	Input low voltage	$\overline{\text{RESET}}$ pin	-0.5		$0.2V_{CC}$ (1)	
V_{IH2}	Input high voltage	$\overline{\text{RESET}}$ pin	$0.9V_{CC}$ (2)		V_{CC}+0.5	
V_{IL3}	Input low voltage	$\overline{\text{RESET}}$ pin as I/O	-0.5		$0.2V_{CC}$ (1)	
V_{IH3}	Input high voltage	$\overline{\text{RESET}}$ pin as I/O	$0.8V_{CC}$ (2)		V_{CC}+0.5	
V_{OL}	Output low voltage (3) (Port B & D and XTAL1, XTAL2 pins as I/O)	I_{OL} = 10mA, V_{CC} = 5V I_{OL} = 5mA, V_{CC} = 3V			0.6 0.5	
V_{OH}	Output high voltage (4) (Port B & D and XTAL1, XTAL2 pins as I/O)	I_{OH} = -10mA, V_{CC} = 5V I_{OH} = -5mA, V_{CC} = 3V	4.3 2.5			
V_{OL3}	Output low voltage (3) ($\overline{\text{RESET}}$ pin as I/O)	I_{OL} = 2.1mA, V_{CC} = 5V I_{OL} = 0.8mA, V_{CC} = 3V			0.7 0.5	
V_{OH3}	Output high voltage (4) ($\overline{\text{RESET}}$ pin as I/O)	I_{OH} = -0.6mA, V_{CC} = 5V I_{OH} = -0.4mA, V_{CC} = 3V	3.8 2.2			
I_{IL}	Input leakage current I/O pin	V_{CC} = 5.5V, pin low (absolute value)			1	µA
I_{IH}	Input leakage current I/O pin	V_{CC} = 5.5V, pin high (absolute value)			1	
R_{RST}	Reset pull-up resistor		30		200	kW
R_{PU}	I/O pin pull-up resistor		20		50	

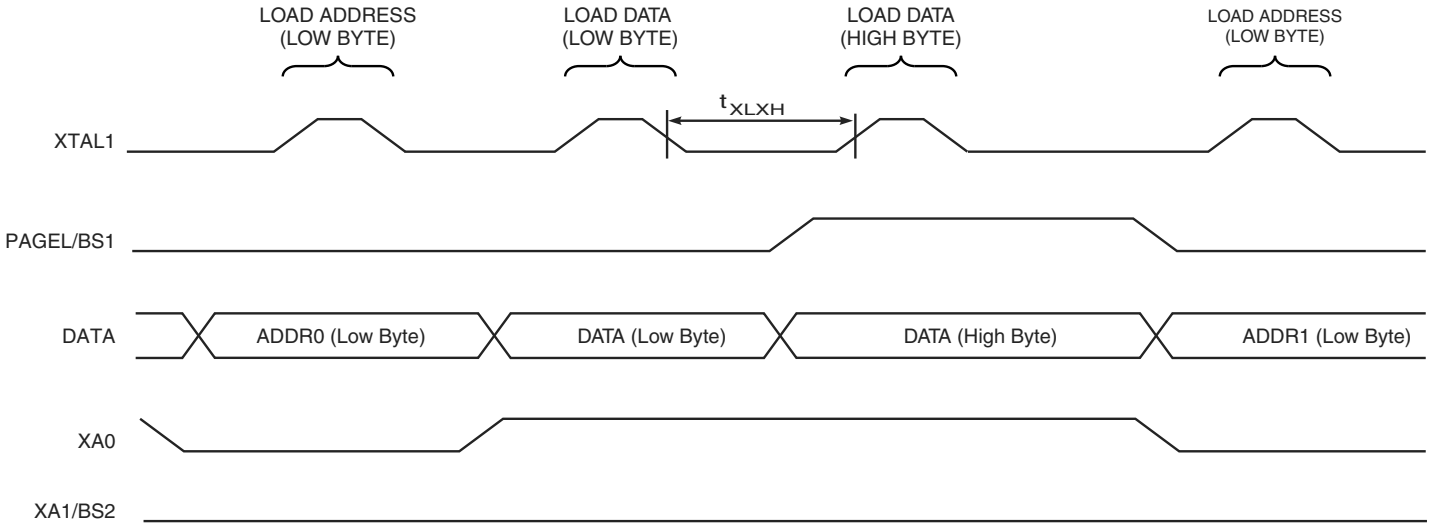
Symbol	Parameter	Condition	Minimum	Typical	Maximum	Units
I_{CC}	Power supply current	Active 8MHz, V_{CC} = 3V, RC osc, PRR = 0xFF		3.5	5	mA
		Active 16MHz, V_{CC} = 5V, Ext Clock, PRR = 0xFF		10.5	15	
		Idle 8MHz, V_{CC} = 3V, RC Osc		1.5	2	
		Idle 16MHz, V_{CC} = 5V, Ext Clock		4.5	7	
	Power-down mode (5)	WDT enabled, V_{CC} = 3V 25°C		7		µA
		WDT enabled, V_{CC} = 3V 125°C			70	
		WDT enabled, V_{CC} = 5V 25°C		10		
		WDT enabled, V_{CC} = 5V 125°C			110	
		WDT disabled, V_{CC} = 3V 25°C		0.5		
		WDT disabled, V_{CC} = 3V 125°C			35	
		WDT disabled, V_{CC} = 5V 25°C		1		
		WDT disabled, V_{CC} = 5V 125°C			55	
V_{REF}	Internal voltage reference (7)	@25°C	2.46	2.56	2.66	V
	Analog comparator input common mode range		0.1		V_{CC} - 0.1	
V_{ACIO}	Analog comparator input offset voltage	Input offset voltage $0.1<V_{IN}<V_{CC}$ - 0.1V		±1.5	±10	mV
		With ±10mV Hysteresis $0.1<V_{IN}<V_{CC}$ - 0.1V		±10	±20	
		With ±25mV Hysteresis $0.1<V_{IN}<V_{CC}$ - 0.1V		±25	±60	
I_{ACLK}	Analog comparator input leakage current	V_{CC} = 5V V_{IN} = V_{CC}/2	-50		50	nA
t_{ACID}	Analog comparator propagation delay	V_{CC} = 2.7V V_{CC} = 5.0V		50 (6)		ns

Note: 1. “Maximum” means the highest value where the pin is guaranteed to be read as low.

2. “Minimum” means the lowest value where the pin is guaranteed to be read as high.

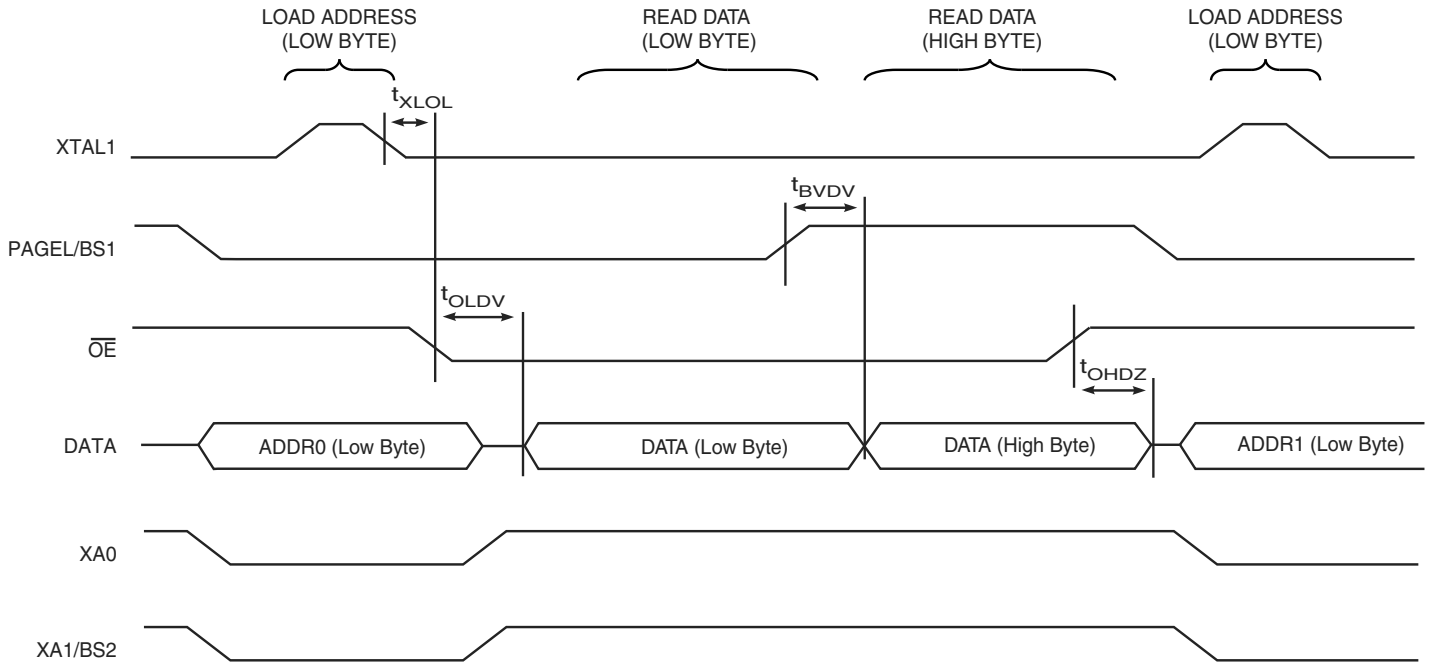
3. Although each I/O port can sink more than the test conditions (20mA at V_{CC} = 5V, 10mA at V_{CC} = 3V) under steady state conditions (non-transient), the following must be observed:
SO20 and TQFN Package:
1] The sum of all I_{OL}, for all ports, should not exceed 400mA.
2] The sum of all I_{OL}, for ports B6 - B7, D0 - D3, E0 should not exceed 100mA.
3] The sum of all I_{OL}, for ports B0 - B1, D4, E1 - E2 should not exceed 100mA.

Figure 22-6. Parallel programming timing, loading sequence with timing requirements [1].



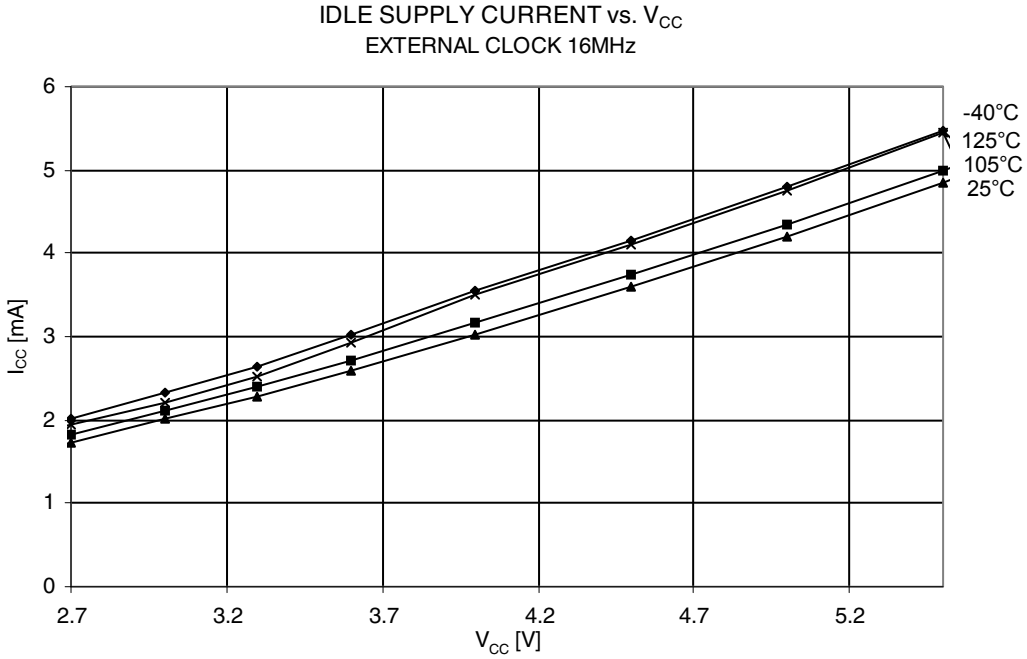
Note: 1. The timing requirements shown in Figure 22-5 on page 276 (that is, t_{DVXH}, t_{XHXL}, and t_{XLDX}) also apply to loading operation.

Figure 22-7. Parallel programming timing, reading sequence (within the same page) with timing requirements [1].



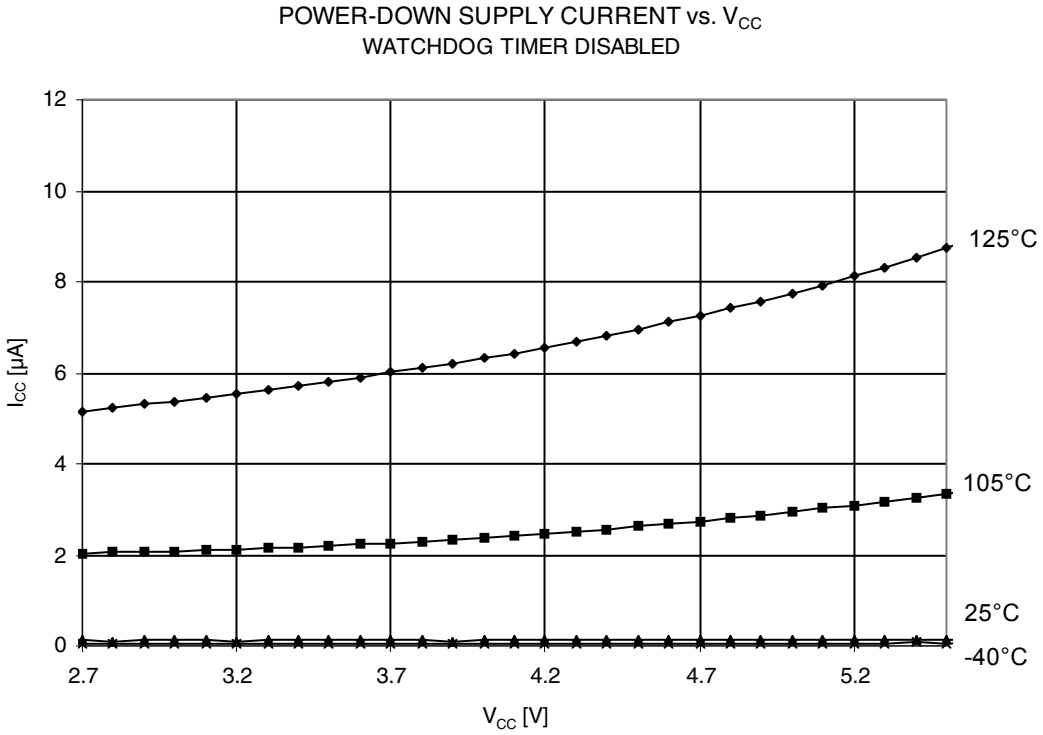
Note: 1. The timing requirements shown in Figure 22-5 on page 276 (that is, t_{DVXH}, t_{XHXL}, and t_{XLDX}) also apply to reading operation.

Figure 23-8. Idle supply current vs. V_{CC} (external clock, 16MHz).



23.3 Power-Down Supply Current

Figure 23-9. Power-down supply current vs. V_{CC} (watchdog timer disabled).



7. ADC measurement reports abnormal values with PSC2-synchronized conversions

When using ADC in synchronized mode, an unexpected extra Single ended conversion can spuriously re-start.This can occur when the End of conversion and the Trigger event occur at the same time.

Work around:

No workaround

8. Over-consumption in power down sleep mode.

In Power-down mode, an extra power consumption up to 500µA may occur.

Work around:

No workaround

27.4 Errata AT90PWM81 revD

- **Clock Switch disable**
- **Crystal oscillator control with Clock Switch**
- **BOD disable fuse**
- **Flash and EEPROM programming failure if CPU clock is switched**
- **ADC Amplifier measurement is unstable**
- **ADC measurement reports abnormal values with PSC2-synchronized conversions**
- **Over-consumption in power down sleep mode**

1. Clock Switch enable & disable

After a “Enable Clock Source” or a “Disable Clock Source” command, the command is still active until the next access of CLKCSR register. If CLKSEL is written with a new value, the corresponding clock will be unintentionnaly enabled or disabled.

Work around:

Atter the Enable or Disable command, write CLKCSR with value 1<<CLKCCE

2. Crystal oscillator control with Clock Switch

When a Xtal oscillator is active and CLKSELR is written with a new value for the selection of another clock source (for instance RC or WD) , the Xtal oscillator gain is not correct.

Work around:

After the commands “Enable Clock Source” and “Clock Source Switching”, write back CLKSELR with the values corresponding to the active Xtal oscillator

3. BOD disable fuse

It is strongly advised to keep the BOD active. Indeed, the RC oscillator may lock if it is activated when the power suppy goes at a low voltage.

Work around:

If it is mandatory to disable the BOD, do not set the RC oscillator as clock source during reset and makes sure the RC oscillator is never active when the power supply is below the lowest POR voltage (2.6V).