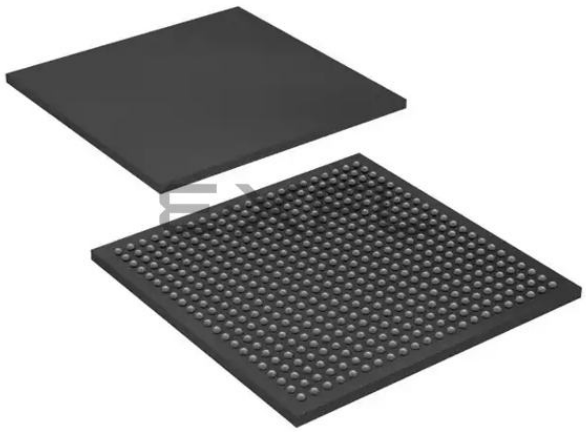

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1079
Number of Logic Elements/Cells	21580
Total RAM Bits	1229184
Number of I/O	230
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1agx20cf484i6n

- Main device features:
  - TriMatrix memory consisting of three RAM block sizes to implement true dual-port memory and first-in first-out (FIFO) buffers with performance up to 380 MHz
  - Up to 16 global clock networks with up to 32 regional clock networks per device
  - High-speed DSP blocks provide dedicated implementation of multipliers, multiply-accumulate functions, and finite impulse response (FIR) filters
  - Up to four enhanced phase-locked loops (PLLs) per device provide spread spectrum, programmable bandwidth, clock switch-over, and advanced multiplication and phase shifting
  - Support for numerous single-ended and differential I/O standards
  - High-speed source-synchronous differential I/O support on up to 47 channels
  - Support for source-synchronous bus standards, including SPI-4 Phase 2 (POS-PHY Level 4), SFI-4.1, XSBI, UTOPIA IV, NPSI, and CSIX-L1
  - Support for high-speed external memory including DDR and DDR2 SDRAM, and SDR SDRAM
  - Support for multiple intellectual property megafunctions from Altera® MegaCore® functions and Altera Megafunction Partners Program (AMPP^{SM})
  - Support for remote configuration updates

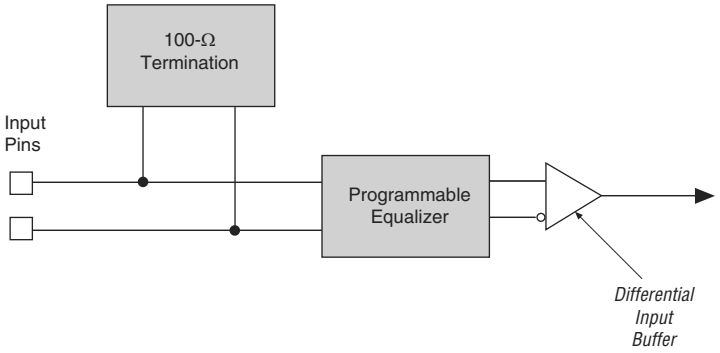
Table 1–1 lists Arria GX device features for FineLine BGA (FBGA) with flip chip packages.

Table 1–1. Arria GX Device Features (Part 1 of 2)

Feature	EP1AGX20C	EP1AGX35C/D		EP1AGX50C/D		EP1AGX60C/D/E			EP1AGX90E
	C	C	D	C	D	C	D	E	E
Package	484-pin, 780-pin (Flip chip)	484-pin (Flip chip)	780-pin (Flip chip)	484-pin (Flip chip)	780-pin, 1152-pin (Flip chip)	484-pin (Flip chip)	780-pin (Flip chip)	1152-pin (Flip chip)	1152-pin (Flip chip)
ALMs	8,632	13,408		20,064		24,040			36,088
Equivalent logic elements (LEs)	21,580	33,520		50,160		60,100			90,220
Transceiver channels	4	4	8	4	8	4	8	12	12
Transceiver data rate	600 Mbps to 3.125 Gbps	600 Mbps to 3.125 Gbps		600 Mbps to 3.125 Gbps		600 Mbps to 3.125 Gbps			600 Mbps to 3.125 Gbps
Source-synchronous receive channels	31	31	31	31	31, 42	31	31	42	47

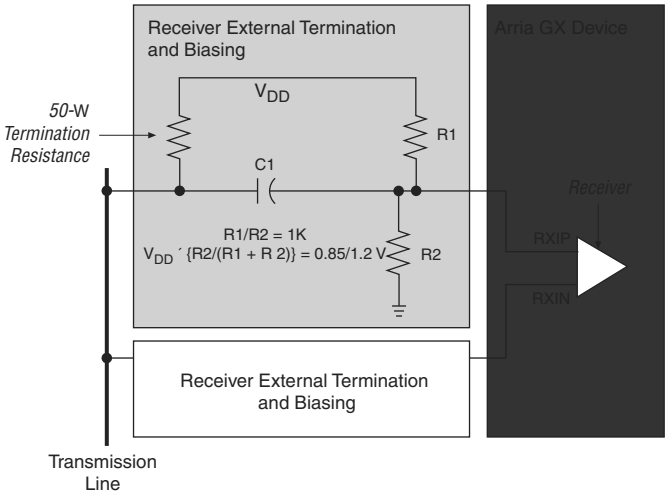
The receiver has 100-Ω on-chip differential termination (R_D OCT) for different protocols, as shown in Figure 2–11. You can disable the receiver's internal termination if external terminations and biasing are provided. The receiver and transmitter differential termination method can be set independently of each other.

Figure 2–11. Receiver Input Buffer



If a design uses external termination, the receiver must be externally terminated and biased to 0.85 V or 1.2 V. Figure 2–12 shows an example of an external termination and biasing circuit.

Figure 2–12. External Termination and Biasing Circuit



Programmable Equalizer

The Arria GX receivers provide a programmable receiver equalization feature to compensate for the effects of channel attenuation for high-speed signaling. PCB traces carrying these high-speed signals have low-pass filter characteristics. Impedance mismatch boundaries can also cause signal degradation. Equalization in the receiver diminishes the lossy attenuation effects of the PCB at high frequencies.

You can dynamically put the PCI Express (PIPE) mode transceiver in reverse parallel loopback by controlling the `tx_detectrxloopback` port instantiated in the MegaWizard Plug-In Manager. A high on the `tx_detectrxloopback` port in P0 power state puts the transceiver in reverse parallel loopback. A high on the `tx_detectrxloopback` port in any other power state does not put the transceiver in reverse parallel loopback.

As seen in Figure 2–21, the serial data received on the `rx_datain` port in reverse parallel loopback goes through the CRU, deserializer, word aligner, and the rate matcher blocks. The parallel data at the output of the receiver rate matcher block is looped back to the input of the transmitter serializer block. The serializer converts the parallel data to serial data and feeds it to the transmitter output buffer that drives the data out on the `tx_dataout` port. The data at the output of the rate matcher also goes through the 8B/10B decoder, byte deserializer, and receiver phase compensation FIFO before being fed to the PLD on the `rx_dataout` port.

Reset and Powerdown

Arria GX transceivers offer a power saving advantage with their ability to shut off functions that are not needed.

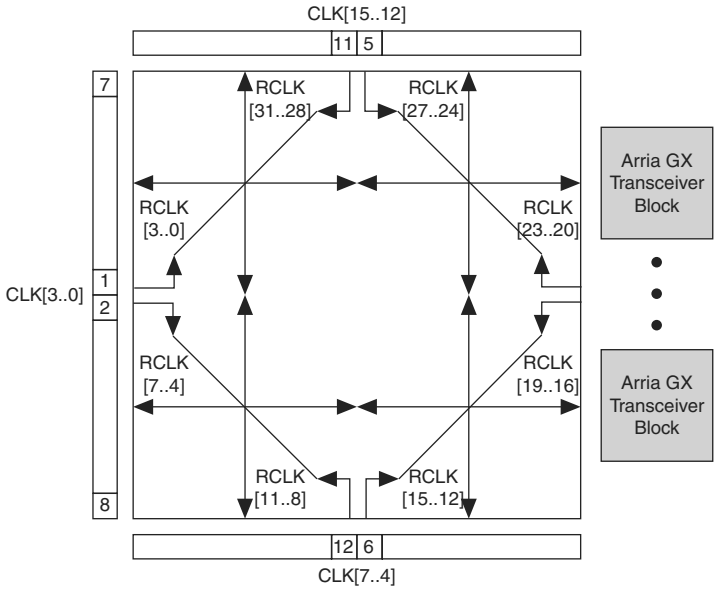
The following three reset signals are available per transceiver channel and can be used to individually reset the digital and analog portions within each channel:

- `tx_digitalreset`
- `rx_analogreset`
- `rx_digitalreset`

The following two powerdown signals are available per transceiver block and can be used to shut down an entire transceiver block that is not being used:

- `gxb_powerdown`
- `gxb_enable`

Figure 2–24. Regional Clock Resources in Arria GX Devices



For the RCLK or GCLK network to route into the transceiver, a local route input output (LRIO) channel is required. Each LRIO clock region has up to eight clock paths and each transceiver block has a maximum of eight clock paths for connecting with LRIO clocks. These resources are limited and determine the number of clocks that can be used between the PLD and transceiver blocks. Table 2–7 and Table 2–8 list the number of LRIO resources available for Arria GX devices with different numbers of transceiver blocks.

Table 2–7. Available Clocking Connections for Transceivers in EP1AGX35D, EP1AGX50D, and EP1AGX60D

Source	Clock Resource		Transceiver	
	Global Clock	Regional Clock	Bank13 8 Clock I/O	Bank14 8 Clock I/O
Region0 8 LRIO clock	✓	RCLK 20-27	✓	—
Region1 8 LRIO clock	✓	RCLK 12-19	—	✓

Table 2–8. Available Clocking Connections for Transceivers in EP1AGX60E and EP1AGX90E

Source	Clock Resource		Transceiver		
	Global Clock	Regional Clock	Bank13 8 Clock I/O	Bank14 8 Clock I/O	Bank15 8 Clock I/O
Region0 8 LRIO clock	✓	RCLK 20-27	✓	—	—
Region1 8 LRIO clock	✓	RCLK 20-27	✓	✓	—
Region2 8 LRIO clock	✓	RCLK 12-19	—	✓	✓
Region3 8 LRIO clock	✓	RCLK 12-19	—	—	✓

Table 2–10 lists the routing scheme for Arria GX device.

Table 2–10. Arria GX Device Routing Scheme

Source	Destination															
	Shared Arithmetic Chain	Carry Chain	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	R24 Interconnect	C4 Interconnect	C16 Interconnect	ALM	M512 RAM Block	M4K RAM Block	M-RAM Block	DSP Blocks	Column IOE	Row IOE
Shared arithmetic chain	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—
Carry chain	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—
Register chain	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—
Local interconnect	—	—	—	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓
Direct link interconnect	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—
R4 interconnect	—	—	—	✓	—	✓	✓	✓	✓	—	—	—	—	—	—	—
R24 interconnect	—	—	—	—	—	✓	✓	✓	✓	—	—	—	—	—	—	—
C4 interconnect	—	—	—	✓	—	✓	—	✓	—	—	—	—	—	—	—	—
C16 interconnect	—	—	—	—	—	✓	✓	✓	✓	—	—	—	—	—	—	—
ALM	✓	✓	✓	✓	✓	✓	—	✓	—	—	—	—	—	—	—	—
M512 RAM block	—	—	—	✓	✓	✓	—	✓	—	—	—	—	—	—	—	—
M4K RAM block	—	—	—	✓	✓	✓	—	✓	—	—	—	—	—	—	—	—
M-RAM block	—	—	—	—	✓	✓	✓	✓	—	—	—	—	—	—	—	—
DSP blocks	—	—	—	—	✓	✓	—	✓	—	—	—	—	—	—	—	—
Column IOE	—	—	—	—	✓	—	—	✓	✓	—	—	—	—	—	—	—
Row IOE	—	—	—	—	✓	✓	✓	✓	—	—	—	—	—	—	—	—

TriMatrix Memory

TriMatrix memory consists of three types of RAM blocks: M512, M4K, and M-RAM. Although these memory blocks are different, they can all implement various types of memory with or without parity, including true dual-port, simple dual-port, and single-port RAM, ROM, and FIFO buffers. Table 2–11 lists the size and features of the different RAM blocks.

Table 2–11. TriMatrix Memory Features (Part 1 of 2)

Memory Feature	M512 RAM Block (32 × 18 Bits)	M4K RAM Block (128 × 36 Bits)	M-RAM Block (4K × 144 Bits)
Maximum performance	345 MHz	380 MHz	290 MHz
True dual-port memory	—	✓	✓
Simple dual-port memory	✓	✓	✓
Single-port memory	✓	✓	✓
Shift register	✓	✓	—

Table 2–11. TriMatrix Memory Features (Part 2 of 2)

Memory Feature	M512 RAM Block (32 × 18 Bits)	M4K RAM Block (128 × 36 Bits)	M-RAM Block (4K × 144 Bits)
ROM	✓	✓	—
FIFO buffer	✓	✓	✓
Pack mode	—	✓	✓
Byte enable	✓	✓	✓
Address clock enable	—	✓	✓
Parity bits	✓	✓	✓
Mixed clock mode	✓	✓	✓
Memory initialization file (**.mif**)	✓	✓	—
Simple dual-port memory mixed width support	✓	✓	✓
True dual-port memory mixed width support	—	✓	✓
Power-up conditions	Outputs cleared	Outputs cleared	Outputs unknown
Register clears	Output registers	Output registers	Output registers
Mixed-port read-during-write	Unknown output/old data	Unknown output/old data	Unknown output
Configurations	512 × 1 256 × 2 128 × 4 64 × 8 64 × 9 32 × 16 32 × 18	4K × 1 2K × 2 1K × 4 512 × 8 512 × 9 256 × 16 256 × 18 128 × 32 128 × 36	64K × 8 64K × 9 32K × 16 32K × 18 16K × 32 16K × 36 8K × 64 8K × 72 4K × 128 4K × 144

TriMatrix memory provides three different memory sizes for efficient application support. The Quartus II software automatically partitions the user-defined memory into the embedded memory blocks using the most efficient size combinations. You can also manually assign the memory to a specific block size or a mixture of block sizes.

M512 RAM Block

The M512 RAM block is a simple dual-port memory block and is useful for implementing small FIFO buffers, DSP, and clock domain transfer applications. Each block contains 576 RAM bits (including parity bits). M512 RAM blocks can be configured in the following modes:

- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

Table 2–13. DSP Blocks in Arria GX Devices *(Note 1)*

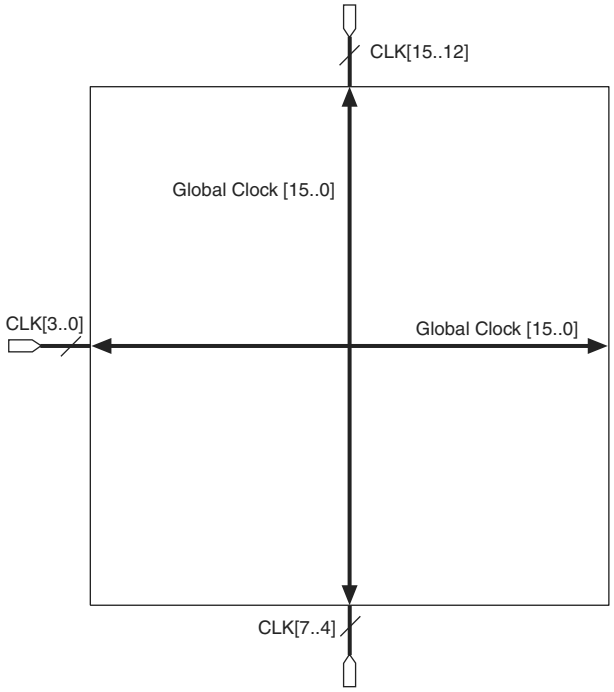
Device	DSP Blocks	Total 9 × 9 Multipliers	Total 18 × 18 Multipliers	Total 36 × 36 Multipliers
EP1AGX20	10	80	40	10
EP1AGX35	14	112	56	14
EP1AGX50	26	208	104	26
EP1AGX60	32	256	128	32
EP1AGX90	44	352	176	44

Note to Table 2–13:

(1) This list only shows functions that can fit into a single DSP block. Multiple DSP blocks can support larger multiplication functions.

Additionally, DSP block input registers can efficiently implement shift registers for FIR filter applications. DSP blocks support Q1.15 format rounding and saturation. Figure 2–51 shows a top-level diagram of the DSP block configured for 18 × 18-bit multiplier mode.

Figure 2–54. Global Clocking



Regional Clock Network

There are eight RCLK networks (RCLK[7..0]) in each quadrant of the Arria GX device that are driven by the dedicated CLK[15..12] and CLK[7..0] input pins, by PLL outputs, or by internal logic. The regional clock networks provide the lowest clock delay and skew for logic contained in a single quadrant. The CLK pins symmetrically drive the RCLK networks in a particular quadrant, as shown in Figure 2–55.

Table 2–20. Global and Regional Clock Connections from Top Clock Pins and Enhanced PLL Outputs

Top Side Global and Regional Clock Network Connectivity	DLLCLK	CLK12	CLK13	CLK14	CLK15	RCLK24	RCLK25	RCLK26	RCLK27	RCLK28	RCLK29	RCLK30	RCLK31
Clock pins													
CLK12p	✓	✓	✓	—	—	✓	—	—	—	✓	—	—	—
CLK13p	✓	✓	✓	—	—	—	✓	—	—	—	✓	—	—
CLK14p	✓	—	—	✓	✓	—	—	✓	—	—	—	✓	—
CLK15p	✓	—	—	✓	✓	—	—	—	✓	—	—	—	✓
CLK12n	—	✓	—	—	—	✓	—	—	—	✓	—	—	—
CLK13n	—	—	✓	—	—	—	✓	—	—	—	✓	—	—
CLK14n	—	—	—	✓	—	—	—	✓	—	—	—	✓	—
CLK15n	—	—	—	—	✓	—	—	—	✓	—	—	—	✓
Drivers from internal logic													
GCLKDRV0	—	✓	—	—	—	—	—	—	—	—	—	—	—
GCLKDRV1	—	—	✓	—	—	—	—	—	—	—	—	—	—
GCLKDRV2	—	—	—	✓	—	—	—	—	—	—	—	—	—
GCLKDRV3	—	—	—	—	✓	—	—	—	—	—	—	—	—
RCLKDRV0	—	—	—	—	—	✓	—	—	—	✓	—	—	—
RCLKDRV1	—	—	—	—	—	—	✓	—	—	—	✓	—	—
RCLKDRV2	—	—	—	—	—	—	—	✓	—	—	—	✓	—
RCLKDRV3	—	—	—	—	—	—	—	—	✓	—	—	—	✓
RCLKDRV4	—	—	—	—	—	✓	—	—	—	✓	—	—	—
RCLKDRV5	—	—	—	—	—	—	✓	—	—	—	✓	—	—
RCLKDRV6	—	—	—	—	—	—	—	✓	—	—	—	✓	—
RCLKDRV7	—	—	—	—	—	—	—	—	✓	—	—	—	✓
Enhanced PLL5 outputs													
c0	✓	✓	✓	—	—	✓	—	—	—	✓	—	—	—
c1	✓	✓	✓	—	—	—	✓	—	—	—	✓	—	—
c2	✓	—	—	✓	✓	—	—	✓	—	—	—	✓	—
c3	✓	—	—	✓	✓	—	—	—	✓	—	—	—	✓
c4	✓	—	—	—	—	✓	—	✓	—	✓	—	✓	—
c5	✓	—	—	—	—	—	✓	—	✓	—	✓	—	✓
Enhanced PLL 11 outputs													
c0	—	✓	✓	—	—	✓	—	—	—	✓	—	—	—
c1	—	✓	✓	—	—	—	✓	—	—	—	✓	—	—
c2	—	—	—	✓	✓	—	—	✓	—	—	—	✓	—
c3	—	—	—	✓	✓	—	—	—	✓	—	—	—	✓
c4	—	—	—	—	—	✓	—	✓	—	✓	—	✓	—
c5	—	—	—	—	—	—	✓	—	✓	—	✓	—	✓

Table 4–12. Typical Pre-Emphasis (First Post-Tap), *(Note 1)*

V_{cc} HTX = 1.5 V	First Post Tap Pre-Emphasis Level				
V_{OD} Setting (mV)	1	2	3	4	5
1000	—	—	23%	36%	49%
1200	—	—	17%	25%	35%

Note to Table 4–12:

(1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

Table 4–13. Typical Pre-Emphasis (First Post-Tap), *(Note 1)*

V_{cc} HTX = 1.2 V	First Post Tap Pre-Emphasis Level				
V_{OD} Setting (mV)	1	2	3	4	5
	TX Term = 100 Ω				
320	24%	61%	114%	—	—
480	—	31%	55%	86%	121%
640	—	20%	35%	54%	72%
800	—	—	23%	36%	49%
960	—	—	18%	25%	35%

Note to Table 4–13:

(1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

DC Electrical Characteristics

Table 4–14 lists the Arria GX device family DC electrical characteristics.

Table 4–14. Arria GX Device DC Operating Conditions (Part 1 of 2) *(Note 1)*

Symbol	Parameter	Conditions	Device	Min	Typ	Max	Units
I_I	Input pin leakage current	$V_I = V_{CCIOmax}$ to 0 V *(2)*	All	–10	—	10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V *(2)*	All	–10	—	10	µA
I_{CCINT0}	V_{CCINT} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25 °C	EP1AGX20/35	—	0.30	*(3)*	A
			EP1AGX50/60	—	0.50	*(3)*	A
			EP1AGX90	—	0.62	*(3)*	A
I_{CCPD0}	V_{CCPD} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25 °C, V_{CCPD} = 3.3V	EP1AGX20/35	—	2.7	*(3)*	mA
			EP1AGX50/60	—	3.6	*(3)*	mA
			EP1AGX90	—	4.3	*(3)*	mA
I_{CCIO0}	V_{CCIO} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25 °C	EP1AGX20/35	—	4.0	*(3)*	mA
			EP1AGX50/60	—	4.0	*(3)*	mA
			EP1AGX90	—	4.0	*(3)*	mA

Table 4–14. Arria GX Device DC Operating Conditions (Part 2 of 2) *(Note 1)*

Symbol	Parameter	Conditions	Device	Min	Typ	Max	Units
R_{CONF} *(4)*	Value of I/O pin pull-up resistor before and during configuration	V_i = 0, V_{CCIO} = 3.3 V	—	10	25	50	kΩ
		V_i = 0, V_{CCIO} = 2.5 V	—	15	35	70	kΩ
		V_i = 0, V_{CCIO} = 1.8 V	—	30	50	100	kΩ
		V_i = 0, V_{CCIO} = 1.5 V	—	40	75	150	kΩ
		V_i = 0, V_{CCIO} = 1.2 V	—	50	90	170	kΩ
	Recommended value of I/O pin external pull-down resistor before and during configuration	—	—	—	1	2	kΩ

Notes to Table 4–14:

(1) Typical values are for T_A = 25 °C, V_{CCINT} = 1.2 V, and V_{CCIO} = 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

(2) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, 1.5, and 1.2 V).

(3) Maximum values depend on the actual TJ and design utilization. For maximum values, refer to the Excel-based PowerPlay Early Power Estimator (available at PowerPlay Early Power Estimators (EPE) and Power Analyzer) or the Quartus® II PowerPlay Power Analyzer feature for maximum values. For more information, refer to "Power Consumption" on page 4–25.

(4) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.

I/O Standard Specifications

Table 4–15 through Table 4–38 show the Arria GX device family I/O standard specifications.

Table 4–15. LVTTL Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO} *(1)*	Output supply voltage	—	3.135	3.465	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.3	0.8	V
V_{OH}	High-level output voltage	I_{OH} = –4 mA *(2)*	2.4	—	V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA *(2)*	—	0.45	V

Notes to Table 4–15:

(1) Arria GX devices comply to the narrow range for the supply voltage as specified in the EIA/JEDEC Standard, JESD8-B.

(2) This specification is supported across all the programmable drive strength settings available for this I/O standard.

Table 4–16. LVCMOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO} *(1)*	Output supply voltage	—	3.135	3.465	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.3	0.8	V
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, I_{OH} = –0.1 mA *(2)*	V_{CCIO} – 0.2	—	V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, I_{OL} = 0.1 mA *(2)*	—	0.2	V

Notes to Table 4–16:

(1) Arria GX devices comply to the narrow range for the supply voltage as specified in the EIA/JEDEC Standard, JESD8-B.

(2) This specification is supported across all the programmable drive strength available for this I/O standard.

Table 4–36. 1.8-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	1.71	1.80	1.89	V
V_{REF}	Input reference voltage	—	0.85	0.90	0.95	V
V_{TT}	Termination voltage	—	0.85	0.90	0.95	V
V_{IH} (DC)	DC high-level input voltage	—	V_{REF} + 0.1	—	—	V
V_{IL} (DC)	DC low-level input voltage	—	–0.3	—	V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage	—	V_{REF} + 0.2	—	—	V
V_{IL} (AC)	AC low-level input voltage	—	—	—	V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(1)*	V_{CCIO} – 0.4	—	—	V
V_{OL}	Low-level output voltage	I_{OH} = –8 mA *(1)*	—	—	0.4	V

Note to Table 4–36:

(1) This specification is supported across all the programmable drive settings available for this I/O standard, as shown in the *Arria GX Architecture* chapter.

Table 4–37. 1.8-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	1.71	1.80	1.89	V
V_{REF}	Input reference voltage	—	0.85	0.90	0.95	V
V_{TT}	Termination voltage	—	0.85	0.90	0.95	V
V_{IH} (DC)	DC high-level input voltage	—	V_{REF} + 0.1	—	—	V
V_{IL} (DC)	DC low-level input voltage	—	–0.3	—	V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage	—	V_{REF} + 0.2	—	—	V
V_{IL} (AC)	AC low-level input voltage	—	—	—	V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(1)*	V_{CCIO} – 0.4	—	—	V
V_{OL}	Low-level output voltage	I_{OH} = –16 mA *(1)*	—	—	0.4	V

Note to Table 4–37:

(1) This specification is supported across all the programmable drive settings available for this I/O standard, as shown in the *Arria GX Architecture* chapter in volume 1 of the *Arria GX Device Handbook*.

Table 4–38. 1.8-V HSTL Class I & II Differential Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage	1.71	1.80	1.89	V
V_{DIF} (DC)	DC input differential voltage	0.2	—	—	V
V_{CM} (DC)	DC common mode input voltage	0.78	—	1.12	V
V_{DIF} (AC)	AC differential input voltage	0.4	—	—	V
V_{OX} (AC)	AC differential cross point voltage	0.68	—	0.9	V

Bus Hold Specifications

Table 4–39 shows the Arria GX device family bus hold specifications.

Table 4–39. Bus Hold Parameters

Parameter	Conditions	V_{CCIO} Level										Units
		1.2 V		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	$V_{IN} > V_{IL}$ (maximum)	22.5	—	25	—	30	—	50	—	70	—	µA
High sustaining current	$V_{IN} < V_{IH}$ (minimum)	–22.5	—	–25	—	–30	—	–50	—	–70	—	µA
Low overdrive current	0 V $< V_{IN} < V_{CCIO}$	—	120	—	160	—	200	—	300	—	500	µA
High overdrive current	0 V < $V_{IN} < V_{CCIO}$	—	–120	—	–160	—	–200	—	–300	—	–500	µA
Bus-hold trip point	—	0.45	0.95	0.5	1.0	0.68	1.07	0.7	1.7	0.8	2.0	V

On-Chip Termination Specifications

Table 4–40 and Table 4–41 define the specification for internal termination resistance tolerance when using series or differential on-chip termination.

Table 4–40. Series On-Chip Termination Specification for Top and Bottom I/O Banks

Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	Industrial Max	Units
25-Ω R_S 3.3/2.5	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.3/2.5V	±30	±30	%
50-Ω R_S 3.3/2.5	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5V	±30	± 30	%
25-Ω R_S 1.8	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8V	±30	±30	%
50-Ω R_S 1.8	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8V	±30	±30	%
50-Ω R_S 1.5	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.5V	±36	±36	%
50-Ω R_S 1.2	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2V	±50	±50	%

For more information about PowerPlay tools, refer to the *PowerPlay Early Power Estimator and PowerPlay Power Analyzer* page and the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

For typical I_{CC} standby specifications, refer to Table 4–14 on page 4–14 .

I/O Timing Model

The DirectDrive technology and MultiTrack interconnect ensures predictable performance, accurate simulation, and accurate timing analysis across all Arria GX device densities and speed grades. This section describes and specifies the performance of I/Os.

All specifications are representative of worst-case supply voltage and junction temperature conditions.

The timing numbers listed in the tables of this section are extracted from the Quartus II software version 7.1.

Preliminary, Correlated, and Final Timing

Timing models can have either preliminary, correlated, or final status. The Quartus II software issues an informational message during design compilation if the timing models are preliminary. Table 4–43 lists the status of the Arria GX device timing models.

- **Preliminary** status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.
- **Correlated** numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.
- **Final timing** numbers are based on complete correlation to actual devices and addressing any minor deviations from the correlated timing model. When the timing models are final, all or most of the Arria GX family devices have been completely characterized and no further changes to the timing model are expected.

Table 4–43. Arria GX Device Timing Model Status

Device	Preliminary	Correlated	Final
EP1AGX20	—	—	✓
EP1AGX35	—	—	✓
EP1AGX50	—	—	✓
EP1AGX60	—	—	✓
EP1AGX90	—	—	✓

Table 4–55. EP1AGX35 Column Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.131	1.131	2.607	ns
		t_H	–1.026	–1.026	–2.330	ns
	GCLK PLL	t_{SU}	2.573	2.573	5.713	ns
		t_H	–2.468	–2.468	–5.436	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.132	1.132	2.607	ns
		t_H	–1.027	–1.027	–2.330	ns
	GCLK PLL	t_{SU}	2.574	2.574	5.715	ns
		t_H	–2.469	–2.469	–5.438	ns
3.3-V PCI	GCLK	t_{SU}	1.256	1.256	2.903	ns
		t_H	–1.151	–1.151	–2.626	ns
	GCLK PLL	t_{SU}	2.698	2.698	6.009	ns
		t_H	–2.593	–2.593	–5.732	ns
3.3-V PCI-X	GCLK	t_{SU}	1.256	1.256	2.903	ns
		t_H	–1.151	–1.151	–2.626	ns
	GCLK PLL	t_{SU}	2.698	2.698	6.009	ns
		t_H	–2.593	–2.593	–5.732	ns
LVDS	GCLK	t_{SU}	1.106	1.106	2.489	ns
		t_H	–1.001	–1.001	–2.212	ns
	GCLK PLL	t_{SU}	2.530	2.530	5.564	ns
		t_H	–2.425	–2.425	–5.287	ns

Table 4–56 lists I/O timing specifications.

Table 4–56. EP1AGX35 Row Pins Output Timing Parameters (Part 1 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	2.904	2.904	6.699	ns
		GCLK PLL	t_{CO}	1.485	1.485	3.627	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.776	2.776	6.059	ns
		GCLK PLL	t_{CO}	1.357	1.357	2.987	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.720	2.720	6.022	ns
		GCLK PLL	t_{CO}	1.301	1.301	2.950	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.776	2.776	6.059	ns
		GCLK PLL	t_{CO}	1.357	1.357	2.987	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.670	2.670	5.753	ns
		GCLK PLL	t_{CO}	1.251	1.251	2.681	ns
2.5 V	4 mA	GCLK	t_{CO}	2.759	2.759	6.033	ns
		GCLK PLL	t_{CO}	1.340	1.340	2.961	ns

Table 4–63. EP1AGX50 Column Pins Output Timing Parameters (Part 3 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.648	2.648	5.777	ns
		GCLK PLL	t_{CO}	1.202	1.202	2.675	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.628	2.628	5.722	ns
		GCLK PLL	t_{CO}	1.185	1.185	2.625	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.606	2.606	5.649	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.552	ns
SSTL-2 CLASS II	20 mA	GCLK	t_{CO}	2.606	2.606	5.636	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.539	ns
SSTL-2 CLASS II	24 mA	GCLK	t_{CO}	2.601	2.601	5.634	ns
		GCLK PLL	t_{CO}	1.160	1.160	2.537	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.643	2.643	5.749	ns
		GCLK PLL	t_{CO}	1.193	1.193	2.639	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.649	2.649	5.708	ns
		GCLK PLL	t_{CO}	1.203	1.203	2.607	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.626	2.626	5.686	ns
		GCLK PLL	t_{CO}	1.182	1.182	2.588	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.630	2.630	5.685	ns
		GCLK PLL	t_{CO}	1.187	1.187	2.586	ns
SSTL-18 CLASS I	12 mA	GCLK	t_{CO}	2.625	2.625	5.669	ns
		GCLK PLL	t_{CO}	1.181	1.181	2.572	ns
SSTL-18 CLASS II	8 mA	GCLK	t_{CO}	2.614	2.614	5.635	ns
		GCLK PLL	t_{CO}	1.170	1.170	2.538	ns
SSTL-18 CLASS II	16 mA	GCLK	t_{CO}	2.623	2.623	5.613	ns
		GCLK PLL	t_{CO}	1.182	1.182	2.516	ns
SSTL-18 CLASS II	18 mA	GCLK	t_{CO}	2.616	2.616	5.621	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.524	ns
SSTL-18 CLASS II	20 mA	GCLK	t_{CO}	2.616	2.616	5.619	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.522	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.637	2.637	5.676	ns
		GCLK PLL	t_{CO}	1.196	1.196	2.570	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.645	2.645	5.659	ns
		GCLK PLL	t_{CO}	1.207	1.207	2.562	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.623	2.623	5.648	ns
		GCLK PLL	t_{CO}	1.185	1.185	2.551	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.627	2.627	5.654	ns
		GCLK PLL	t_{CO}	1.189	1.189	2.557	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.619	2.619	5.647	ns
		GCLK PLL	t_{CO}	1.181	1.181	2.550	ns

Table 4–63. EP1AGX50 Column Pins Output Timing Parameters (Part 4 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
1.8-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.602	2.602	5.574	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.314	ns
1.8-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.604	2.604	5.578	ns
		GCLK PLL	t_{CO}	1.166	1.166	2.325	ns
1.8-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.604	2.604	5.577	ns
		GCLK PLL	t_{CO}	1.166	1.166	2.334	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.637	2.637	5.675	ns
		GCLK PLL	t_{CO}	1.196	1.196	2.569	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.644	2.644	5.651	ns
		GCLK PLL	t_{CO}	1.206	1.206	2.554	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.626	2.626	5.653	ns
		GCLK PLL	t_{CO}	1.188	1.188	2.556	ns
1.5-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.626	2.626	5.655	ns
		GCLK PLL	t_{CO}	1.188	1.188	2.558	ns
1.5-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.620	2.620	5.653	ns
		GCLK PLL	t_{CO}	1.182	1.182	2.556	ns
1.5-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.607	2.607	5.573	ns
		GCLK PLL	t_{CO}	1.169	1.169	2.368	ns
1.5-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.610	2.610	5.571	ns
		GCLK PLL	t_{CO}	1.172	1.172	2.378	ns
1.5-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.612	2.612	5.581	ns
		GCLK PLL	t_{CO}	1.174	1.174	2.391	ns
3.3-V PCI	—	GCLK	t_{CO}	2.786	2.786	5.803	ns
		GCLK PLL	t_{CO}	1.322	1.322	2.697	ns
3.3-V PCI-X	—	GCLK	t_{CO}	2.786	2.786	5.803	ns
		GCLK PLL	t_{CO}	1.322	1.322	2.697	ns
LVDS	—	GCLK	t_{CO}	3.621	3.621	6.969	ns
		GCLK PLL	t_{CO}	2.190	2.190	3.880	ns

Table 4–64 through Table 4–65 list EP1AGX50 regional clock (RCLK) adder values that should be added to the GCLK values. These adder values are used to determine I/O timing when the I/O pin is driven using the regional clock. This applies for all I/O standards supported by Arria GX with general purpose I/O pins.

Table 4–72. EP1AGX90 Row Pins Input Timing Parameters (Part 2 of 2)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
1.8-V HSTL CLASS I	GCLK	t_{SU}	1.159	1.159	2.447	ns
		t_H	–1.054	–1.054	–2.170	ns
	GCLK PLL	t_{SU}	3.212	3.212	6.565	ns
		t_H	–3.107	–3.107	–6.288	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	1.157	1.157	2.441	ns
		t_H	–1.052	–1.052	–2.164	ns
	GCLK PLL	t_{SU}	3.235	3.235	6.597	ns
		t_H	–3.130	–3.130	–6.320	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.185	1.185	2.575	ns
		t_H	–1.080	–1.080	–2.298	ns
	GCLK PLL	t_{SU}	3.238	3.238	6.693	ns
		t_H	–3.133	–3.133	–6.416	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.183	1.183	2.569	ns
		t_H	–1.078	–1.078	–2.292	ns
	GCLK PLL	t_{SU}	3.261	3.261	6.725	ns
		t_H	–3.156	–3.156	–6.448	ns
LVDS	GCLK	t_{SU}	1.098	1.098	2.439	ns
		t_H	–0.993	–0.993	–2.162	ns
	GCLK PLL	t_{SU}	3.160	3.160	6.566	ns
		t_H	–3.055	–3.055	–6.289	ns

Table 4–73 lists I/O timing specifications.

Table 4–73. EP1AGX90 Column Pins Input Timing Parameters (Part 1 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.018	1.018	2.290	ns
		t_H	–0.913	–0.913	–2.013	ns
	GCLK PLL	t_{SU}	3.082	3.082	6.425	ns
		t_H	–2.977	–2.977	–6.148	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.018	1.018	2.290	ns
		t_H	–0.913	–0.913	–2.013	ns
	GCLK PLL	t_{SU}	3.082	3.082	6.425	ns
		t_H	–2.977	–2.977	–6.148	ns
2.5 V	GCLK	t_{SU}	1.028	1.028	2.272	ns
		t_H	–0.923	–0.923	–1.995	ns
	GCLK PLL	t_{SU}	3.092	3.092	6.407	ns
		t_H	–2.987	–2.987	–6.130	ns

Table 4–90 lists clock timing specifications.

Table 4–90. EP1AGX50 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.653	1.653	3.841	ns
t_{COUT}	1.651	1.651	3.839	ns
t_{PLLCIN}	0.245	0.245	0.755	ns
$t_{PLLCOUT}$	0.245	0.245	0.755	ns

EP1AGX60 Clock Timing Parameters

Table 4–91 to Table 4–92 on page 4–82 list the GCLK clock timing parameters for EP1AGX60 devices.

Table 4–91 lists clock timing specifications.

Table 4–91. EP1AGX60 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.531	1.531	3.593	ns
t_{COUT}	1.536	1.536	3.587	ns
t_{PLLCIN}	–0.023	–0.023	0.188	ns
$t_{PLLCOUT}$	–0.018	–0.018	0.182	ns

Table 4–92 lists clock timing specifications.

Table 4–92. EP1AGX60 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.792	1.792	4.165	ns
t_{COUT}	1.792	1.792	4.165	ns
t_{PLLCIN}	0.238	0.238	0.758	ns
$t_{PLLCOUT}$	0.238	0.238	0.758	ns

Table 4–93 through Table 4–94 list the RCLK clock timing parameters for EP1AGX60 devices.

Table 4–93 lists clock timing specifications.

Table 4–93. EP1AGX60 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.382	1.382	3.268	ns
t_{COUT}	1.387	1.387	3.262	ns
t_{PLLCIN}	–0.031	–0.031	0.174	ns
$t_{PLLCOUT}$	–0.026	–0.026	0.168	ns

Table 4–94 lists clock timing specifications.

Table 4–94. EP1AGX60 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.649	1.649	3.835	ns
t_{COUT}	1.651	1.651	3.839	ns
t_{PLLCIN}	0.245	0.245	0.755	ns
$t_{PLLCOUT}$	0.245	0.245	0.755	ns

EP1AGX90 Clock Timing Parameters

Table 4–95 through Table 4–96 list the GCLK clock timing parameters for EP1AGX90 devices.

Table 4–95 lists clock timing specifications.

Table 4–95. EP1AGX90 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.630	1.630	3.799	ns
t_{COUT}	1.635	1.635	3.793	ns
t_{PLLCIN}	–0.422	–0.422	–0.310	ns
$t_{PLLCOUT}$	–0.417	–0.417	–0.316	ns