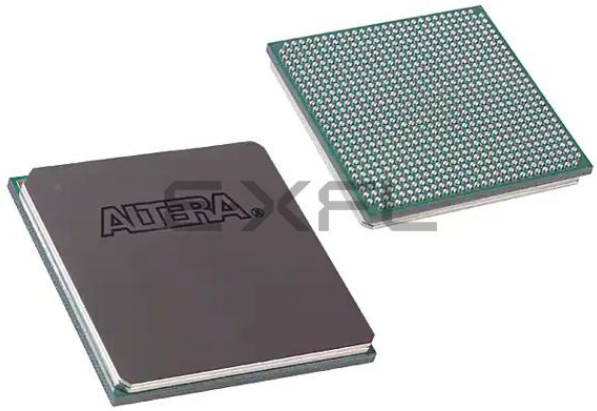
Intel - EP1AGX20CF780C6N Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1079
Number of Logic Elements/Cells	21580
Total RAM Bits	1229184
Number of I/O	341
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1agx20cf780c6n

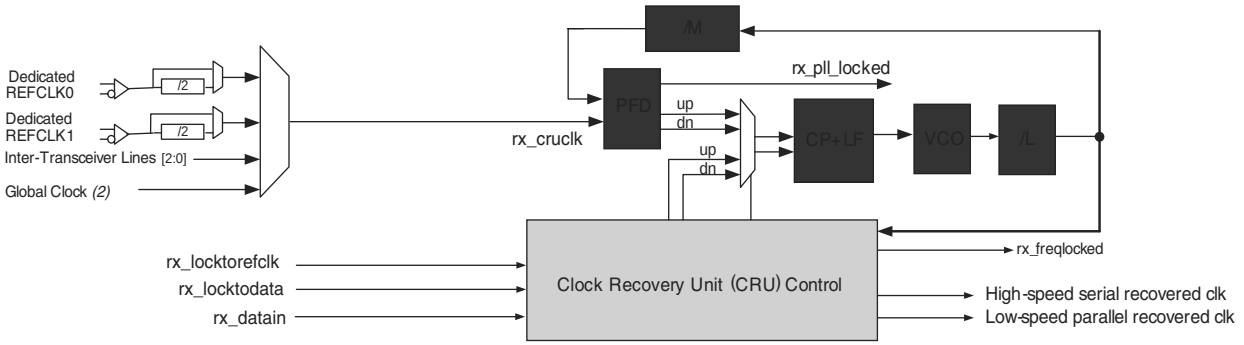
The receiver equalization circuit is comprised of a programmable amplifier. Each stage is a peaking equalizer with a different center frequency and programmable gain. This allows varying amounts of gain to be applied, depending on the overall frequency response of the channel loss. Channel loss is defined as the summation of all losses through the PCB traces, vias, connectors, and cables present in the physical link. The Quartus II software allows five equalization settings for Arria GX devices.

Receiver PLL and Clock Recovery Unit (CRU)

Each transceiver block has four receiver PLLs and CRU units, each of which is dedicated to a receiver channel. The receiver PLL is fed by an input reference clock. The receiver PLL, in conjunction with the CRU, generates two clocks: a high-speed serial recovered clock that clocks the deserializer and a low-speed parallel recovered clock that clocks the receiver's digital logic.

Figure 2–13 shows a block diagram of the receiver PLL and CRU circuits.

Figure 2–13. Receiver PLL and Clock Recovery Unit



Notes to Figure 2–13:

(1) You only need to select the protocol and the available input reference clock frequency in the ALTGXB MegaWizard Plug-In Manager. Based on your selections, the ALTGXB MegaWizard Plug-In Manager automatically selects the necessary /M and /L dividers.

(2) The global clock line must be driven from an input pin only.

The reference clock input to the receiver PLL can be derived from:

- One of the two available dedicated reference clock input pins (`REFCLK0` or `REFCLK1`) of the associated transceiver block
- PLD global clock network (must be driven directly from an input clock pin and cannot be driven by user logic or enhanced PLL)
- Inter-transceiver block lines driven by reference clock input pins of other transceiver blocks

All the parameters listed are programmable in the Quartus II software. The receiver PLL has the following features:

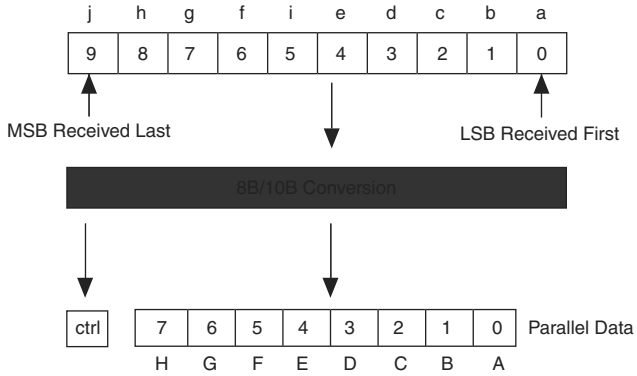
- Operates from 600 Mbps to 3.125 Gbps.
- Uses a reference clock between 50 MHz and 622.08 MHz.
- Programmable bandwidth settings: low, medium, and high.
- Programmable `rx_locktorefclk` (forces the receiver PLL to lock to reference clock) and `rx_locktodata` (forces the receiver PLL to lock to data).

8B/10B Decoder

The 8B/10B decoder is used in all supported functional modes. The 8B/10B decoder takes in 10-bit data from the rate matcher and decodes it into 8-bit data + 1-bit control identifier, thereby restoring the original transmitted data at the receiver. The 8B/10B decoder indicates whether the received 10-bit character is a data or control code through the `rx_ctrldetect` port. If the received 10-bit code group is a control character (`Kx.y`), the `rx_ctrldetect` signal is driven high and if it is a data character (`Dx.y`), the `rx_ctrldetect` signal is driven low.

Figure 2–17 shows a 10-bit code group decoded to an 8-bit data and a 1-bit control indicator.

Figure 2–17. 10-Bit to 8-Bit Conversion



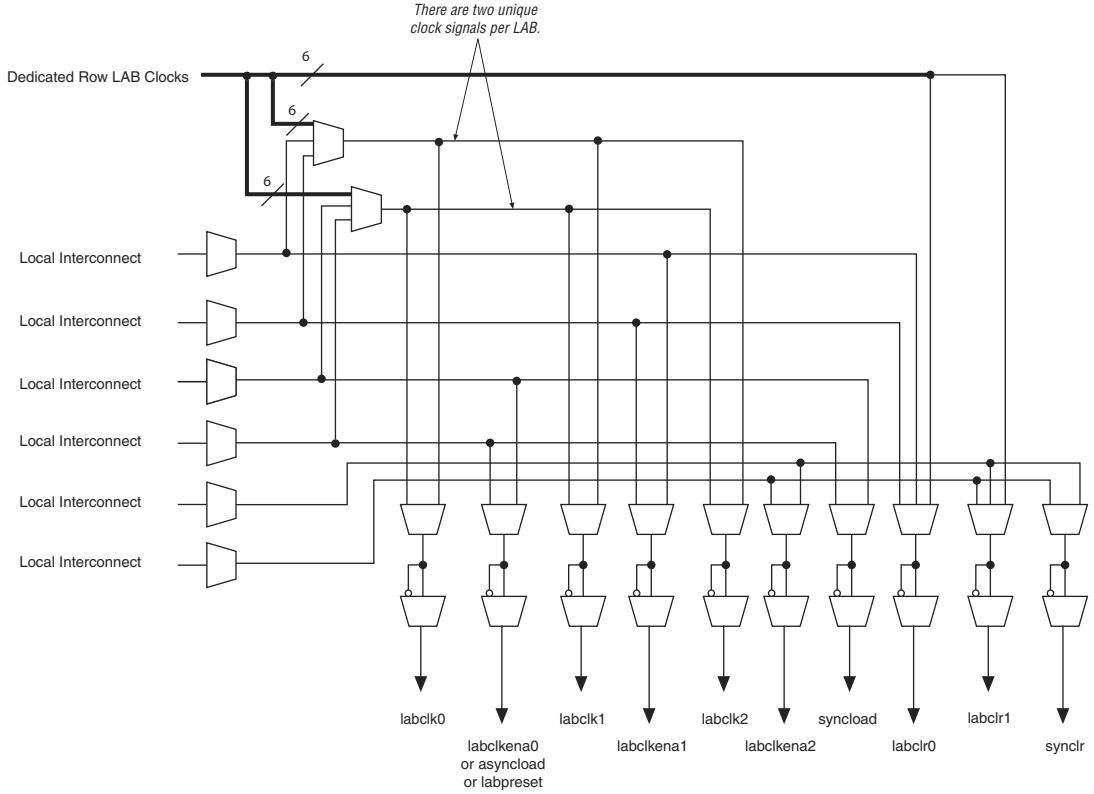
If the received 10-bit code is not a part of valid Dx.y or Kx.y code groups, the 8B/10B decoder block asserts an error flag on the `rx_errdetect` port. If the received 10-bit code is detected with incorrect running disparity, the 8B/10B decoder block asserts an error flag on the `rx_disperr` and `rx_errdetect` ports. The error flag signals (`rx_errdetect` and `rx_disperr`) have the same data path delay from the 8B/10B decoder to the PLD-transceiver interface as the bad code group.

Receiver State Machine

The receiver state machine operates in Basic, GIGE, PCI Express (PIPE), and XAUI modes. In GIGE mode, the receiver state machine replaces invalid code groups with K30.7. In XAUI mode, the receiver state machine translates the XAUI PCS code group to the XAUI XGMII code group.

Figure 2–27 shows the LAB control signal generation circuit.

Figure 2–27. LAB-Wide Control Signals



Adaptive Logic Modules

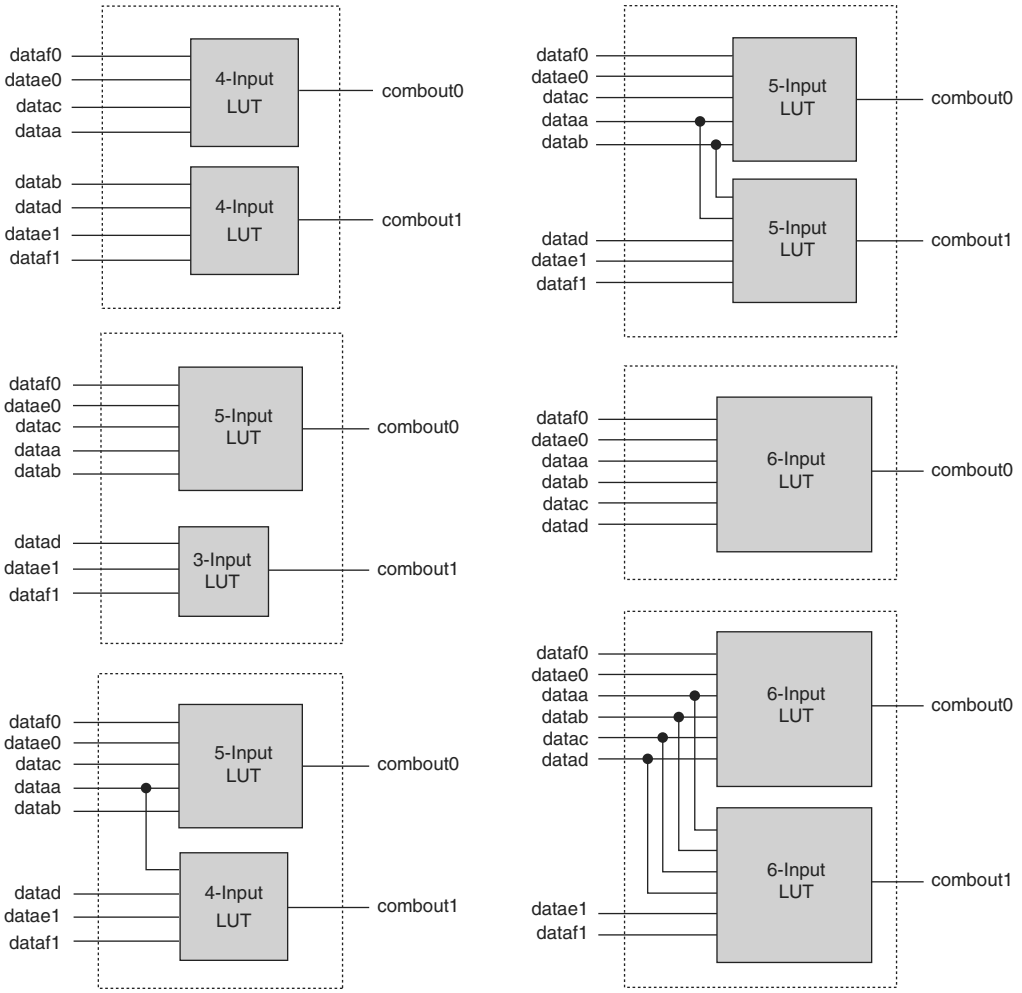
The basic building block of logic in the Arria GX architecture is the ALM. The ALM provides advanced features with efficient logic utilization. Each ALM contains a variety of look-up table (LUT)-based resources that can be divided between two adaptive LUTs (ALUTs). With up to eight inputs to the two ALUTs, one ALM can implement various combinations of two functions. This adaptability allows the ALM to be completely backward-compatible with four-input LUT architectures. One ALM can also implement any function of up to six inputs and certain seven-input functions.

In addition to the adaptive LUT-based resources, each ALM contains two programmable registers, two dedicated full adders, a carry chain, a shared arithmetic chain, and a register chain. Through these dedicated resources, the ALM can efficiently implement various arithmetic functions and shift registers. Each ALM drives all types of interconnects: local, row, column, carry chain, shared arithmetic chain, register chain, and direct link interconnects. Figure 2–28 shows a high-level block diagram of the Arria GX ALM while Figure 2–29 shows a detailed view of all the connections in the ALM.

Normal Mode

Normal mode is suitable for general logic applications and combinational functions. In this mode, up to eight data inputs from the LAB local interconnect are inputs to the combinational logic. Normal mode allows two functions to be implemented in one Arria GX ALM, or an ALM to implement a single function of up to six inputs. The ALM can support certain combinations of completely independent functions and various combinations of functions which have common inputs. Figure 2–30 shows the supported LUT combinations in normal mode.

Figure 2–30. ALM in Normal Mode *(Note 1)*



Note to Figure 2–30:

(1) Combinations of functions with less inputs than those shown are also supported. For example, combinations of functions with the following number of inputs are supported: 4 and 3, 3 and 3, 3 and 2, 5 and 2, and so on.

Normal mode provides complete backward compatibility with four-input LUT architectures. Two independent functions of four inputs or less can be implemented in one Arria GX ALM. In addition, a five-input function and an independent three-input function can be implemented without sharing inputs.

Table 2–12. M-RAM Row Interface Unit Signals (Part 2 of 2)

Unit Interface Block	Input Signals	Output Signals
L4	datain_a[56..42] byteena_a[5..4]	dataout_a[59..48]
L5	datain_a[71..57] byteena_a[7..6]	dataout_a[71..60]
R0	datain_b[14..0] byteena_b[1..0]	dataout_b[11..0]
R1	datain_b[29..15] byteena_b[3..2]	dataout_b[23..12]
R2	datain_b[35..30] addressb[4..0] addr_ena_b clock_b clocken_b renwe_b aclr_b	dataout_b[35..24]
R3	addressb[15..5] datain_b[41..36]	dataout_b[47..36]
R4	datain_b[56..42] byteena_b[5..4]	dataout_b[59..48]
R5	datain_b[71..57] byteena_b[7..6]	dataout_b[71..60]

For more information about TriMatrix memory, refer to the *TriMatrix Embedded Memory Blocks in Arria GX Devices* chapter.

Digital Signal Processing Block

The most commonly used DSP functions are finite impulse response (FIR) filters, complex FIR filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, direct cosine transform (DCT) functions, and correlators. All of these use the multiplier as the fundamental building block. Additionally, some applications need specialized operations such as multiply-add and multiply-accumulate operations. Arria GX devices provide DSP blocks to meet the arithmetic requirements of these functions.

Each Arria GX device has two to four columns of DSP blocks to efficiently implement DSP functions faster than ALM-based implementations. Each DSP block can be configured to support up to:

- Eight 9 × 9-bit multipliers
- Four 18 × 18-bit multipliers
- One 36 × 36-bit multiplier

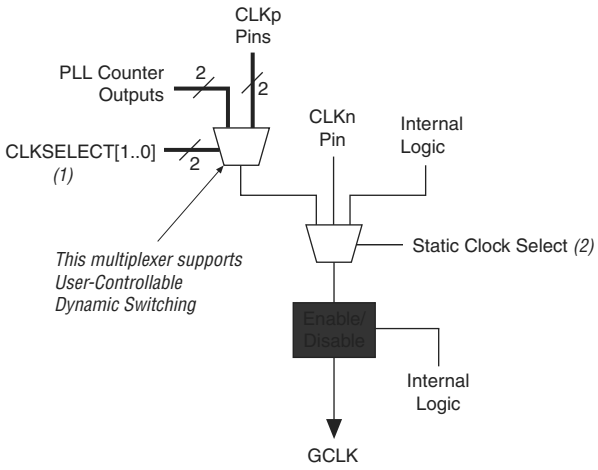
Clock Control Block

Each GCLK, RCLK, and PLL external clock output has its own clock control block. The control block has two functions:

- Clock source selection (dynamic selection for global clocks)
- Clock power-down (dynamic clock enable or disable)

Figure 2–58 through Figure 2–60 show the clock control block for the global clock, regional clock, and PLL external clock output, respectively.

Figure 2–58. Global Clock Control Blocks

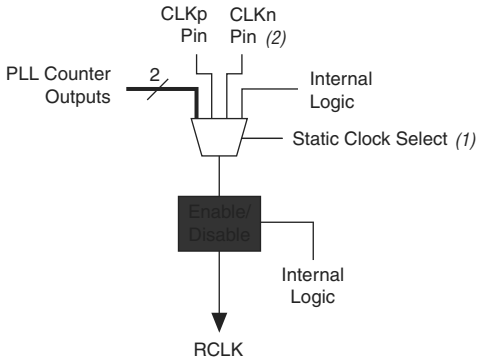


Notes to Figure 2–58:

(1) These clock select signals can be dynamically controlled through internal logic when the device is operating in user mode.

(2) These clock select signals can only be set through a configuration file (SRAM Object File [**.sof**] or Programmer Object File [**.pof**]) and cannot be dynamically controlled during user mode operation.

Figure 2–59. Regional Clock Control Blocks

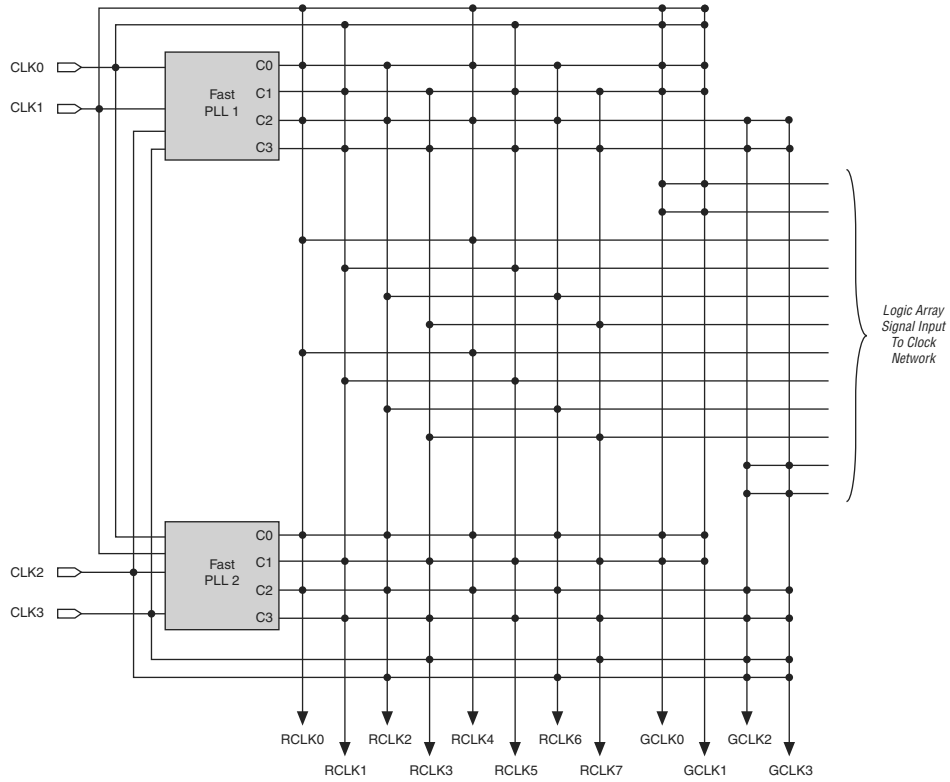


Notes to Figure 2–59:

(1) These clock select signals can only be set through a configuration file (**.sof** or **.pof**) and cannot be dynamically controlled during user mode operation.

(2) Only the `CLKn` pins on the top and bottom of the device feed to regional clock select.

Figure 2–62. Global and Regional Clock Connections from Center Clock Pins and Fast PLL Outputs *(Note 1)*



Note to Figure 2–62:

(1) The global or regional clocks in a fast PLL's quadrant can drive the fast PLL input. A dedicated clock input pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

Table 2–19. Global and Regional Clock Connections from Left Side Clock Pins and Fast PLL Outputs (Part 2 of 2)

Left Side Global & Regional Clock Network Connectivity	CLK0	CLK1	CLK2	CLK3	RCLK0	RCLK1	RCLK2	RCLK3	RCLK4	RCLK5	RCLK6	RCLK7
RCLKDRV7	—	—	—	—	—	—	—	✓	—	—	—	✓
PLL 1 Outputs												
c0	✓	✓	—	—	✓	—	✓	—	✓	—	✓	—
c1	✓	✓	—	—	—	✓	—	✓		✓	—	✓
c2	—	—	✓	✓	✓	—	✓	—	✓	—	✓	—
c3	—	—	✓	✓	—	✓	—	✓	—	✓	—	✓
PLL 2 Outputs												
c0	✓	✓	—	—	—	✓	—	✓	—	✓	—	✓
c1	✓	✓	—	—	✓	—	✓	—	✓	—	✓	—
c2	—	—	✓	✓	—	✓	—	✓	—	✓	—	✓
c3	—	—	✓	✓	✓	—	✓	—	✓	—	✓	—
PLL 7 Outputs												
c0	—	—	✓	✓	—	✓	—	✓	—	—	—	—
c1	—	—	✓	✓	✓	—	✓	—	—	—	—	—
c2	✓	✓	—	—	—	✓	—	✓	—	—	—	—
c3	✓	✓	—	—	✓	—	✓	—	—	—	—	—
PLL 8 Outputs												
c0	—	—	✓	✓	—	—	—	—	✓	—	✓	—
c1	—	—	✓	✓	—	—	—	—	—	✓	—	✓
c2	✓	✓	—	—	—	—	—	—	✓	—	✓	—
c3	✓	✓	—	—	—	—	—	—	—	✓	—	✓

For the specific sustaining current driven through this resistor and overdrive current used to identify the next-driven input level, refer to the *DC & Switching Characteristics* chapter.

Programmable Pull-Up Resistor

Each Arria GX device I/O pin provides an optional programmable pull-up resistor during user mode. If you enable this feature for an I/O pin, the pull-up resistor (typically 25 kΩ) holds the output to the V_{CCIO} level of the output pin's bank.

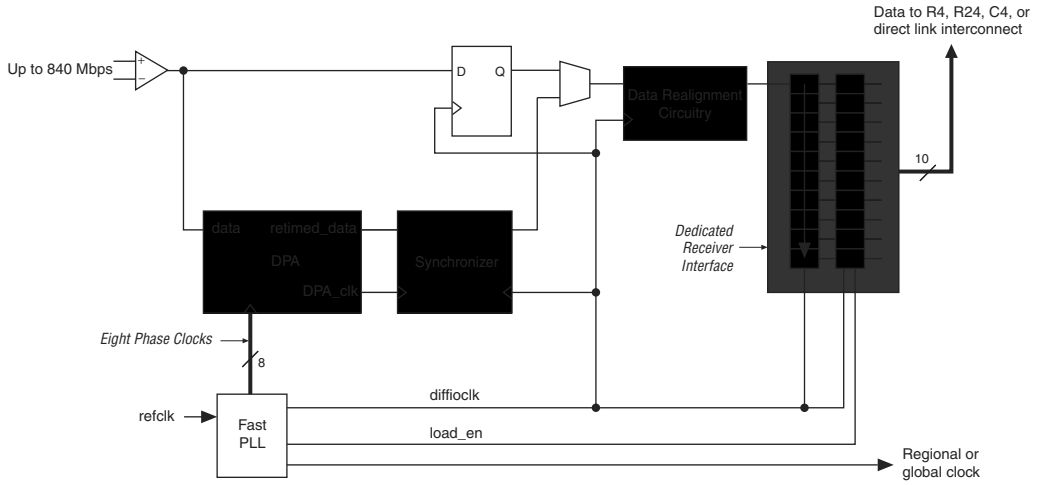
Advanced I/O Standard Support

Arria GX device IOEs support the following I/O standards:

- 3.3-V LVTTL/LVCMOS
- 2.5-V LVTTL/LVCMOS
- 1.8-V LVTTL/LVCMOS
- 1.5-V LVCMOS
- 3.3-V PCI
- 3.3-V PCI-X mode 1
- LVDS
- LVPECL (on input and output clocks only)
- Differential 1.5-V HSTL class I and II
- Differential 1.8-V HSTL class I and II
- Differential SSTL-18 class I and II
- Differential SSTL-2 class I and II
- 1.2-V HSTL class I and II
- 1.5-V HSTL class I and II
- 1.8-V HSTL class I and II
- SSTL-2 class I and II
- SSTL-18 class I and II

Figure 2–80 shows the block diagram of the Arria GX receiver channel.

Figure 2–80. GX Receiver Channel



An external pin or global or regional clock can drive the fast PLLs, which can output up to three clocks: two multiplied high-speed clocks to drive the SERDES block and/or external pin, and a low-speed clock to drive the logic array. In addition, eight phase-shifted clocks from the V_{CO} can feed to the DPA circuitry.

For more information about fast PLL, refer to the *PLLs in Arria GX Devices* chapter.

The eight phase-shifted clocks from the fast PLL feed to the DPA block. The DPA block selects the closest phase to the center of the serial data eye to sample the incoming data. This allows the source-synchronous circuitry to capture incoming data correctly regardless of channel-to-channel or clock-to-channel skew. The DPA block locks to a phase closest to the serial data phase. The phase-aligned DPA clock is used to write the data into the synchronizer.

The synchronizer sits between the DPA block and the data realignment and SERDES circuitry. Because every channel using the DPA block can have a different phase selected to sample the data, the synchronizer is needed to synchronize the data to the high-speed clock domain of the data realignment and the SERDES circuitry.

For high-speed source-synchronous interfaces such as POS-PHY 4 and the Parallel RapidIO standard, the source synchronous clock rate is not a byte- or SERDES-rate multiple of the data rate. Byte alignment is necessary for these protocols because the source synchronous clock does not provide a byte or word boundary as the clock is one half the data rate, not one eighth. The Arria GX device's high-speed differential I/O circuitry provides dedicated data realignment circuitry for user-controlled byte boundary shifting. This simplifies designs while saving ALM resources. You can use an ALM-based state machine to signal the shift of receiver byte boundaries until a specified pattern is detected to indicate byte alignment.

V_{CCSEL} is sampled during power up. Therefore, the V_{CCSEL} setting cannot change on-the-fly or during a reconfiguration. The V_{CCSEL} input buffer is powered by V_{CCINT} and must be hard-wired to V_{CCPD} or ground. A logic high V_{CCSEL} connection selects the 1.8-V/1.5-V input buffer, and a logic low selects the 3.3-V/2.5-V input buffer. V_{CCSEL} should be set to comply with the logic levels driven out of the configuration device or MAX II microprocessor.

If the design must support configuration input voltages of 3.3 V/2.5 V, set V_{CCSEL} to a logic low. You can set the V_{CCIO} voltage of the I/O bank that contains the configuration inputs to any supported voltage. If the design must support configuration input voltages of 1.8 V/1.5 V, set V_{CCSEL} to a logic high and the V_{CCIO} of the bank that contains the configuration inputs to 1.8 V/1.5 V.

For more information about multi-volt support, including information about using TDO and nCEO in multi-volt systems, refer to the *Arria GX Architecture* chapter.

Configuration Schemes

You can load the configuration data for an Arria GX device with one of five configuration schemes (refer to Table 3–4), chosen on the basis of the target application. You can use a configuration device, intelligent controller, or the JTAG port to configure an Arria GX device. A configuration device can automatically configure an Arria GX device at system power up.

You can configure multiple Arria GX devices in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device. Arria GX FPGAs offer the following:

- Configuration data decompression to reduce configuration file storage
- Remote system upgrades for remotely updating Arria GX designs

Table 3–4 lists which configuration features can be used in each configuration scheme.

For more information about configuration schemes in Arria GX devices, refer to the *Configuring Arria GX Devices* chapter.

Table 3–4. Arria GX Configuration Features (Part 1 of 2)

Configuration Scheme	Configuration Method	Decompression	Remote System Upgrade
FPP	MAX II device or microprocessor and flash device	✓ *(1)*	✓
	Enhanced configuration device	✓ *(2)*	✓
AS	Serial configuration device	✓	✓ *(3)*
PS	MAX II device or microprocessor and flash device	✓	✓
	Enhanced configuration device	✓	✓
	Download cable *(4)*	✓	—
PPA	MAX II device or microprocessor and flash device	—	✓

For more information about Arria GX PLLs, refer to the *PLLs in Arria GX Devices* chapter.

Automated Single Event Upset (SEU) Detection

Arria GX devices offer on-chip circuitry for automated checking of single event upset (SEU) detection. Some applications that require the device to operate error free at high elevations or in close proximity to Earth's North or South Pole requires periodic checks to ensure continued data integrity. The error detection cyclic redundancy check (CRC) feature controlled by the **Device and Pin Options** dialog box in the Quartus II software uses a 32-bit CRC circuit to ensure data reliability and is one of the best options for mitigating SEU.

You can implement the error detection CRC feature with existing circuitry in Arria GX devices, eliminating the need for external logic. Arria GX devices compute CRC during configuration. The Arria GX device checks the computed-CRC against an automatically computed CRC during normal operation. The `CRC_ERROR` pin reports a soft error when configuration SRAM data is corrupted, triggering device reconfiguration.

Custom-Built Circuitry

Dedicated circuitry is built into Arria GX devices to automatically perform error detection. This circuitry constantly checks for errors in the configuration SRAM cells while the device is in user mode. You can monitor one external pin for the error and use it to trigger a reconfiguration cycle. You can select the desired time between checks by adjusting a built-in clock divider.

Software Interface

Beginning with version 7.1 of the Quartus II software, you can turn on the automated error detection CRC feature in the **Device and Pin Options** dialog box. This dialog box allows you to enable the feature and set the internal frequency of the CRC between 400 kHz to 50 MHz. This controls the rate that the CRC circuitry verifies the internal configuration SRAM bits in the Arria GX FPGA.

For more information about CRC, refer to *AN 357: Error Detection Using CRC in Altera FPGAs*.

Table 4–7. Arria GX Transceiver Block AC Specification *(Note 1), (2), (3)* (Part 2 of 4)

Description	Condition	–6 Speed Grade Commercial & Industrial	Units
Deterministic jitter at 3.125 Gbps	REFCLK = 156.25 MHz Pattern = CJPAT V_{OD} = 1200 mV No Pre-emphasis	0.17	UI
XAUI Receiver Jitter Tolerance *(4)*			
Total jitter	Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.65	UI
Deterministic jitter	Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.37	UI
Peak-to-peak jitter	Jitter frequency = 22.1 KHz	> 8.5	UI
Peak-to-peak jitter	Jitter frequency = 1.875 MHz	> 0.1	UI
Peak-to-peak jitter	Jitter frequency = 20 MHz	> 0.1	UI
PCI Express (PIPE) Transmitter Jitter Generation *(5)*			
Total Transmitter Jitter Generation	Compliance Pattern; V_{OD} = 800 mV; Pre-emphasis = 49%	< 0.25	UI p-p
PCI Express (PIPE) Receiver Jitter Tolerance *(5)*			
Total Receiver Jitter Tolerance	Compliance Pattern; DC Gain = 3 db	> 0.6	UI p-p
Gigabit Ethernet (GIGE) Transmitter Jitter Generation *(7)*			
Total Transmitter Jitter Generation (TJ)	CRPAT: V_{OD} = 800 mV; Pre-emphasis = 0%	< 0.279	UI p-p
Deterministic Transmitter Jitter Generation (DJ)	CRPAT; V_{OD} = 800 mV; Pre-emphasis = 0%	< 0.14	UI p-p
Gigabit Ethernet (GIGE) Receiver Jitter Tolerance			
Total Jitter Tolerance	CJPAT Compliance Pattern; DC Gain = 0 dB	> 0.66	UI p-p
Deterministic Jitter Tolerance	CJPAT Compliance Pattern; DC Gain = 0 dB	> 0.4	UI p-p
Serial RapidIO (1.25 Gbps, 2.5 Gbps, and 3.125 Gbps) Transmitter Jitter Generation *(6)*			
Total Transmitter Jitter Generation (TJ)	CJPAT Compliance Pattern; V_{OD} = 800 mV; Pre-emphasis = 0%	< 0.35	UI p-p
Deterministic Transmitter Jitter Generation (DJ)	CJPAT Compliance Pattern; V_{OD} = 800 mV; Pre-emphasis = 0%	< 0.17	UI p-p

Table 4–12. Typical Pre-Emphasis (First Post-Tap), *(Note 1)*

V_{cc} HTX = 1.5 V	First Post Tap Pre-Emphasis Level				
V_{OD} Setting (mV)	1	2	3	4	5
1000	—	—	23%	36%	49%
1200	—	—	17%	25%	35%

Note to Table 4–12:

(1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

Table 4–13. Typical Pre-Emphasis (First Post-Tap), *(Note 1)*

V_{cc} HTX = 1.2 V	First Post Tap Pre-Emphasis Level				
V_{OD} Setting (mV)	1	2	3	4	5
	TX Term = 100 Ω				
320	24%	61%	114%	—	—
480	—	31%	55%	86%	121%
640	—	20%	35%	54%	72%
800	—	—	23%	36%	49%
960	—	—	18%	25%	35%

Note to Table 4–13:

(1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

DC Electrical Characteristics

Table 4–14 lists the Arria GX device family DC electrical characteristics.

Table 4–14. Arria GX Device DC Operating Conditions (Part 1 of 2) *(Note 1)*

Symbol	Parameter	Conditions	Device	Min	Typ	Max	Units
I_I	Input pin leakage current	$V_I = V_{CCIOmax}$ to 0 V *(2)*	All	–10	—	10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V *(2)*	All	–10	—	10	µA
I_{CCINT0}	V_{CCINT} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25 °C	EP1AGX20/35	—	0.30	*(3)*	A
			EP1AGX50/60	—	0.50	*(3)*	A
			EP1AGX90	—	0.62	*(3)*	A
I_{CCPD0}	V_{CCPD} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25 °C, V_{CCPD} = 3.3V	EP1AGX20/35	—	2.7	*(3)*	mA
			EP1AGX50/60	—	3.6	*(3)*	mA
			EP1AGX90	—	4.3	*(3)*	mA
I_{CCIO0}	V_{CCIO} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25 °C	EP1AGX20/35	—	4.0	*(3)*	mA
			EP1AGX50/60	—	4.0	*(3)*	mA
			EP1AGX90	—	4.0	*(3)*	mA

Table 4–67. EP1AGX60 Column Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
LVDS	GCLK	t_{SU}	0.980	0.980	2.062	ns
		t_{H}	–0.875	–0.875	–1.785	ns
	GCLK PLL	t_{SU}	2.557	2.557	5.512	ns
		t_{H}	–2.452	–2.452	–5.235	ns

Table 4–68 lists I/O timing specifications.

Table 4–68. EP1AGX60 Row Pins Output Timing Parameters (Part 1 of 2)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	3.052	3.052	7.142	ns
		GCLK PLL	t_{CO}	1.490	1.490	3.719	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.924	2.924	6.502	ns
		GCLK PLL	t_{CO}	1.362	1.362	3.079	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.868	2.868	6.465	ns
		GCLK PLL	t_{CO}	1.306	1.306	3.042	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.924	2.924	6.502	ns
		GCLK PLL	t_{CO}	1.362	1.362	3.079	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.818	2.818	6.196	ns
		GCLK PLL	t_{CO}	1.256	1.256	2.773	ns
2.5 V	4 mA	GCLK	t_{CO}	2.907	2.907	6.476	ns
		GCLK PLL	t_{CO}	1.345	1.345	3.053	ns
2.5 V	8 mA	GCLK	t_{CO}	2.804	2.804	6.218	ns
		GCLK PLL	t_{CO}	1.242	1.242	2.795	ns
2.5 V	12 mA	GCLK	t_{CO}	2.785	2.785	6.104	ns
		GCLK PLL	t_{CO}	1.223	1.223	2.681	ns
1.8 V	2 mA	GCLK	t_{CO}	2.991	2.991	7.521	ns
		GCLK PLL	t_{CO}	1.419	1.419	4.078	ns
1.8 V	4 mA	GCLK	t_{CO}	2.980	2.980	6.742	ns
		GCLK PLL	t_{CO}	1.408	1.408	3.299	ns
1.8 V	6 mA	GCLK	t_{CO}	2.869	2.869	6.441	ns
		GCLK PLL	t_{CO}	1.297	1.297	2.998	ns
1.8 V	8 mA	GCLK	t_{CO}	2.838	2.838	6.327	ns
		GCLK PLL	t_{CO}	1.266	1.266	2.884	ns
1.5 V	2 mA	GCLK	t_{CO}	2.951	2.951	7.020	ns
		GCLK PLL	t_{CO}	1.379	1.379	3.577	ns
1.5 V	4 mA	GCLK	t_{CO}	2.844	2.844	6.419	ns
		GCLK PLL	t_{CO}	1.272	1.272	2.976	ns

Table 4–69. EP1AGX60 Column Pins Output Timing Parameters (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
1.8 V	6 mA	GCLK	t_{CO}	2.822	2.822	6.577	ns
		GCLK PLL	t_{CO}	1.252	1.252	3.142	ns
1.8 V	8 mA	GCLK	t_{CO}	2.824	2.824	6.486	ns
		GCLK PLL	t_{CO}	1.254	1.254	3.051	ns
1.8 V	10 mA	GCLK	t_{CO}	2.778	2.778	6.409	ns
		GCLK PLL	t_{CO}	1.208	1.208	2.974	ns
1.8 V	12 mA	GCLK	t_{CO}	2.779	2.779	6.352	ns
		GCLK PLL	t_{CO}	1.209	1.209	2.917	ns
1.5 V	2 mA	GCLK	t_{CO}	2.873	2.873	7.145	ns
		GCLK PLL	t_{CO}	1.303	1.303	3.710	ns
1.5 V	4 mA	GCLK	t_{CO}	2.809	2.809	6.576	ns
		GCLK PLL	t_{CO}	1.239	1.239	3.141	ns
1.5 V	6 mA	GCLK	t_{CO}	2.812	2.812	6.458	ns
		GCLK PLL	t_{CO}	1.242	1.242	3.023	ns
1.5 V	8 mA	GCLK	t_{CO}	2.771	2.771	6.405	ns
		GCLK PLL	t_{CO}	1.201	1.201	2.970	ns
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.757	2.757	6.184	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.744	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.740	2.740	6.134	ns
		GCLK PLL	t_{CO}	1.167	1.167	2.694	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.718	2.718	6.061	ns
		GCLK PLL	t_{CO}	1.145	1.145	2.621	ns
SSTL-2 CLASS II	20 mA	GCLK	t_{CO}	2.719	2.719	6.048	ns
		GCLK PLL	t_{CO}	1.146	1.146	2.608	ns
SSTL-2 CLASS II	24 mA	GCLK	t_{CO}	2.715	2.715	6.046	ns
		GCLK PLL	t_{CO}	1.142	1.142	2.606	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.753	2.753	6.155	ns
		GCLK PLL	t_{CO}	1.183	1.183	2.720	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.758	2.758	6.116	ns
		GCLK PLL	t_{CO}	1.185	1.185	2.676	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.737	2.737	6.097	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.657	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.742	2.742	6.095	ns
		GCLK PLL	t_{CO}	1.169	1.169	2.655	ns
SSTL-18 CLASS I	12 mA	GCLK	t_{CO}	2.736	2.736	6.081	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.641	ns
SSTL-18 CLASS II	8 mA	GCLK	t_{CO}	2.725	2.725	6.047	ns
		GCLK PLL	t_{CO}	1.152	1.152	2.607	ns

Table 4–74. EP1AGX90 Row Pins Output Timing Parameters (Part 3 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.857	2.857	6.106	ns
		GCLK PLL	t_{CO}	0.779	0.779	1.950	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.842	2.842	6.098	ns
		GCLK PLL	t_{CO}	0.764	0.764	1.942	ns
LVDS	—	GCLK	t_{CO}	2.898	2.898	6.265	ns
		GCLK PLL	t_{CO}	0.831	0.831	2.129	ns

Table 4–75 lists I/O timing specifications.

Table 4–75. EP1AGX90 Column Pins Output Timing Parameters (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	3.141	3.141	7.164	ns
		GCLK PLL	t_{CO}	1.077	1.077	3.029	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.996	2.996	6.792	ns
		GCLK PLL	t_{CO}	0.932	0.932	2.657	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.929	2.929	6.792	ns
		GCLK PLL	t_{CO}	0.865	0.865	2.657	ns
3.3-V LVTTL	16 mA	GCLK	t_{CO}	2.903	2.903	6.623	ns
		GCLK PLL	t_{CO}	0.839	0.839	2.488	ns
3.3-V LVTTL	20 mA	GCLK	t_{CO}	2.881	2.881	6.498	ns
		GCLK PLL	t_{CO}	0.817	0.817	2.363	ns
3.3-V LVTTL	24 mA	GCLK	t_{CO}	2.874	2.874	6.500	ns
		GCLK PLL	t_{CO}	0.810	0.810	2.365	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.996	2.996	6.792	ns
		GCLK PLL	t_{CO}	0.932	0.932	2.657	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.904	2.904	6.497	ns
		GCLK PLL	t_{CO}	0.840	0.840	2.362	ns
3.3-V LVCMOS	12 mA	GCLK	t_{CO}	2.876	2.876	6.419	ns
		GCLK PLL	t_{CO}	0.812	0.812	2.284	ns
3.3-V LVCMOS	16 mA	GCLK	t_{CO}	2.883	2.883	6.387	ns
		GCLK PLL	t_{CO}	0.819	0.819	2.252	ns
3.3-V LVCMOS	20 mA	GCLK	t_{CO}	2.870	2.870	6.369	ns
		GCLK PLL	t_{CO}	0.806	0.806	2.234	ns
3.3-V LVCMOS	24 mA	GCLK	t_{CO}	2.859	2.859	6.347	ns
		GCLK PLL	t_{CO}	0.795	0.795	2.212	ns
2.5 V	4 mA	GCLK	t_{CO}	2.958	2.958	6.824	ns
		GCLK PLL	t_{CO}	0.894	0.894	2.689	ns

Table 4–107. Arria GX Maximum Output Clock Rate for Dedicated Clock Pins (Part 4 of 4)

I/O Standards	Drive Strength	–6 Speed Grade	Units
1.5 V	SERIES_50_OHMS	373	MHz
SSTL-2 CLASS I	SERIES_50_OHMS	467	MHz
SSTL-2 CLASS II	SERIES_25_OHMS	467	MHz
SSTL-18 CLASS I	SERIES_50_OHMS	327	MHz
SSTL-18 CLASS II	SERIES_25_OHMS	420	MHz
1.8-V HSTL CLASS I	SERIES_50_OHMS	561	MHz
1.8-V HSTL CLASS II	SERIES_25_OHMS	420	MHz
1.5-V HSTL CLASS I	SERIES_50_OHMS	467	MHz
1.2-V HSTL	SERIES_50_OHMS	233	MHz
DIFFERENTIAL SSTL-2	SERIES_50_OHMS	467	MHz
DIFFERENTIAL 2.5-V SSTL CLASS II	SERIES_25_OHMS	467	MHz
DIFFERENTIAL 1.8-V SSTL CLASS I	SERIES_50_OHMS	327	MHz
DIFFERENTIAL 1.8-V SSTL CLASS II	SERIES_25_OHMS	420	MHz
DIFFERENTIAL 1.8-V HSTL CLASS I	SERIES_50_OHMS	561	MHz
DIFFERENTIAL 1.8-V HSTL CLASS II	SERIES_25_OHMS	420	MHz
DIFFERENTIAL 1.5-V HSTL CLASS I	SERIES_50_OHMS	467	MHz
DIFFERENTIAL 1.2-V HSTL	SERIES_50_OHMS	233	MHz

Duty Cycle Distortion

Duty cycle distortion (DCD) describes how much the falling edge of a clock is off from its ideal position. The ideal position is when both the clock high time (CLKH) and the clock low time (CLKL) equal half of the clock period (T), as shown in Figure 4–10. DCD is the deviation of the non-ideal falling edge from the ideal falling edge, such as D1 for the falling edge A and D2 for the falling edge B (refer to Figure 4–10). The maximum DCD for a clock is the larger value of D1 and D2.

Table 4–115. High-Speed I/O Specifications (Part 2 of 2) *Note (1), (2)*

Symbol	Conditions			–6 Speed Grade			Units
				Min	Typ	Max	
DPA lock time	Standard	Training Pattern	Transition Density		—	—	Number of repetitions
	SPI-4	000000000011 11111111	10%	256	—	—	
	Parallel Rapid I/O	00001111	25%	256	—	—	
		10010000	50%	256	—	—	
	Miscellaneous	10101010	100%	256	—	—	
		01010101	—	256	—	—	

Notes to Table 4–115:

(1) When J = 4 to 10, the SERDES block is used.

(2) When J = 1 or 2, the SERDES block is bypassed.

(3) The input clock frequency and the W factor must satisfy the following fast PLL VCO specification: 150 ≤ input clock frequency × W ≤ 1,040.

(4) The minimum specification is dependent on the clock source (fast PLL, enhanced PLL, clock pin, and so on) and the clock routing resource (global, regional, or local) used. The I/O differential buffer and input register do not have a minimum toggle rate.

About this Handbook

This handbook provides comprehensive information about the Altera® Arria® GX family of devices.

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Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicates command names and dialog box titles. For example, **Save As** dialog box.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, dialog box options, software utility names, and other GUI labels. For example, **\qdesigns** directory, **d:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicates document titles. For example, *AN 519: Stratix IV Design Guidelines*.
Italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>***.pof** file.
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