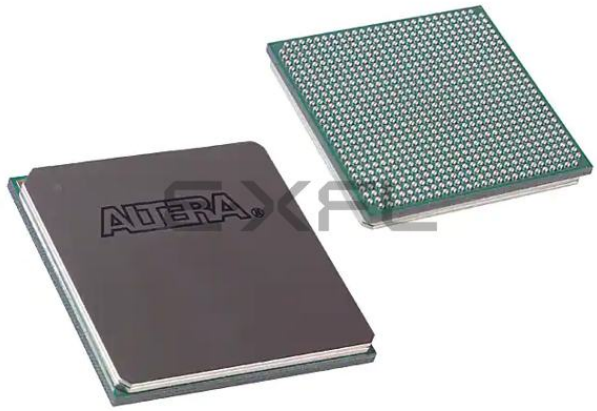


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1079
Number of Logic Elements/Cells	21580
Total RAM Bits	1229184
Number of I/O	341
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	780-BBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1agx20cf780i6

1. Arria GX Device Family Overview

AGX51001-2.0

Introduction

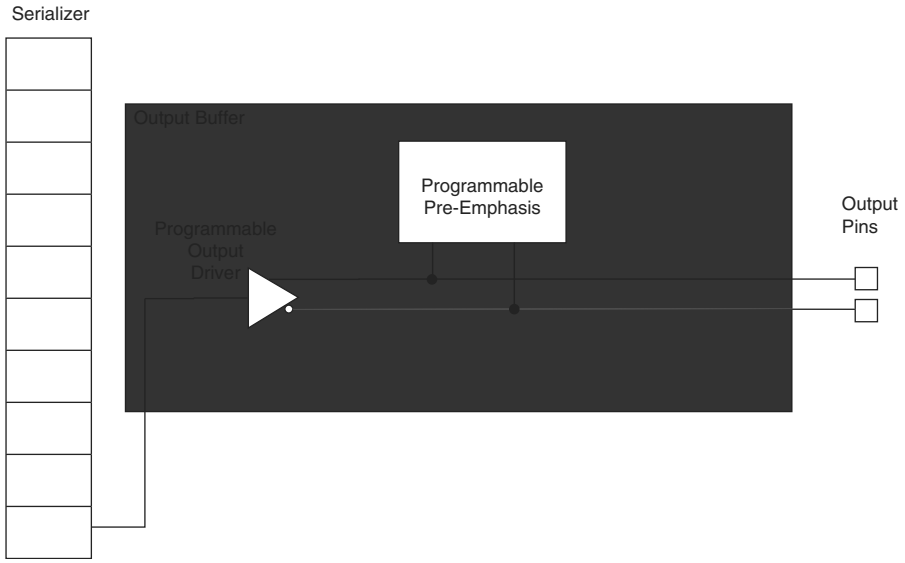
The Arria® GX family of devices combines 3.125 Gbps serial transceivers with reliable packaging technology and a proven logic array. Arria GX devices include 4 to 12 high-speed transceiver channels, each incorporating clock data recovery (CDR) technology and embedded SERDES circuitry designed to support PCI-Express, Gigabit Ethernet, SDI, SerialLite II, XAUI, and Serial RapidIO protocols, along with the ability to develop proprietary, serial-based IP using its Basic mode. The transceivers build upon the success of the Stratix® II GX family. The Arria GX FPGA technology offers a 1.2-V logic array with the right level of performance and dependability needed to support these mainstream protocols.

Features

The key features of Arria GX devices include:

- Transceiver block features
  - High-speed serial transceiver channels with CDR support up to 3.125 Gbps.
  - Devices available with 4, 8, or 12 high-speed full-duplex serial transceiver channels
  - Support for the following CDR-based bus standards—PCI Express, Gigabit Ethernet, SDI, SerialLite II, XAUI, and Serial RapidIO, along with the ability to develop proprietary, serial-based IP using its Basic mode
  - Individual transmitter and receiver channel power-down capability for reduced power consumption during non-operation
  - 1.2- and 1.5-V pseudo current mode logic (PCML) support on transmitter output buffers
  - Receiver indicator for loss of signal (available only in PCI Express [PIPE] mode)
  - Hot socketing feature for hot plug-in or hot swap and power sequencing support without the use of external devices
  - Dedicated circuitry that is compliant with PIPE, XAUI, Gigabit Ethernet, Serial Digital Interface (SDI), and Serial RapidIO
  - 8B/10B encoder/decoder performs 8-bit to 10-bit encoding and 10-bit to 8-bit decoding
  - Phase compensation FIFO buffer performs clock domain translation between the transceiver block and the logic array
  - Channel aligner compliant with XAUI

Figure 2–8. Output Buffer



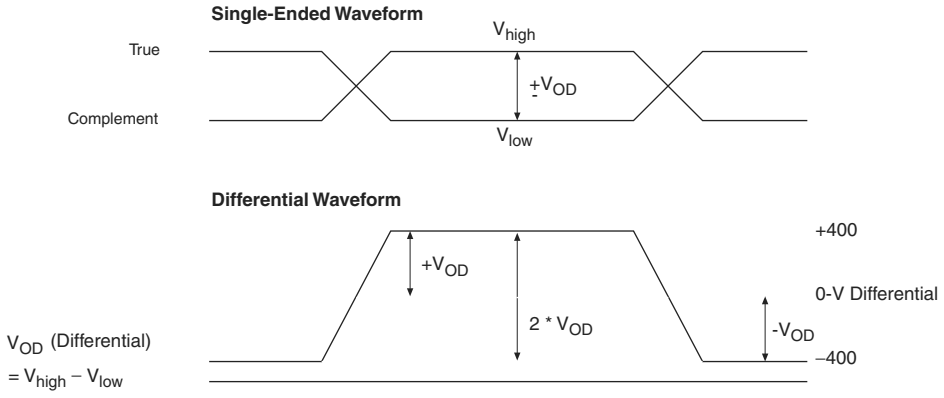
Programmable Output Driver

The programmable output driver can be set to drive out differentially from 400 to 1200 mV. The differential output voltage (V_{OD}) can be statically set by using the ALTGXB megafunction.

You can configure the output driver with 100-Ω OCT or external OCT.

Differential signaling conventions are shown in Figure 2–9. The differential amplitude represents the value of the voltage between the true and complement signals. Peak-to-peak differential voltage is defined as 2 (V_{HIGH} – V_{LOW}) = 2 single-ended voltage swing. The common mode voltage is the average of V_{HIGH} and V_{LOW}.

Figure 2–9. Differential Signaling



Bit-Slip Mode

The word aligner can operate in either pattern detection mode or in bit-slip mode.

The bit-slip mode provides the option to manually shift the word boundary through the FPGA. This feature is useful for:

- Longer synchronization patterns than the pattern detector can accommodate
- Scrambled data stream
- Input stream consisting of over-sampled data

The word aligner outputs a word boundary as it is received from the analog receiver after reset. You can examine the word and search its boundary in the FPGA. To do so, assert the `rx_bitslip` signal. The `rx_bitslip` signal should be toggled and held constant for at least two FPGA clock cycles.

For every rising edge of the `rx_bitslip` signal, the current word boundary is slipped by one bit. Every time a bit is slipped, the bit received earliest is lost. If bit slipping shifts a complete round of bus width, the word boundary is back to the original boundary.

The `rx_syncstatus` signal is not available in bit-slipping mode.

Channel Aligner

The channel aligner is available only in XAUI mode and aligns the signals of all four channels within a transceiver. The channel aligner follows the IEEE 802.3ae, clause 48 specification for channel bonding.

The channel aligner is a 16-word FIFO buffer with a state machine controlling the channel bonding process. The state machine looks for an /A/ (/K28.3/) in each channel and aligns all the /A/ code groups in the transceiver. When four columns of /A/ (denoted by //A//) are detected, the `rx_channelaligned` signal goes high, signifying that all the channels in the transceiver have been aligned. The reception of four consecutive misaligned /A/ code groups restarts the channel alignment sequence and sends the `rx_channelaligned` signal low.

XAUI Mode

In XAUI mode, the rate matcher adheres to clause 48 of the IEEE 802.3ae specification for clock rate compensation. The rate matcher performs clock compensation on columns of /R/ (/K28.0/), denoted by //R//. An //R// is added or deleted automatically based on the number of words in the FIFO buffer.

PCI Express (PIPE) Mode Rate Matcher

In PCI Express (PIPE) mode, the rate matcher can compensate up to ± 300 PPM (600 PPM total) frequency difference between the upstream transmitter and the receiver. The rate matcher logic looks for skip ordered sets (SOS), which contains a /K28.5/ comma followed by three /K28.0/ skip characters. The rate matcher logic deletes or inserts /K28.0/ skip characters as necessary from/to the rate matcher FIFO.

The rate matcher in PCI Express (PIPE) mode has a FIFO buffer overflow and underflow protection. In the event of a FIFO buffer overflow, the rate matcher deletes any data after detecting the overflow condition to prevent FIFO pointer corruption until the rate matcher is not full. In an underflow condition, the rate matcher inserts 9'h1FE (/K30.7/) until the FIFO buffer is not empty. These measures ensure that the FIFO buffer can gracefully exit the overflow and underflow condition without requiring a FIFO reset. The rate matcher FIFO overflow and underflow condition is indicated on the `pipestatus` port.

You can bypass the rate matcher in PCI Express (PIPE) mode if you have a synchronous system where the upstream transmitter and local receiver derive their reference clocks from the same source.

GIGE Mode Rate Matcher

In GIGE mode, the rate matcher can compensate up to ± 100 PPM (200 PPM total) frequency difference between the upstream transmitter and the receiver. The rate matcher logic inserts or deletes /I2/ idle ordered sets to/from the rate matcher FIFO during the inter-frame or inter-packet gap (IFG or IPG). /I2/ is selected as the rate matching ordered set because it maintains the running disparity, unlike /I1/ that alters the running disparity. Because the /I2/ ordered-set contains two 10-bit code groups (/K28.5/, /D16.2/), 20 bits are inserted or deleted at a time for rate matching.

The rate matcher logic has the capability to insert or delete /C1/ or /C2/ configuration ordered sets when 'GIGE Enhanced' mode is chosen as the sub-protocol in the MegaWizard Plug-In Manager.

If the frequency PPM difference between the upstream transmitter and the local receiver is high, or if the packet size is too large, the rate matcher FIFO buffer can face an overflow or underflow situation.

Basic Mode

In basic mode, you can program the skip and control pattern for rate matching. There is no restriction on the deletion of a skip character in a cluster. The rate matcher deletes the skip characters as long as they are available. For insertion, the rate matcher inserts skip characters such that the number of skip characters at the output of rate matcher does not exceed five.

Table 2–6 lists the reset signals available in Arria GX devices and the transceiver circuitry affected by each signal.

Table 2–6. Reset Signal Map to Arria GX Blocks

Reset Signal	Transmitter Phase Compensation FIFO Module/ Byte Serializer	Transmitter 8B/10B Encoder	Transmitter Serializer	Transmitter Analog Circuits	Transmitter PLL	Transmitter XAUI State Machine	BIST Generators	Receiver Deserializer	Receiver Word Aligner	Receiver Deskew FIFO Module	Receiver Rate Matcher	Receiver 8B/10B Decoder	Receiver Phase Comp FIFO Module/ Byte Deserializer	Receiver PLL / CRU	Receiver XAUI State Machine	BIST Verifiers	Receiver Analog Circuits
rx_digitalreset	—	—	—	—	—	—	—	—	✓	—	✓	✓	✓	—	✓	✓	—
rx_analogreset	—	—	—	—	—	—	—	✓	—	—	—	—	—	✓	—	—	✓
tx_digitalreset	✓	✓	—	—	—	✓	✓	—	—	—	—	—	—	—	—	—	—
gxb_powerdown	✓	✓	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓	✓	✓	✓
gxb_enable	✓	✓	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓	✓	✓	✓

Calibration Block

Arria GX devices use the calibration block to calibrate OCT for the PLLs, and their associated output buffers, and the terminating resistors on the transceivers. The calibration block counters the effects of process, voltage, and temperature (PVT). The calibration block references a derived voltage across an external reference resistor to calibrate the OCT resistors on Arria GX devices. You can power down the calibration block. However, powering down the calibration block during operations can yield transmit and receive data errors.

Transceiver Clocking

This section describes the clock distribution in an Arria GX transceiver channel and the PLD clock resource utilization by the transceiver blocks.

Transceiver Channel Clock Distribution

Each transceiver block has one transmitter PLL and four receiver PLLs.

The transmitter PLL multiplies the input reference clock to generate a high-speed serial clock at a frequency that is half the data rate of the configured functional mode. This high-speed serial clock (or its divide-by-two version if the functional mode uses byte serializer) is fed to the CMU clock divider block. Depending on the configured functional mode, the CMU clock divider block divides the high-speed serial clock to generate the low-speed parallel clock that clocks the transceiver PCS logic in the associated channel. The low-speed parallel clock is also forwarded to the PLD logic array on the `tx_clkout` or `coreclkout` ports.

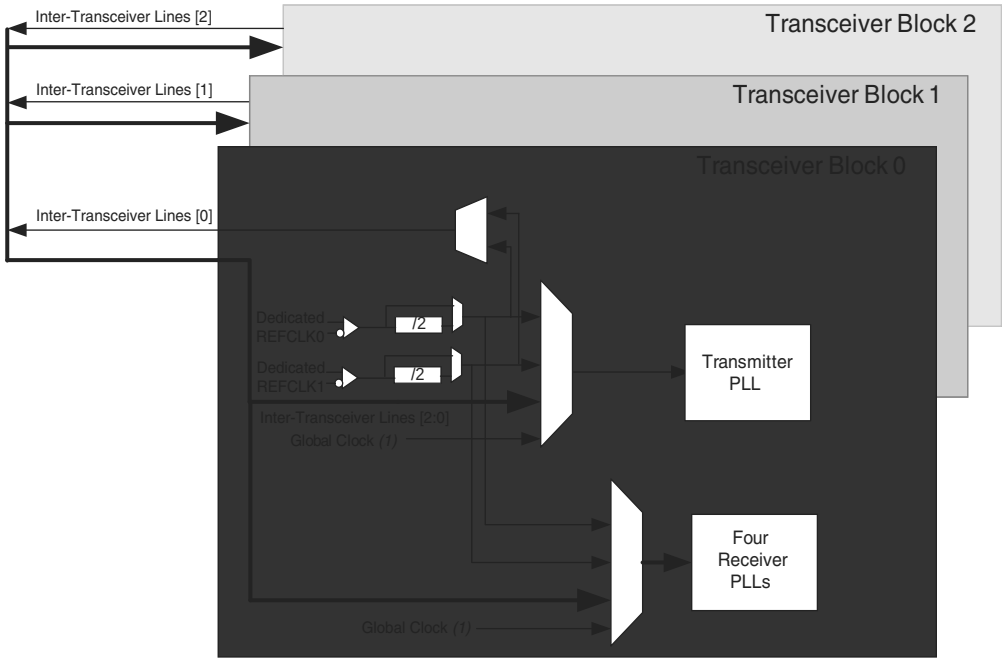
The receiver PLL in each channel is also fed by an input reference clock. The receiver PLL along with the clock recovery unit generates a high-speed serial recovered clock and a low-speed parallel recovered clock. The low-speed parallel recovered clock feeds the receiver PCS logic until the rate matcher. The CMU low-speed parallel clock clocks the rest of the logic from the rate matcher until the receiver phase compensation FIFO. In modes that do not use a rate matcher, the receiver PCS logic is clocked by the recovered clock until the receiver phase compensation FIFO.

The input reference clock to the transmitter and receiver PLLs can be derived from:

- One of two available dedicated reference clock input pins (`REFCLK0` or `REFCLK1`) of the associated transceiver block
- PLD clock network (must be driven directly from an input clock pin and cannot be driven by user logic or enhanced PLL)
- Inter-transceiver block lines driven by reference clock input pins of other transceiver blocks

Figure 2–22 shows the input reference clock sources for the transmitter and receiver PLL.

Figure 2–22. Input Reference Clock Sources



For more information about transceiver clocking in all supported functional modes, refer to the *Arria GX Transceiver Architecture* chapter.

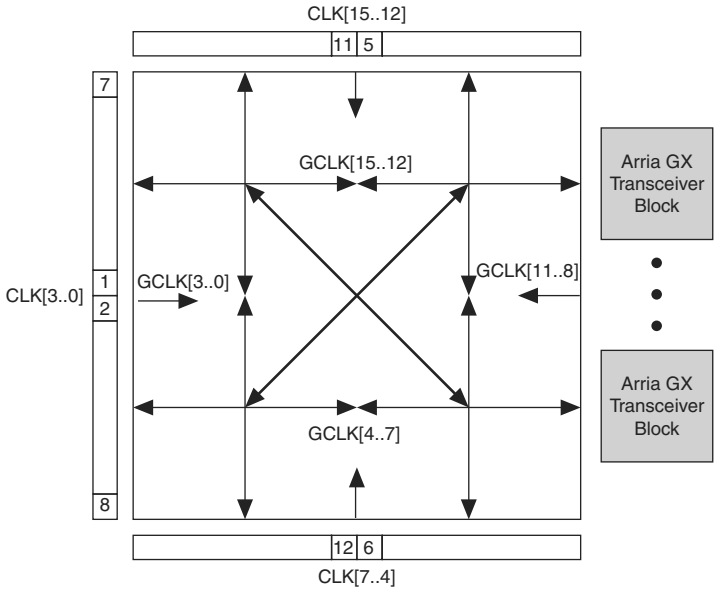
PLD Clock Utilization by Transceiver Blocks

Arria GX devices have up to 16 global clock (GCLK) lines and 16 regional clock (RCLK) lines that are used to route the transceiver clocks. The following transceiver clocks use the available global and regional clock resources:

- `pll_inclk` (if driven from an FPGA input pin)
- `rx_cruclk` (if driven from an FPGA input pin)
- `tx_clkout/coreclkout` (CMU low-speed parallel clock forwarded to the PLD)
- Recovered clock from each channel (`rx_clkout`) in non-rate matcher mode
- Calibration clock (`cal_blk_clk`)
- Fixed clock (`fixedclk` used for receiver detect circuitry in PCI Express [PIPE] mode only)

Figure 2–23 and Figure 2–24 show the available GCLK and RCLK resources in Arria GX devices.

Figure 2–23. Global Clock Resources in Arria GX Devices



As indicated, the Arria GX DSP block can support one 36 × 36-bit multiplier in a single DSP block and is true for any combination of signed, unsigned, or mixed sign multiplications.

Figure 2–50 shows one of the columns with surrounding LAB rows.

Figure 2–50. DSP Blocks Arranged in Columns

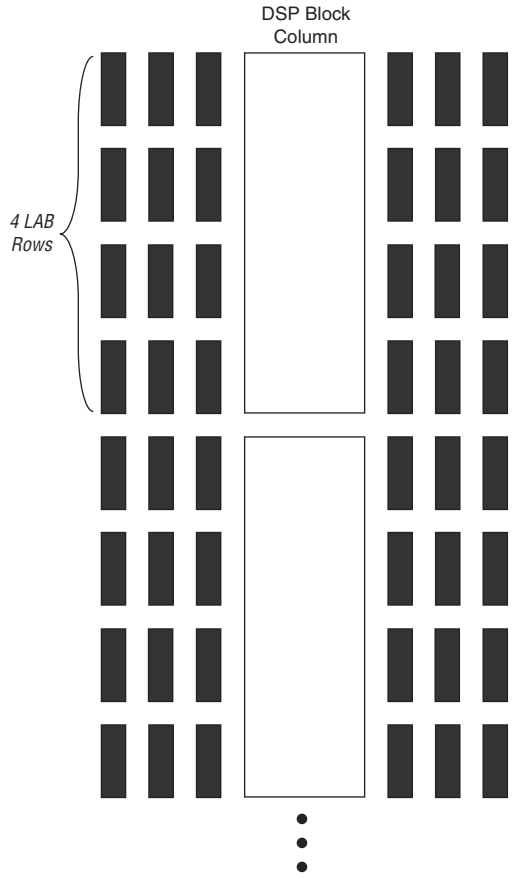
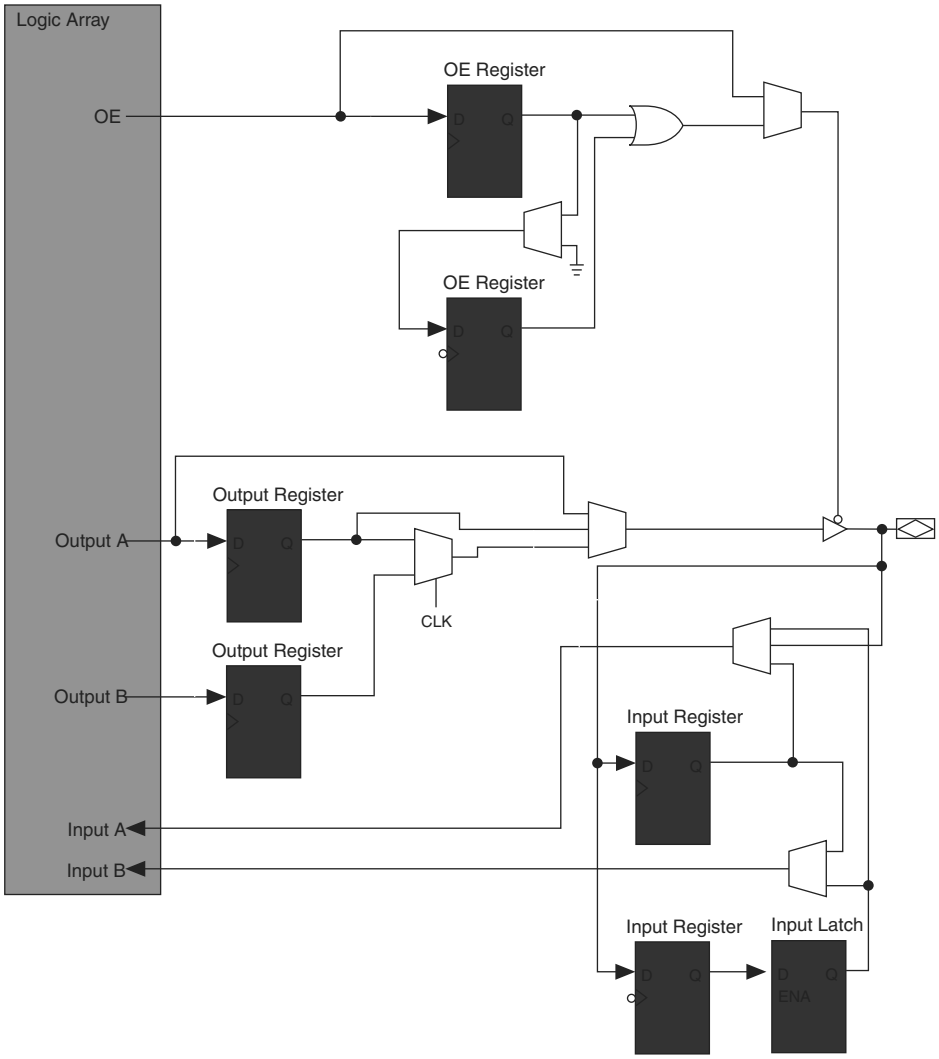


Table 2–13 lists the number of DSP blocks in each Arria GX device. DSP block multipliers can optionally feed an adder/subtractor or accumulator in the block depending on the configuration, which makes routing to ALMs easier, saves ALM routing resources, and increases performance because all connections and blocks are in the DSP block.

The IOE in Arria GX devices contains a bidirectional I/O buffer, six registers, and a latch for a complete embedded bidirectional single data rate or DDR transfer. Figure 2–67 shows the Arria GX IOE structure. The IOE contains two input registers (plus a latch), two output registers, and two output enable registers. The design can use both input registers and the latch to capture DDR input and both output registers to drive DDR outputs. Additionally, the design can use the output enable (OE) register for fast clock-to-output enable timing. The negative edge-clocked OE register is used for DDR SDRAM interfacing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins.

Figure 2–67. Arria GX IOE Structure



The IOEs are located in I/O blocks around the periphery of the Arria GX device. There are up to four IOEs per row I/O block and four IOEs per column I/O block. Row I/O blocks drive row, column, or direct link interconnects. Column I/O blocks drive column interconnects.

Configuring Arria GX FPGAs with JRunner

The JRunner software driver configures Altera FPGAs, including Arria GX FPGAs, through the ByteBlaster™ II or ByteBlasterMV cables in JTAG mode. The programming input file supported is in Raw Binary File (**.rbf**) format. JRunner also requires a Chain Description File (**.cdf**) generated by the Quartus II software. JRunner is targeted for embedded JTAG configuration. The source code is developed for the Windows NT operating system (OS), but can be customized to run on other platforms.

For more information about the JRunner software driver, refer to the *AN414: JRunner Software Driver: An Embedded Solution for PLD JTAG Configuration* and the source files on the Altera website.

Programming Serial Configuration Devices with SRunner

You can program a serial configuration device in-system by an external microprocessor using SRunner™. SRunner is a software driver developed for embedded serial configuration device programming that can be easily customized to fit into different embedded systems. SRunner software driver reads a raw programming data file (**.rpd**) and writes to serial configuration devices. The serial configuration device programming time using SRunner software driver is comparable to the programming time when using the Quartus II software.

For more information about SRunner, refer to the *AN418: SRunner: An Embedded Solution for Serial Configuration Device Programming* and the source code on the Altera website.

For more information about programming serial configuration devices, refer to the *Serial Configuration Devices (EPCS1, EPCS4, EPCS64, and EPCS128) Data Sheet* in the *Configuration Handbook*.

Configuring Arria GX FPGAs with the MicroBlaster Driver

The MicroBlaster™ software driver supports a raw binary file (RBF) programming input file and is ideal for embedded FPP or PS configuration. The source code is developed for the Windows NT operating system, although it can be customized to run on other operating systems.

For more information about the MicroBlaster software driver, refer to the *Configuring the MicroBlaster Fast Passive Parallel Software Driver White Paper* or the *AN423: Configuring the MicroBlaster Passive Serial Software Driver*.

PLL Reconfiguration

The phase-locked loops (PLLs) in the Arria GX device family support reconfiguration of their multiply, divide, VCO-phase selection, and bandwidth selection settings without reconfiguring the entire device. You can use either serial data from the logic array or regular I/O pins to program the PLL's counter settings in a serial chain. This option provides considerable flexibility for frequency synthesis, allowing real-time variation of the PLL frequency and delay. The rest of the device is functional while reconfiguring the PLL.

Table 4–6. Arria GX Transceiver Block AC Specification (Part 1 of 3)

Symbol / Description	Conditions	–6 Speed Grade Commercial and Industrial			Units
		Min	Typ	Max	
Reference clock					
Input reference clock frequency	—	50	—	622.08	MHz
Absolute V_{MAX} for a REFCLK Pin	—	—	—	3.3	V
Absolute V_{MIN} for a REFCLK Pin	—	–0.3	—	—	V
Rise/Fall time	—	—	0.2	—	UI
Duty cycle	—	45	—	55	%
Peak to peak differential input voltage V_{ID} (diff p-p)	—	200	—	2000	mV
Spread spectrum clocking *(1)*	0 to –0.5%	30	—	33	kHz
On-chip termination resistors	—		115 ± 20%		Ω
V_{ICM} (AC coupled)	—		1200 ± 5%		mV
V_{ICM} (DC coupled) *(2)*	PCI Express (PIPE) mode	0.25	—	0.55	V
RREFB	—		2000 +/-1%		Ω
Transceiver Clocks					
Calibration block clock frequency	—	10	—	125	MHz
Calibration block minimum power-down pulse width	—	30	—	—	ns
fixedclk clock frequency *(3)*	—		125 ±10%		MHz
reconfig clock frequency	SDI mode	2.5	—	50	MHz
Transceiver block minimum power-down pulse width	—	100	—	—	ns
Receiver					
Data rate	—	600	—	3125	Mbps
Absolute V_{MAX} for a receiver pin *(4)*	—	—	—	2.0	V
Absolute V_{MIN} for a receiver pin	—	–0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p)	Vicm = 0.85 V	—	—	3.3	V
Minimum peak-to-peak differential input voltage V_{ID} (diff p-p)	DC Gain = 3 dB	160	—	—	mV
On-chip termination resistors	—		100±15%		Ω
V_{ICM} *(15)*	Vicm = 0.85 V setting	850 ± 10%	850 ± 10%	850 ± 10%	mV
	Vicm = 1.2 V setting	1200 ± 10%	1200 ± 10%	1200 ± 10%	mV
Bandwidth at 3.125 Gbps	BW = Low	—	30	—	MHz
	BW = Med	—	40	—	
	BW = High	—	50	—	

Table 4–7. Arria GX Transceiver Block AC Specification *(Note 1), (2), (3)* (Part 3 of 4)

Description	Condition	–6 Speed Grade Commercial & Industrial	Units
Serial RapidIO (1.25 Gbps, 2.5 Gbps, and 3.125 Gbps) Receiver Jitter Tolerance *(6)*			
Total Jitter Tolerance	CJPAT Compliance Pattern; DC Gain = 0 dB	> 0.65	UI p-p
Combined Deterministic and Random Jitter Tolerance (J_{DR})	CJPAT Compliance Pattern; DC Gain = 0 dB	> 0.55	UI p-p
Deterministic Jitter Tolerance (J_D)	CJPAT Compliance Pattern; DC Gain = 0 dB	> 0.37	UI p-p
Sinusoidal Jitter Tolerance	Jitter Frequency = 22.1 KHz	> 8.5	UI p-p
	Jitter Frequency = 200 KHz	> 1.0	UI p-p
	Jitter Frequency = 1.875 MHz	> 0.1	UI p-p
	Jitter Frequency = 20 MHz	> 0.1	UI p-p
SDI Transmitter Jitter Generation *(8)*			
Alignment Jitter (peak-to-peak)	Data Rate = 1.485 Gbps (HD) REFCLK = 74.25 MHz Pattern = Color Bar Vod = 800 mV No Pre-emphasis Low-Frequency Roll-Off = 100 KHz	0.2	UIv
	Data Rate = 2.97 Gbps (3G) REFCLK = 148.5 MHz Pattern = Color Bar Vod = 800 mV No Pre-emphasis Low-Frequency Roll-Off = 100 KHz	0.3	UI

Figure 4–5. Receiver Input Waveforms for Differential I/O Standards

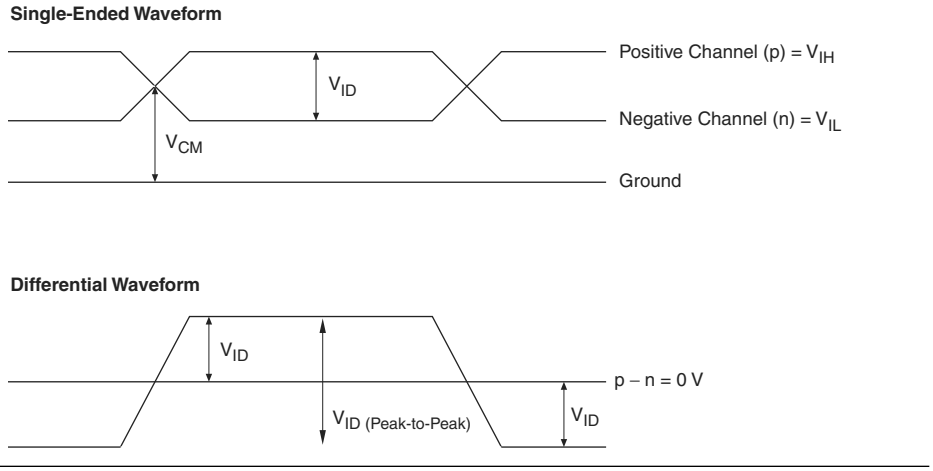


Figure 4–6. Transmitter Output Waveforms for Differential I/O Standards

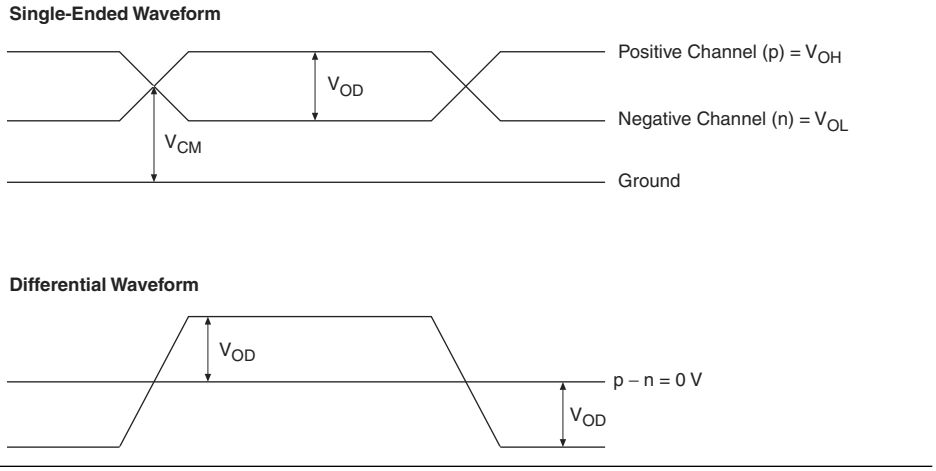


Table 4–20. 2.5-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage for left and right I/O banks (1, 2, 5, and 6)	—	2.375	2.5	2.625	V
V_{ID}	Input differential voltage swing (single-ended)	—	100	350	900	mV
V_{ICM}	Input common mode voltage	—	200	1,250	1,800	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	250	—	450	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	1.125	—	1.375	V
R_L	Receiver differential input discrete resistor (external to Arria GX devices)	—	90	100	110	Ω

Table 4–50. EP1AGX20 Row Pins output Timing Parameters (Part 2 of 2)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.626	2.626	5.614	ns
		GCLK PLL	t_{CO}	1.207	1.207	2.542	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.602	2.602	5.538	ns
		GCLK PLL	t_{CO}	1.183	1.183	2.466	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.568	2.568	5.407	ns
		GCLK PLL	t_{CO}	1.149	1.149	2.335	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.614	2.614	5.556	ns
		GCLK PLL	t_{CO}	1.195	1.195	2.484	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.618	2.618	5.485	ns
		GCLK PLL	t_{CO}	1.199	1.199	2.413	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.594	2.594	5.468	ns
		GCLK PLL	t_{CO}	1.175	1.175	2.396	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.597	2.597	5.447	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.375	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.595	2.595	5.466	ns
		GCLK PLL	t_{CO}	1.176	1.176	2.394	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.598	2.598	5.430	ns
		GCLK PLL	t_{CO}	1.179	1.179	2.358	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.580	2.580	5.426	ns
		GCLK PLL	t_{CO}	1.161	1.161	2.354	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.584	2.584	5.415	ns
		GCLK PLL	t_{CO}	1.165	1.165	2.343	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.575	2.575	5.414	ns
		GCLK PLL	t_{CO}	1.156	1.156	2.342	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.594	2.594	5.443	ns
		GCLK PLL	t_{CO}	1.175	1.175	2.371	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.597	2.597	5.429	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.357	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.582	2.582	5.421	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.349	ns
LVDS	—	GCLK	t_{CO}	2.654	2.654	5.613	ns
		GCLK PLL	t_{CO}	1.226	1.226	2.530	ns

Table 4–55. EP1AGX35 Column Pins Input Timing Parameters (Part 2 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
2.5 V	GCLK	t_{SU}	1.261	1.261	2.897	ns
		t_H	–1.156	–1.156	–2.620	ns
	GCLK PLL	t_{SU}	2.703	2.703	6.003	ns
		t_H	–2.598	–2.598	–5.726	ns
1.8 V	GCLK	t_{SU}	1.327	1.327	3.107	ns
		t_H	–1.222	–1.222	–2.830	ns
	GCLK PLL	t_{SU}	2.769	2.769	6.213	ns
		t_H	–2.664	–2.664	–5.936	ns
1.5 V	GCLK	t_{SU}	1.330	1.330	3.200	ns
		t_H	–1.225	–1.225	–2.923	ns
	GCLK PLL	t_{SU}	2.772	2.772	6.306	ns
		t_H	–2.667	–2.667	–6.029	ns
SSTL-2 CLASS I	GCLK	t_{SU}	1.075	1.075	2.372	ns
		t_H	–0.970	–0.970	–2.095	ns
	GCLK PLL	t_{SU}	2.517	2.517	5.480	ns
		t_H	–2.412	–2.412	–5.203	ns
SSTL-2 CLASS II	GCLK	t_{SU}	1.075	1.075	2.372	ns
		t_H	–0.970	–0.970	–2.095	ns
	GCLK PLL	t_{SU}	2.517	2.517	5.480	ns
		t_H	–2.412	–2.412	–5.203	ns
SSTL-18 CLASS I	GCLK	t_{SU}	1.113	1.113	2.479	ns
		t_H	–1.008	–1.008	–2.202	ns
	GCLK PLL	t_{SU}	2.555	2.555	5.585	ns
		t_H	–2.450	–2.450	–5.308	ns
SSTL-18 CLASS II	GCLK	t_{SU}	1.114	1.114	2.479	ns
		t_H	–1.009	–1.009	–2.202	ns
	GCLK PLL	t_{SU}	2.556	2.556	5.587	ns
		t_H	–2.451	–2.451	–5.310	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	1.113	1.113	2.479	ns
		t_H	–1.008	–1.008	–2.202	ns
	GCLK PLL	t_{SU}	2.555	2.555	5.585	ns
		t_H	–2.450	–2.450	–5.308	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	1.114	1.114	2.479	ns
		t_H	–1.009	–1.009	–2.202	ns
	GCLK PLL	t_{SU}	2.556	2.556	5.587	ns
		t_H	–2.451	–2.451	–5.310	ns

Table 4–66. EP1AGX60 Row Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.281	1.281	2.777	ns
		t_H	–1.176	–1.176	–2.500	ns
	GCLK PLL	t_{SU}	2.853	2.853	6.220	ns
		t_H	–2.748	–2.748	–5.943	ns
LVDS	GCLK	t_{SU}	1.208	1.208	2.664	ns
		t_H	–1.103	–1.103	–2.387	ns
	GCLK PLL	t_{SU}	2.767	2.767	6.083	ns
		t_H	–2.662	–2.662	–5.806	ns

Table 4–67 lists I/O timing specifications.

Table 4–67. EP1AGX60 Column Pins Input Timing Parameters (Part 1 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.124	1.124	2.493	ns
		t_H	–1.019	–1.019	-2.216	ns
	GCLK PLL	t_{SU}	2.694	2.694	5.928	ns
		t_H	–2.589	–2.589	-5.651	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.124	1.124	2.493	ns
		t_H	–1.019	–1.019	-2.216	ns
	GCLK PLL	t_{SU}	2.694	2.694	5.928	ns
		t_H	–2.589	–2.589	-5.651	ns
2.5 V	GCLK	t_{SU}	1.134	1.134	2.475	ns
		t_H	–1.029	–1.029	-2.198	ns
	GCLK PLL	t_{SU}	2.704	2.704	5.910	ns
		t_H	–2.599	–2.599	-5.633	ns
1.8 V	GCLK	t_{SU}	1.200	1.200	2.685	ns
		t_H	–1.095	–1.095	-2.408	ns
	GCLK PLL	t_{SU}	2.770	2.770	6.120	ns
		t_H	–2.665	–2.665	-5.843	ns
1.5 V	GCLK	t_{SU}	1.203	1.203	2.778	ns
		t_H	–1.098	–1.098	-2.501	ns
	GCLK PLL	t_{SU}	2.773	2.773	6.213	ns
		t_H	–2.668	–2.668	-5.936	ns
SSTL-2 CLASS I	GCLK	t_{SU}	0.948	0.948	1.951	ns
		t_H	–0.843	–0.843	-1.674	ns
	GCLK PLL	t_{SU}	2.519	2.519	5.388	ns
		t_H	–2.414	–2.414	-5.111	ns

Table 4–67. EP1AGX60 Column Pins Input Timing Parameters (Part 2 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
SSTL-2 CLASS II	GCLK	t_{SU}	0.948	0.948	1.951	ns
		t_H	–0.843	–0.843	–1.674	ns
	GCLK PLL	t_{SU}	2.519	2.519	5.388	ns
		t_H	–2.414	–2.414	–5.111	ns
SSTL-18 CLASS I	GCLK	t_{SU}	0.986	0.986	2.057	ns
		t_H	–0.881	–0.881	–1.780	ns
	GCLK PLL	t_{SU}	2.556	2.556	5.492	ns
		t_H	–2.451	–2.451	–5.215	ns
SSTL-18 CLASS II	GCLK	t_{SU}	0.987	0.987	2.058	ns
		t_H	–0.882	–0.882	–1.781	ns
	GCLK PLL	t_{SU}	2.558	2.558	5.495	ns
		t_H	–2.453	–2.453	–5.218	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	0.986	0.986	2.057	ns
		t_H	–0.881	–0.881	–1.780	ns
	GCLK PLL	t_{SU}	2.556	2.556	5.492	ns
		t_H	–2.451	–2.451	–5.215	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	0.987	0.987	2.058	ns
		t_H	–0.882	–0.882	–1.781	ns
	GCLK PLL	t_{SU}	2.558	2.558	5.495	ns
		t_H	–2.453	–2.453	–5.218	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.004	1.004	2.185	ns
		t_H	–0.899	–0.899	–1.908	ns
	GCLK PLL	t_{SU}	2.574	2.574	5.620	ns
		t_H	–2.469	–2.469	–5.343	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.005	1.005	2.186	ns
		t_H	–0.900	–0.900	–1.909	ns
	GCLK PLL	t_{SU}	2.576	2.576	5.623	ns
		t_H	–2.471	–2.471	–5.346	ns
3.3-V PCI	GCLK	t_{SU}	1.129	1.129	2.481	ns
		t_H	–1.024	–1.024	–2.204	ns
	GCLK PLL	t_{SU}	2.699	2.699	5.916	ns
		t_H	–2.594	–2.594	–5.639	ns
3.3-V PCI-X	GCLK	t_{SU}	1.129	1.129	2.481	ns
		t_H	–1.024	–1.024	–2.204	ns
	GCLK PLL	t_{SU}	2.699	2.699	5.916	ns
		t_H	–2.594	–2.594	–5.639	ns

Table 4–104. Arria GX Maximum Input Clock Rate for Dedicated Clock Pins (Part 2 of 2)

I/O Standards	–6 Speed Grade	Units
3.3-V PCI-X	373	MHz
SSTL-18 CLASS I	467	MHz
SSTL-18 CLASS II	467	MHz
1.8-V HSTL CLASS I	467	MHz
1.8-V HSTL CLASS II	467	MHz
1.5-V HSTL CLASS I	467	MHz
1.5-V HSTL CLASS II	467	MHz
1.2-V HSTL	233	MHz
DIFFERENTAL SSTL-2	467	MHz
DIFFERENTIAL 2.5-V SSTL CLASS II	467	MHz
DIFFERENTIAL 1.8-V SSTL CLASS I	467	MHz
DIFFERENTIAL 1.8-V SSTL CLASS II	467	MHz
DIFFERENTIAL 1.8-V HSTL CLASS I	467	MHz
DIFFERENTIAL 1.8-V HSTL CLASS II	467	MHz
DIFFERENTIAL 1.5-V HSTL CLASS I	467	MHz
DIFFERENTIAL 1.5-V HSTL CLASS II	467	MHz
DIFFERENTIAL 1.2-V HSTL	233	MHz
LVDS	640	MHz
LVDS *(1)*	373	MHz

Note to Table 4–104:

(1) This set of numbers refers to the VIO dedicated input clock pins.

Table 4–105 shows the maximum output clock toggle rates for Arria GX device column I/O pins.

Table 4–105. Arria GX Maximum Output Toggle Rate for Column I/O Pins (Part 1 of 3)

I/O Standards	Drive Strength	–6 Speed Grade	Units
3.3-V LVTTL	4 mA	196	MHz
	8 mA	303	MHz
	12 mA	393	MHz
	16 mA	486	MHz
	20 mA	570	MHz
	24 mA	626	MHz

Table 4–115. High-Speed I/O Specifications (Part 2 of 2) *Note (1), (2)*

Symbol	Conditions			–6 Speed Grade			Units
				Min	Typ	Max	
DPA lock time	Standard	Training Pattern	Transition Density		—	—	Number of repetitions
	SPI-4	000000000011 11111111	10%	256	—	—	
	Parallel Rapid I/O	00001111	25%	256	—	—	
		10010000	50%	256	—	—	
	Miscellaneous	10101010	100%	256	—	—	
		01010101	—	256	—	—	

Notes to Table 4–115:

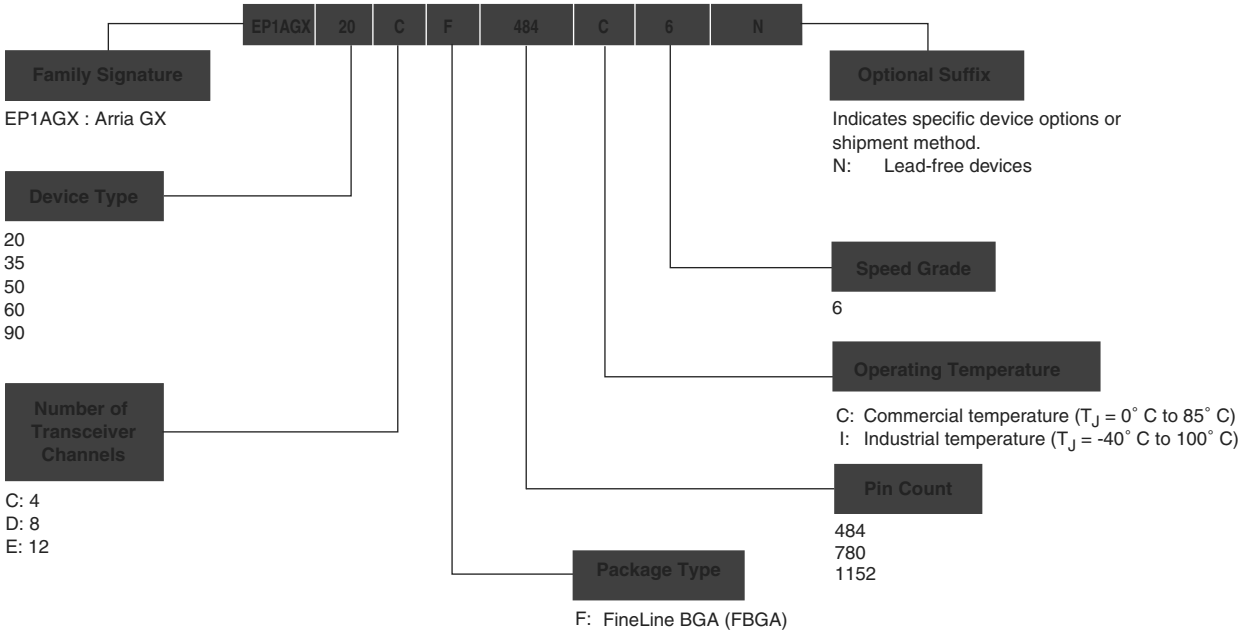
(1) When J = 4 to 10, the SERDES block is used.

(2) When J = 1 or 2, the SERDES block is bypassed.

(3) The input clock frequency and the W factor must satisfy the following fast PLL VCO specification: 150 ≤ input clock frequency × W ≤ 1,040.

(4) The minimum specification is dependent on the clock source (fast PLL, enhanced PLL, clock pin, and so on) and the clock routing resource (global, regional, or local) used. The I/O differential buffer and input register do not have a minimum toggle rate.

Figure 5–1. Arria GX Device Packaging Ordering Information



Document Revision History

Table 5–1 shows the revision history for this chapter.

Table 5–1. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
December 2009, v2.0	■ Document template update. ■ Minor text edits.	—
August 2007, v1.1	Added the "Referenced Documents" section.	—
May 2007, v1.0	Initial Release.	—