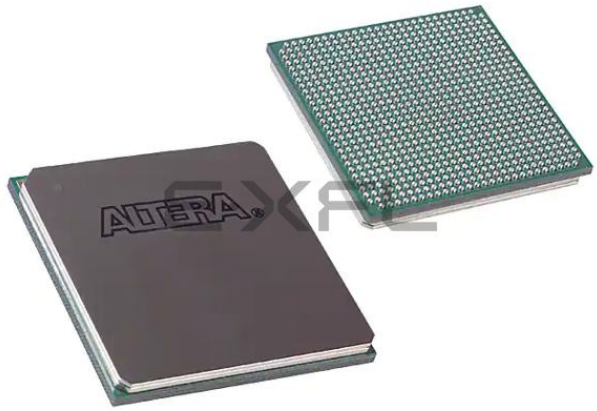

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

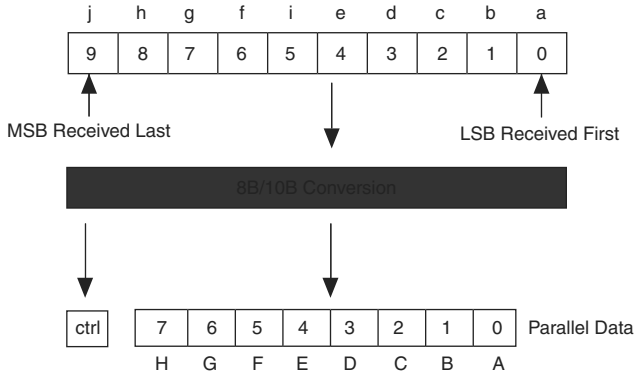
Details	
Product Status	Obsolete
Number of LABs/CLBs	1079
Number of Logic Elements/Cells	21580
Total RAM Bits	1229184
Number of I/O	341
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	780-BBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1agx20cf780i6n

8B/10B Decoder

The 8B/10B decoder is used in all supported functional modes. The 8B/10B decoder takes in 10-bit data from the rate matcher and decodes it into 8-bit data + 1-bit control identifier, thereby restoring the original transmitted data at the receiver. The 8B/10B decoder indicates whether the received 10-bit character is a data or control code through the `rx_ctrldetect` port. If the received 10-bit code group is a control character (`Kx.y`), the `rx_ctrldetect` signal is driven high and if it is a data character (`Dx.y`), the `rx_ctrldetect` signal is driven low.

Figure 2–17 shows a 10-bit code group decoded to an 8-bit data and a 1-bit control indicator.

Figure 2–17. 10-Bit to 8-Bit Conversion



If the received 10-bit code is not a part of valid Dx.y or Kx.y code groups, the 8B/10B decoder block asserts an error flag on the `rx_errdetect` port. If the received 10-bit code is detected with incorrect running disparity, the 8B/10B decoder block asserts an error flag on the `rx_disperr` and `rx_errdetect` ports. The error flag signals (`rx_errdetect` and `rx_disperr`) have the same data path delay from the 8B/10B decoder to the PLD-transceiver interface as the bad code group.

Receiver State Machine

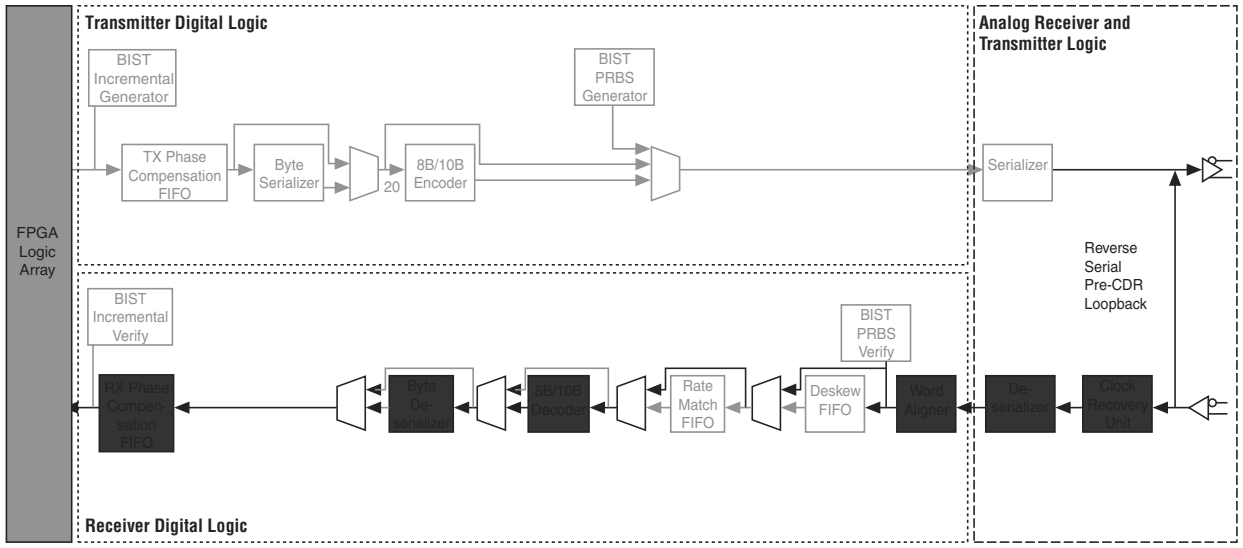
The receiver state machine operates in Basic, GIGE, PCI Express (PIPE), and XAUI modes. In GIGE mode, the receiver state machine replaces invalid code groups with K30.7. In XAUI mode, the receiver state machine translates the XAUI PCS code group to the XAUI XGMII code group.

Reverse Serial Pre-CDR Loopback

Reverse serial pre-CDR loopback mode uses the analog portion of the transceiver. An external source (pattern generator or transceiver) generates the source data. The high-speed serial source data arrives at the high-speed differential receiver input buffer, loops back before the CRU unit, and is transmitted though the high-speed differential transmitter output buffer. It is for test or verification use only to verify the signal being received after the gain and equalization improvements of the input buffer. The signal at the output is not exactly what is received because the signal goes through the output buffer and the V_{OD} is changed to the V_{OD} setting level. Pre-emphasis settings have no effect.

Figure 2–20 shows the Arria GX block in reverse serial pre-CDR loopback mode.

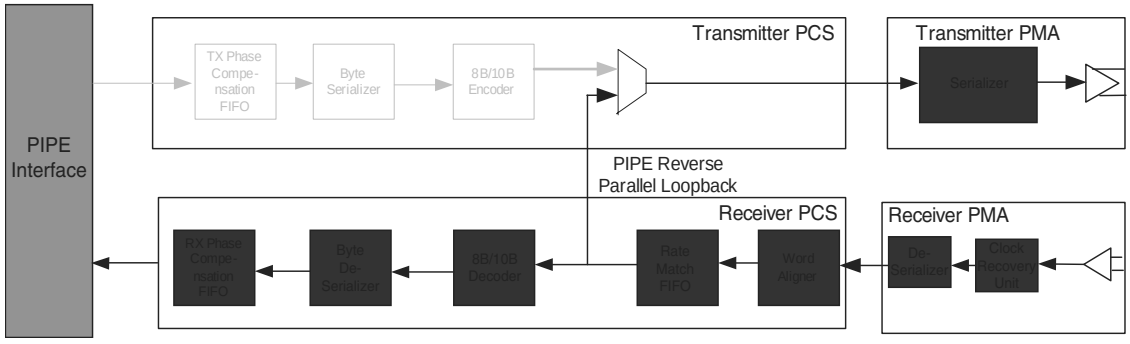
Figure 2–20. Arria GX Block in Reverse Serial Pre-CDR Loopback Mode



PCI Express (PIPE) Reverse Parallel Loopback

Figure 2–21 shows the data path for PCI Express (PIPE) reverse parallel loopback. The reverse parallel loopback configuration is compliant with the PCI Express (PIPE) specification and is available only on PCI Express (PIPE) mode.

Figure 2–21. PCI Express (PIPE) Reverse Parallel Loopback



For more information about transceiver clocking in all supported functional modes, refer to the *Arria GX Transceiver Architecture* chapter.

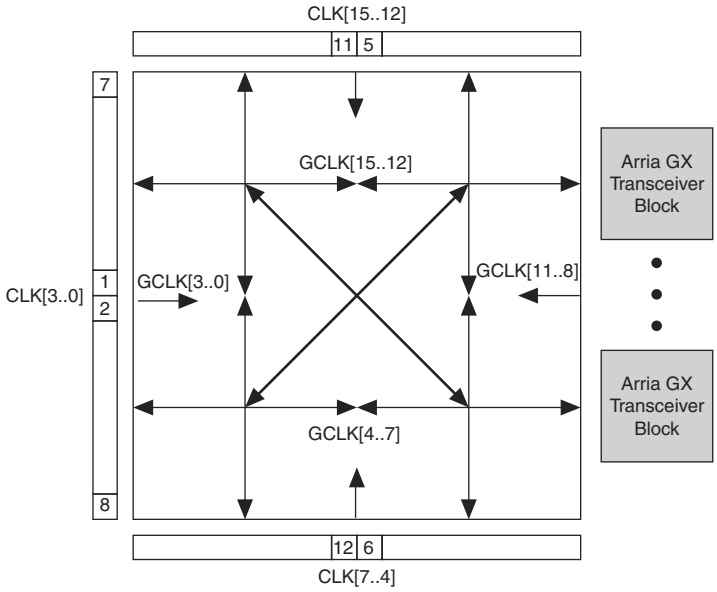
PLD Clock Utilization by Transceiver Blocks

Arria GX devices have up to 16 global clock (GCLK) lines and 16 regional clock (RCLK) lines that are used to route the transceiver clocks. The following transceiver clocks use the available global and regional clock resources:

- `pll_inclk` (if driven from an FPGA input pin)
- `rx_cruclk` (if driven from an FPGA input pin)
- `tx_clkout/coreclkout` (CMU low-speed parallel clock forwarded to the PLD)
- Recovered clock from each channel (`rx_clkout`) in non-rate matcher mode
- Calibration clock (`cal_blk_clk`)
- Fixed clock (`fixedclk` used for receiver detect circuitry in PCI Express [PIPE] mode only)

Figure 2–23 and Figure 2–24 show the available GCLK and RCLK resources in Arria GX devices.

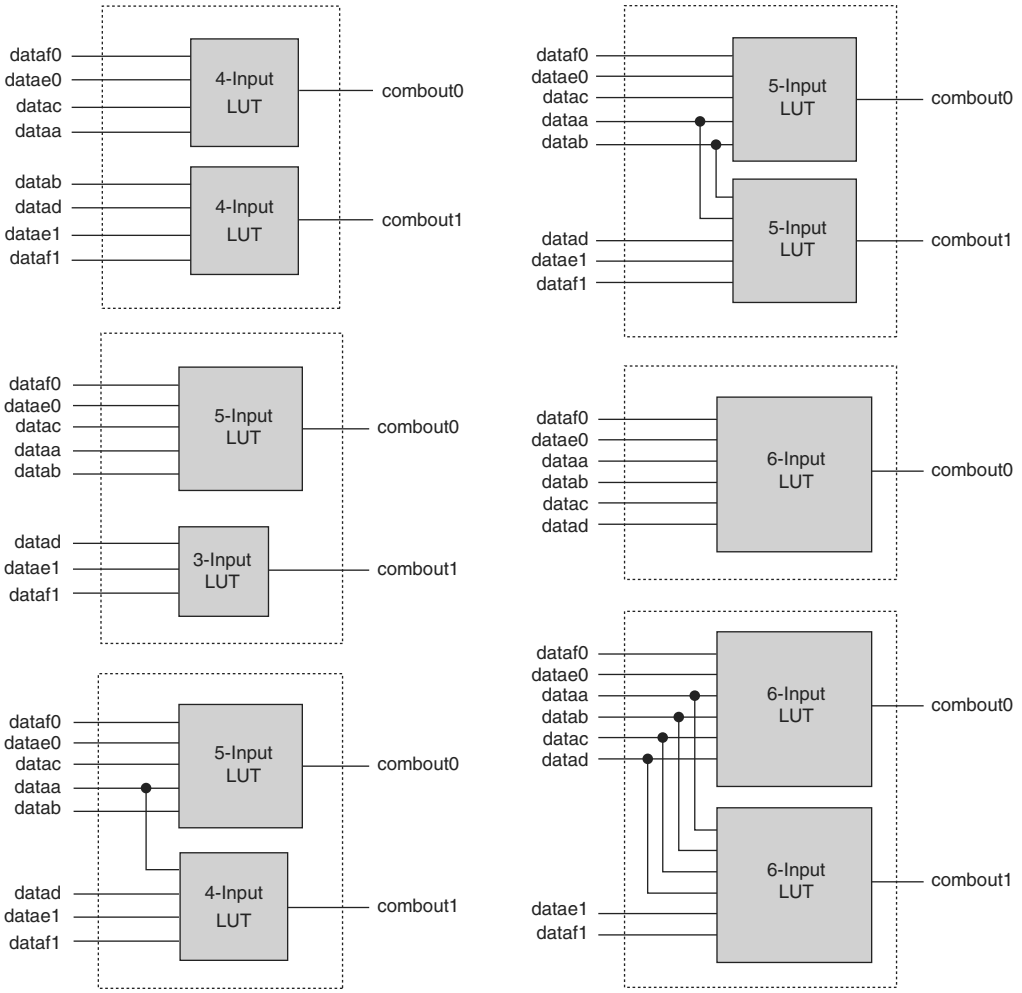
Figure 2–23. Global Clock Resources in Arria GX Devices



Normal Mode

Normal mode is suitable for general logic applications and combinational functions. In this mode, up to eight data inputs from the LAB local interconnect are inputs to the combinational logic. Normal mode allows two functions to be implemented in one Arria GX ALM, or an ALM to implement a single function of up to six inputs. The ALM can support certain combinations of completely independent functions and various combinations of functions which have common inputs. Figure 2–30 shows the supported LUT combinations in normal mode.

Figure 2–30. ALM in Normal Mode *(Note 1)*



Note to Figure 2–30:

(1) Combinations of functions with less inputs than those shown are also supported. For example, combinations of functions with the following number of inputs are supported: 4 and 3, 3 and 3, 3 and 2, 5 and 2, and so on.

Normal mode provides complete backward compatibility with four-input LUT architectures. Two independent functions of four inputs or less can be implemented in one Arria GX ALM. In addition, a five-input function and an independent three-input function can be implemented without sharing inputs.

Table 2–11. TriMatrix Memory Features (Part 2 of 2)

Memory Feature	M512 RAM Block (32 × 18 Bits)	M4K RAM Block (128 × 36 Bits)	M-RAM Block (4K × 144 Bits)
ROM	✓	✓	—
FIFO buffer	✓	✓	✓
Pack mode	—	✓	✓
Byte enable	✓	✓	✓
Address clock enable	—	✓	✓
Parity bits	✓	✓	✓
Mixed clock mode	✓	✓	✓
Memory initialization file (**.mif**)	✓	✓	—
Simple dual-port memory mixed width support	✓	✓	✓
True dual-port memory mixed width support	—	✓	✓
Power-up conditions	Outputs cleared	Outputs cleared	Outputs unknown
Register clears	Output registers	Output registers	Output registers
Mixed-port read-during-write	Unknown output/old data	Unknown output/old data	Unknown output
Configurations	512 × 1 256 × 2 128 × 4 64 × 8 64 × 9 32 × 16 32 × 18	4K × 1 2K × 2 1K × 4 512 × 8 512 × 9 256 × 16 256 × 18 128 × 32 128 × 36	64K × 8 64K × 9 32K × 16 32K × 18 16K × 32 16K × 36 8K × 64 8K × 72 4K × 128 4K × 144

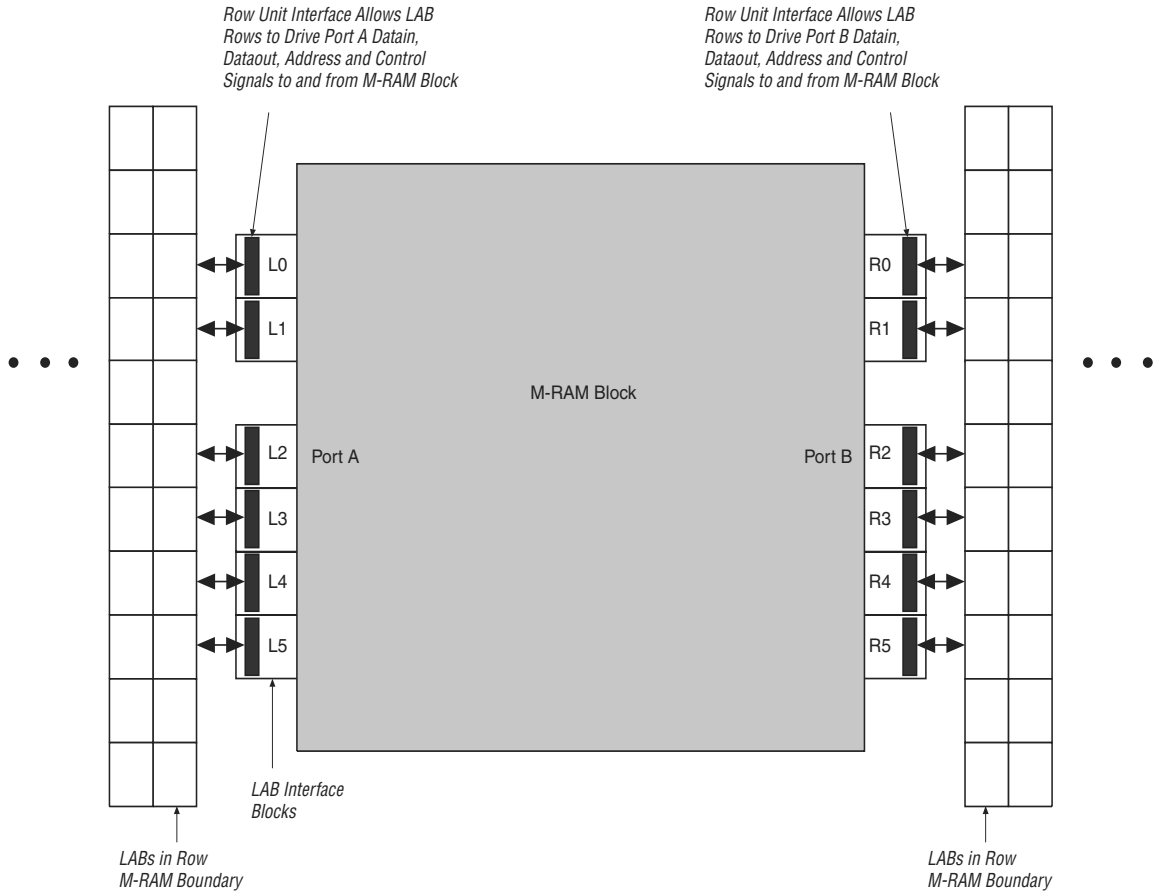
TriMatrix memory provides three different memory sizes for efficient application support. The Quartus II software automatically partitions the user-defined memory into the embedded memory blocks using the most efficient size combinations. You can also manually assign the memory to a specific block size or a mixture of block sizes.

M512 RAM Block

The M512 RAM block is a simple dual-port memory block and is useful for implementing small FIFO buffers, DSP, and clock domain transfer applications. Each block contains 576 RAM bits (including parity bits). M512 RAM blocks can be configured in the following modes:

- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

Figure 2–48. M-RAM Block LAB Row Interface *(Note 1)*



Note to Figure 2–48:

(1) Only R24 and C16 interconnects cross the M-RAM block boundaries.

Table 2–13. DSP Blocks in Arria GX Devices *(Note 1)*

Device	DSP Blocks	Total 9 × 9 Multipliers	Total 18 × 18 Multipliers	Total 36 × 36 Multipliers
EP1AGX20	10	80	40	10
EP1AGX35	14	112	56	14
EP1AGX50	26	208	104	26
EP1AGX60	32	256	128	32
EP1AGX90	44	352	176	44

Note to Table 2–13:

(1) This list only shows functions that can fit into a single DSP block. Multiple DSP blocks can support larger multiplication functions.

Additionally, DSP block input registers can efficiently implement shift registers for FIR filter applications. DSP blocks support Q1.15 format rounding and saturation. Figure 2–51 shows a top-level diagram of the DSP block configured for 18 × 18-bit multiplier mode.

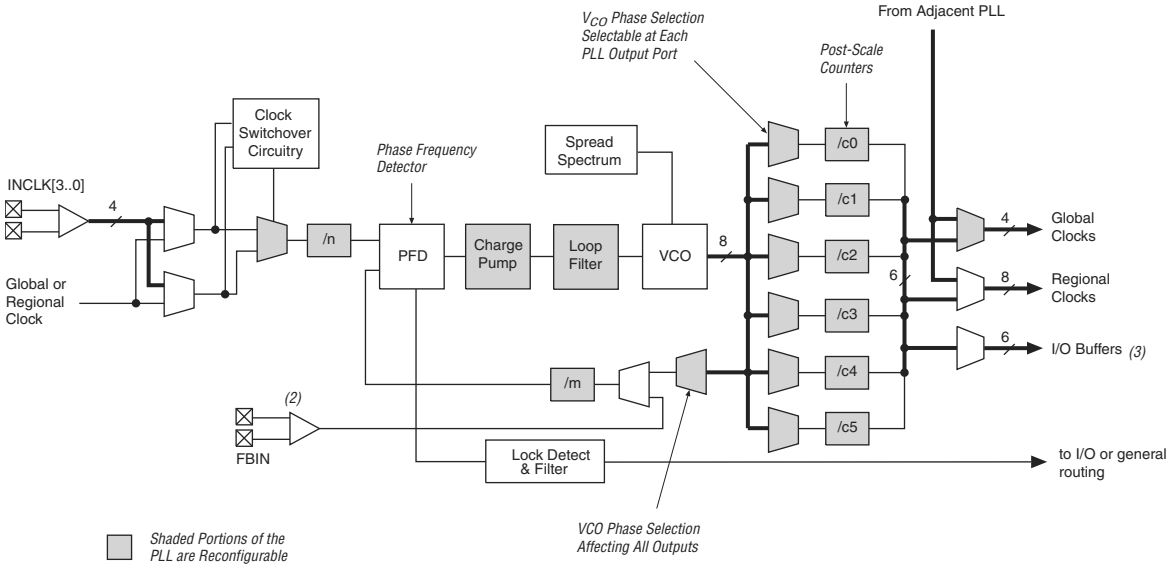
Table 2–20. Global and Regional Clock Connections from Top Clock Pins and Enhanced PLL Outputs

Top Side Global and Regional Clock Network Connectivity	DLLCLK	CLK12	CLK13	CLK14	CLK15	RCLK24	RCLK25	RCLK26	RCLK27	RCLK28	RCLK29	RCLK30	RCLK31
Clock pins													
CLK12p	✓	✓	✓	—	—	✓	—	—	—	✓	—	—	—
CLK13p	✓	✓	✓	—	—	—	✓	—	—	—	✓	—	—
CLK14p	✓	—	—	✓	✓	—	—	✓	—	—	—	✓	—
CLK15p	✓	—	—	✓	✓	—	—	—	✓	—	—	—	✓
CLK12n	—	✓	—	—	—	✓	—	—	—	✓	—	—	—
CLK13n	—	—	✓	—	—	—	✓	—	—	—	✓	—	—
CLK14n	—	—	—	✓	—	—	—	✓	—	—	—	✓	—
CLK15n	—	—	—	—	✓	—	—	—	✓	—	—	—	✓
Drivers from internal logic													
GCLKDRV0	—	✓	—	—	—	—	—	—	—	—	—	—	—
GCLKDRV1	—	—	✓	—	—	—	—	—	—	—	—	—	—
GCLKDRV2	—	—	—	✓	—	—	—	—	—	—	—	—	—
GCLKDRV3	—	—	—	—	✓	—	—	—	—	—	—	—	—
RCLKDRV0	—	—	—	—	—	✓	—	—	—	✓	—	—	—
RCLKDRV1	—	—	—	—	—	—	✓	—	—	—	✓	—	—
RCLKDRV2	—	—	—	—	—	—	—	✓	—	—	—	✓	—
RCLKDRV3	—	—	—	—	—	—	—	—	✓	—	—	—	✓
RCLKDRV4	—	—	—	—	—	✓	—	—	—	✓	—	—	—
RCLKDRV5	—	—	—	—	—	—	✓	—	—	—	✓	—	—
RCLKDRV6	—	—	—	—	—	—	—	✓	—	—	—	✓	—
RCLKDRV7	—	—	—	—	—	—	—	—	✓	—	—	—	✓
Enhanced PLL5 outputs													
c0	✓	✓	✓	—	—	✓	—	—	—	✓	—	—	—
c1	✓	✓	✓	—	—	—	✓	—	—	—	✓	—	—
c2	✓	—	—	✓	✓	—	—	✓	—	—	—	✓	—
c3	✓	—	—	✓	✓	—	—	—	✓	—	—	—	✓
c4	✓	—	—	—	—	✓	—	✓	—	✓	—	✓	—
c5	✓	—	—	—	—	—	✓	—	✓	—	✓	—	✓
Enhanced PLL 11 outputs													
c0	—	✓	✓	—	—	✓	—	—	—	✓	—	—	—
c1	—	✓	✓	—	—	—	✓	—	—	—	✓	—	—
c2	—	—	—	✓	✓	—	—	✓	—	—	—	✓	—
c3	—	—	—	✓	✓	—	—	—	✓	—	—	—	✓
c4	—	—	—	—	—	✓	—	✓	—	✓	—	✓	—
c5	—	—	—	—	—	—	✓	—	✓	—	✓	—	✓

Enhanced PLLs

Arria GX devices contain up to four enhanced PLLs with advanced clock management features. These features include support for external clock feedback mode, spread-spectrum clocking, and counter cascading. Figure 2–65 shows a diagram of the enhanced PLL.

Figure 2–65. Arria GX Enhanced PLL *(Note 1)*



Notes to Figure 2–65:

(1) Each clock source can come from any of the four clock pins that are physically located on the same side of the device as the PLL.

(2) If the feedback input is used, you will lose one (or two, if FBIN is differential) external clock output pin.

(3) Each enhanced PLL has three differential external clock outputs or six single-ended external clock outputs.

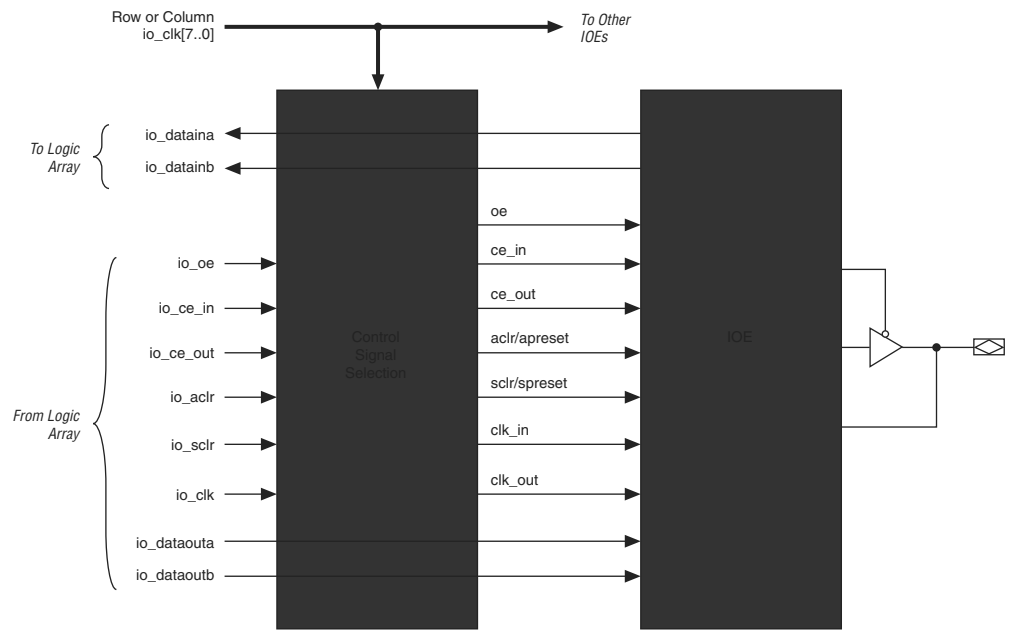
(4) The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal cannot drive the PLL.

Fast PLLs

Arria GX devices contain up to four fast PLLs with high-speed serial interfacing ability. Fast PLLs offer high-speed outputs to manage the high-speed differential I/O interfaces. Figure 2–66 shows a diagram of the fast PLL.

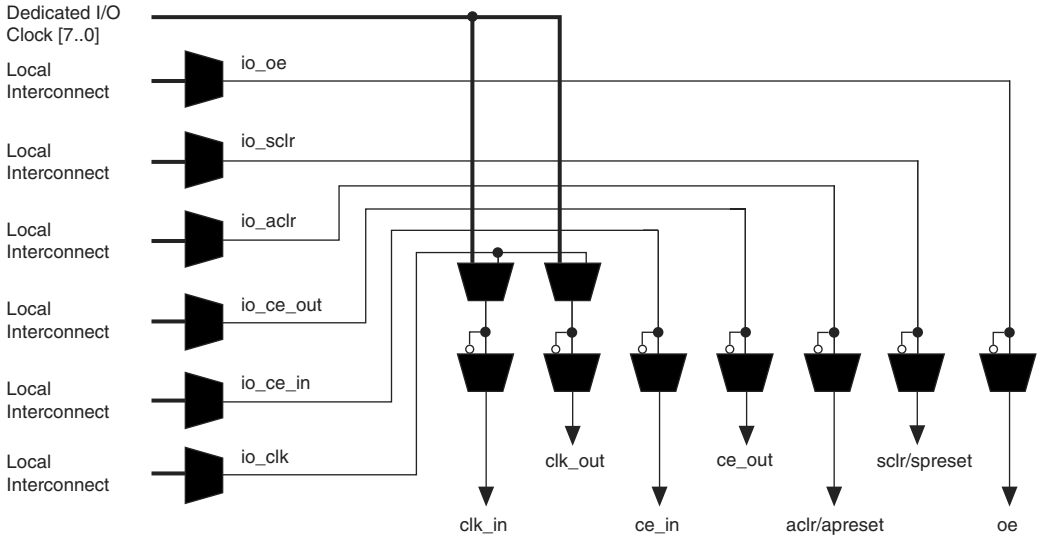
Figure 2–70 shows the signal paths through the I/O block.

Figure 2–70. Signal Path Through the I/O Block



Each IOE contains its own control signal selection for the following control signals: `oe`, `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, `clk_in`, and `clk_out`. Figure 2–71 shows the control signal selection.

Figure 2–71. Control Signal Selection per IOE *(Note 1)*



Notes to Figure 2–71:

(1) Control signals `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, and `oe` can be global signals even though their control selection multiplexers are not directly fed by the `ioe_clk[7..0]` signals. The `ioe_clk` signals can drive the I/O local interconnect, which then drives the control selection multiplexers.

A path in which a pin directly drives a register can require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinational logic may not require the delay. Programmable delays exist for decreasing input-pin-to-logic-array and IOE input register delays. The Quartus II Compiler can program these delays to automatically minimize setup time while providing a zero hold time. Programmable delays can increase the register-to-pin delays for output and/or output enable registers. Programmable delays are no longer required to ensure zero hold times for logic array register-to-IOE register transfers. The Quartus II Compiler can create zero hold time for these transfers. Table 2–22 shows the programmable delays for Arria GX devices.

Table 2–22. Arria GX Devices Programmable Delay Chain

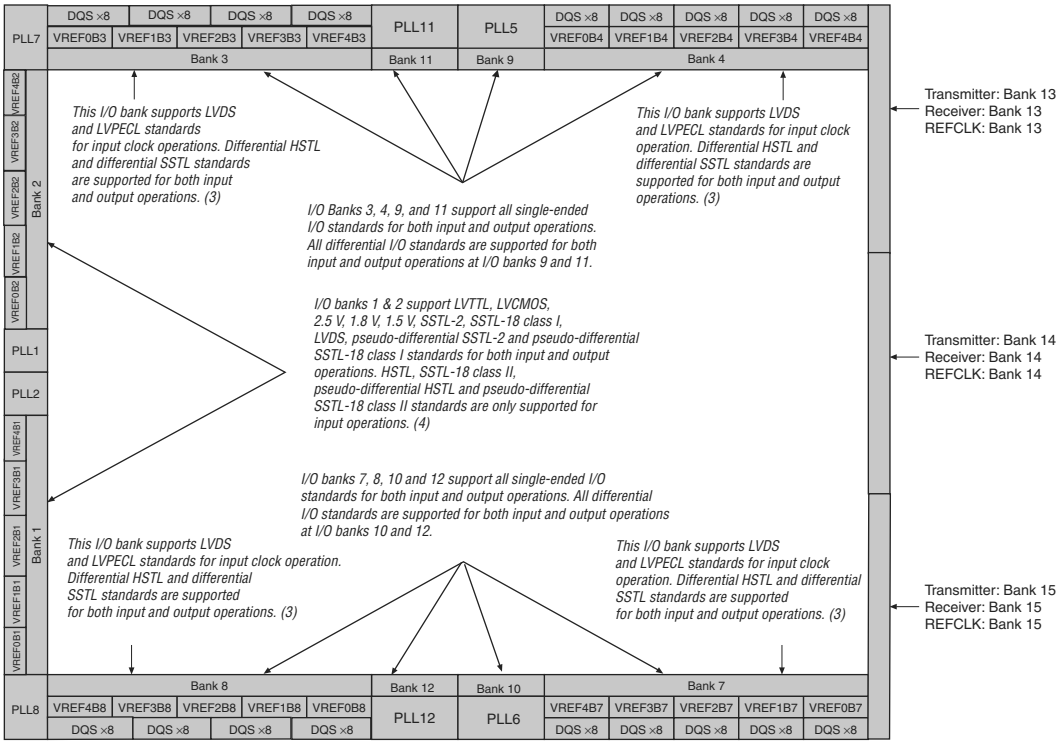
Programmable Delays	Quartus II Logic Option
Input pin to logic array delay	Input delay from pin to internal cells
Input pin to input register delay	Input delay from pin to input register
Output pin delay	Delay from output register to output pin
Output enable register t_{CO} delay	Delay to output enable pin

IOE registers in Arria GX devices share the same source for clear or preset. You can program preset or clear for each individual IOE. You can also program the registers to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power-up. If one register in an IOE uses a preset or clear signal, all registers in the IOE must use that same signal if they require preset or clear. Additionally, a synchronous reset signal is available for the IOE registers.

Double Data Rate I/O Pins

Arria GX devices have six registers in the IOE, which support DDR interfacing by clocking data on both positive and negative clock edges. The IOEs in Arria GX devices support DDR inputs, DDR outputs, and bidirectional DDR modes. When using the IOE for DDR inputs, the two input registers clock double rate input data on alternating edges. An input latch is also used in the IOE for DDR input acquisition. The latch holds the data that is present during the clock high times, allowing both bits of data to be synchronous with the same clock edge (either rising or falling). Figure 2–73 shows an IOE configured for DDR input. Figure 2–74 shows the DDR input timing diagram.

Figure 2–78. Arria GX I/O Banks *(Note 1), (2)*



Notes to Figure 2–78:

(1) Figure 2–78 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

(2) Depending on the size of the device, different device members have different numbers of V_{REF} groups. For the exact locations, refer to the pin list and the Quartus II software.

(3) Banks 9 through 12 are enhanced PLL external clock output banks.

(4) Horizontal I/O banks feature SERDES and DPA circuitry for high-speed differential I/O standards. For more information about differential I/O standards, refer to the *High-Speed Differential I/O Interfaces in Arria GX Devices* chapter.

Each I/O bank has its own VCCIO pins. A single device can support 1.5-, 1.8-, 2.5-, and 3.3-V interfaces; each bank can support a different V_{CCIO} level independently. Each bank also has dedicated VREF pins to support the voltage-referenced standards (such as SSTL-2).

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. Each bank can support one V_{REF} voltage level. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTL, LVCMOS, and 3.3-V PCI for inputs and outputs.

On-Chip Termination

Arria GX devices provide differential (for the LVDS technology I/O standard) and on-chip series termination to reduce reflections and maintain signal integrity. There is no calibration support for these on-chip termination resistors. On-chip termination simplifies board design by minimizing the number of external termination resistors required. Termination can be placed inside the package, eliminating small stubs that can still lead to reflections.

Table 4–7. Arria GX Transceiver Block AC Specification *(Note 1), (2), (3)* (Part 2 of 4)

Description	Condition	–6 Speed Grade Commercial & Industrial	Units
Deterministic jitter at 3.125 Gbps	REFCLK = 156.25 MHz Pattern = CJPAT V_{OD} = 1200 mV No Pre-emphasis	0.17	UI
XAUI Receiver Jitter Tolerance *(4)*			
Total jitter	Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.65	UI
Deterministic jitter	Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.37	UI
Peak-to-peak jitter	Jitter frequency = 22.1 KHz	> 8.5	UI
Peak-to-peak jitter	Jitter frequency = 1.875 MHz	> 0.1	UI
Peak-to-peak jitter	Jitter frequency = 20 MHz	> 0.1	UI
PCI Express (PIPE) Transmitter Jitter Generation *(5)*			
Total Transmitter Jitter Generation	Compliance Pattern; V_{OD} = 800 mV; Pre-emphasis = 49%	< 0.25	UI p-p
PCI Express (PIPE) Receiver Jitter Tolerance *(5)*			
Total Receiver Jitter Tolerance	Compliance Pattern; DC Gain = 3 db	> 0.6	UI p-p
Gigabit Ethernet (GIGE) Transmitter Jitter Generation *(7)*			
Total Transmitter Jitter Generation (TJ)	CRPAT: V_{OD} = 800 mV; Pre-emphasis = 0%	< 0.279	UI p-p
Deterministic Transmitter Jitter Generation (DJ)	CRPAT; V_{OD} = 800 mV; Pre-emphasis = 0%	< 0.14	UI p-p
Gigabit Ethernet (GIGE) Receiver Jitter Tolerance			
Total Jitter Tolerance	CJPAT Compliance Pattern; DC Gain = 0 dB	> 0.66	UI p-p
Deterministic Jitter Tolerance	CJPAT Compliance Pattern; DC Gain = 0 dB	> 0.4	UI p-p
Serial RapidIO (1.25 Gbps, 2.5 Gbps, and 3.125 Gbps) Transmitter Jitter Generation *(6)*			
Total Transmitter Jitter Generation (TJ)	CJPAT Compliance Pattern; V_{OD} = 800 mV; Pre-emphasis = 0%	< 0.35	UI p-p
Deterministic Transmitter Jitter Generation (DJ)	CJPAT Compliance Pattern; V_{OD} = 800 mV; Pre-emphasis = 0%	< 0.17	UI p-p

Table 4–9. PCS Latency (Part 2 of 2) (Part 2 of 2)

Functional Mode	Configuration	Receiver PCS Latency									
		Word Aligner	Deskew FIFO	Rate Matcher *(3)*	8B/10B Decoder	Receiver State Machine	Byte Deserializer	Byte Order	Receiver Phase Comp FIFO	Receiver PIPE	Sum *(2)*
BASIC Single Width	8/10-bit channel width; with Rate Matcher	4–5	—	11–13	1	—	1	1	1–2	1	19–23
	8/10-bit channel width; without Rate Matcher	4–5	—	—	1	—	1	1	1–2	—	8–10
	16/20-bit channel width; with Rate Matcher	2–2.5	—	5.5–6.5	0.5	—	1	1	1–2	—	11–14
	16/20-bit channel width; without Rate Matcher	2–2.5	—	—	0.5	—	1	1	1–2	—	6–7

Notes to Table 4–9:

(1) The latency numbers are with respect to the PLD-transceiver interface clock cycles.

(2) The total latency number is rounded off in the Sum column.

(3) The rate matcher latency shown is the steady state latency. Actual latency may vary depending on the skip ordered set gap allowed by the protocol, actual PPM difference between the reference clocks, and so forth.

Table 4–10 through Table 4–13 show the typical V_{OD} for data rates from 600 Mbps to 3.125 Gbps. The specification is for measurement at the package ball.

Table 4–10. Typical V_{OD} Setting, TX Term = 100 Ω

V_{cc} HTX = 1.5 V	V_{OD} Setting (mV)				
	400	600	800	1000	1200
V_{OD} Typical (mV)	430	625	830	1020	1200

Table 4–11. Typical V_{OD} Setting, TX Term = 100 Ω

V_{cc} HTX = 1.2 V	V_{OD} Setting (mV)				
	320	480	640	800	960
V_{OD} Typical (mV)	344	500	664	816	960

Table 4–12. Typical Pre-Emphasis (First Post-Tap), *(Note 1)*

V_{cc} HTX = 1.5 V	First Post Tap Pre-Emphasis Level				
V_{OD} Setting (mV)	1	2	3	4	5
	TX Term = 100 Ω				
400	24%	62%	112%	184%	—
600	—	31%	56%	86%	122%
800	—	20%	35%	53%	73%

Table 4–21. 3.3-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO} *(1)*	I/O supply voltage for top and bottom PLL banks (9, 10, 11, and 12)	—	3.135	3.3	3.465	V
V_{ID}	Input differential voltage swing (single-ended)	—	100	350	900	mV
V_{ICM}	Input common mode voltage	—	200	1,250	1,800	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	250	—	710	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	840	—	1,570	mV
R_L	Receiver differential input discrete resistor (external to Arria GX devices)	—	90	100	110	Ω

Note to Table 4–21:

(1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT}, not V_{CCIO}. The PLL clock output/feedback differential buffers are powered by VCC_PLL_OUT. For differential clock output/feedback operation, connect VCC_PLL_OUT to 3.3 V.

Table 4–22. 3.3-V PCML Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage	3.135	3.3	3.465	V
V_{ID}	Input differential voltage swing (single-ended)	300	—	600	mV
V_{ICM}	Input common mode voltage	1.5	—	3.465	V
V_{OD}	Output differential voltage (single-ended)	300	370	500	mV
ΔV_{OD}	Change in V_{OD} between high and low	—	—	50	mV
V_{OCM}	Output common mode voltage	2.5	2.85	3.3	V
ΔV_{OCM}	Change in V_{OCM} between high and low	—	—	50	mV
V_T	Output termination voltage	—	V_{CCIO}	—	V
R_1	Output external pull-up resistors	45	50	55	Ω
R_2	Output external pull-up resistors	45	50	55	Ω

Table 4–23. LVPECL Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units	Parameter
V_{CCIO} *(1)*	I/O supply voltage	—	3.135	3.3	3.465	V
V_{ID}	Input differential voltage swing (single-ended)	—	300	600	1,000	mV
V_{ICM}	Input common mode voltage	—	1.0	—	2.5	V
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	525	—	970	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	1,650	—	2,250	mV
R_L	Receiver differential input resistor	—	90	100	110	Ω

Note to Table 4–23:

(1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT}, not V_{CCIO}. The PLL clock output/feedback differential buffers are powered by VCC_PLL_OUT. For differential clock output/feedback operation, connect VCC_PLL_OUT to 3.3 V.

Table 4–49. EP1AGX20 Column Pins Input Timing Parameters (Part 2 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
SSTL-2 CLASS II	GCLK	t_{SU}	1.075	1.075	2.372	ns
		t_H	–0.970	–0.970	–2.095	ns
	GCLK PLL	t_{SU}	2.517	2.517	5.480	ns
		t_H	–2.412	–2.412	–5.203	ns
SSTL-18 CLASS I	GCLK	t_{SU}	1.113	1.113	2.479	ns
		t_H	–1.008	–1.008	–2.202	ns
	GCLK PLL	t_{SU}	2.555	2.555	5.585	ns
		t_H	–2.450	–2.450	–5.308	ns
SSTL-18 CLASS II	GCLK	t_{SU}	1.114	1.114	2.479	ns
		t_H	–1.009	–1.009	–2.202	ns
	GCLK PLL	t_{SU}	2.556	2.556	5.587	ns
		t_H	–2.451	–2.451	–5.310	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	1.113	1.113	2.479	ns
		t_H	–1.008	–1.008	–2.202	ns
	GCLK PLL	t_{SU}	2.555	2.555	5.585	ns
		t_H	–2.450	–2.450	–5.308	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	1.114	1.114	2.479	ns
		t_H	–1.009	–1.009	–2.202	ns
	GCLK PLL	t_{SU}	2.556	2.556	5.587	ns
		t_H	–2.451	–2.451	–5.310	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.131	1.131	2.607	ns
		t_H	–1.026	–1.026	–2.330	ns
	GCLK PLL	t_{SU}	2.573	2.573	5.713	ns
		t_H	–2.468	–2.468	–5.436	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.132	1.132	2.607	ns
		t_H	–1.027	–1.027	–2.330	ns
	GCLK PLL	t_{SU}	2.574	2.574	5.715	ns
		t_H	–2.469	–2.469	–5.438	ns
3.3-V PCI	GCLK	t_{SU}	1.256	1.256	2.903	ns
		t_H	–1.151	–1.151	–2.626	ns
	GCLK PLL	t_{SU}	2.698	2.698	6.009	ns
		t_H	–2.593	–2.593	–5.732	ns
3.3-V PCI-X	GCLK	t_{SU}	1.256	1.256	2.903	ns
		t_H	–1.151	–1.151	–2.626	ns
	GCLK PLL	t_{SU}	2.698	2.698	6.009	ns
		t_H	–2.593	–2.593	–5.732	ns

Table 4–49. EP1AGX20 Column Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
LVDS	GCLK	t_{SU}	1.106	1.106	2.489	ns
		t_H	–1.001	–1.001	–2.212	ns
	GCLK PLL	t_{SU}	2.530	2.530	5.564	ns
		t_H	–2.425	–2.425	–5.287	ns

Table 4–50 describes I/O timing specifications.

Table 4–50. EP1AGX20 Row Pins output Timing Parameters (Part 1 of 2)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	2.904	2.904	6.699	ns
		GCLK PLL	t_{CO}	1.485	1.485	3.627	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.776	2.776	6.059	ns
		GCLK PLL	t_{CO}	1.357	1.357	2.987	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.720	2.720	6.022	ns
		GCLK PLL	t_{CO}	1.301	1.301	2.950	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.776	2.776	6.059	ns
		GCLK PLL	t_{CO}	1.357	1.357	2.987	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.670	2.670	5.753	ns
		GCLK PLL	t_{CO}	1.251	1.251	2.681	ns
2.5 V	4 mA	GCLK	t_{CO}	2.759	2.759	6.033	ns
		GCLK PLL	t_{CO}	1.340	1.340	2.961	ns
2.5 V	8 mA	GCLK	t_{CO}	2.656	2.656	5.775	ns
		GCLK PLL	t_{CO}	1.237	1.237	2.703	ns
2.5 V	12 mA	GCLK	t_{CO}	2.637	2.637	5.661	ns
		GCLK PLL	t_{CO}	1.218	1.218	2.589	ns
1.8 V	2 mA	GCLK	t_{CO}	2.829	2.829	7.052	ns
		GCLK PLL	t_{CO}	1.410	1.410	3.980	ns
1.8 V	4 mA	GCLK	t_{CO}	2.818	2.818	6.273	ns
		GCLK PLL	t_{CO}	1.399	1.399	3.201	ns
1.8 V	6 mA	GCLK	t_{CO}	2.707	2.707	5.972	ns
		GCLK PLL	t_{CO}	1.288	1.288	2.900	ns
1.8 V	8 mA	GCLK	t_{CO}	2.676	2.676	5.858	ns
		GCLK PLL	t_{CO}	1.257	1.257	2.786	ns
1.5 V	2 mA	GCLK	t_{CO}	2.789	2.789	6.551	ns
		GCLK PLL	t_{CO}	1.370	1.370	3.479	ns
1.5 V	4 mA	GCLK	t_{CO}	2.682	2.682	5.950	ns
		GCLK PLL	t_{CO}	1.263	1.263	2.878	ns

Table 4–66. EP1AGX60 Row Pins Input Timing Parameters (Part 2 of 3)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
1.8 V	GCLK	t_{SU}	1.477	1.477	3.275	ns
		t_H	–1.372	–1.372	–2.998	ns
	GCLK PLL	t_{SU}	3.049	3.049	6.718	ns
		t_H	–2.944	–2.944	–6.441	ns
1.5 V	GCLK	t_{SU}	1.480	1.480	3.370	ns
		t_H	–1.375	–1.375	–3.093	ns
	GCLK PLL	t_{SU}	3.052	3.052	6.813	ns
		t_H	–2.947	–2.947	–6.536	ns
SSTL-2 CLASS I	GCLK	t_{SU}	1.237	1.237	2.566	ns
		t_H	–1.132	–1.132	–2.289	ns
	GCLK PLL	t_{SU}	2.800	2.800	5.990	ns
		t_H	–2.695	–2.695	–5.713	ns
SSTL-2 CLASS II	GCLK	t_{SU}	1.237	1.237	2.566	ns
		t_H	–1.132	–1.132	–2.289	ns
	GCLK PLL	t_{SU}	2.800	2.800	5.990	ns
		t_H	–2.695	–2.695	–5.713	ns
SSTL-18 CLASS I	GCLK	t_{SU}	1.255	1.255	2.649	ns
		t_H	–1.150	–1.150	–2.372	ns
	GCLK PLL	t_{SU}	2.827	2.827	6.092	ns
		t_H	–2.722	–2.722	–5.815	ns
SSTL-18 CLASS II	GCLK	t_{SU}	1.255	1.255	2.649	ns
		t_H	–1.150	–1.150	–2.372	ns
	GCLK PLL	t_{SU}	2.827	2.827	6.092	ns
		t_H	–2.722	–2.722	–5.815	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	1.255	1.255	2.649	ns
		t_H	–1.150	–1.150	–2.372	ns
	GCLK PLL	t_{SU}	2.827	2.827	6.092	ns
		t_H	–2.722	–2.722	–5.815	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	1.255	1.255	2.649	ns
		t_H	–1.150	–1.150	–2.372	ns
	GCLK PLL	t_{SU}	2.827	2.827	6.092	ns
		t_H	–2.722	–2.722	–5.815	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.281	1.281	2.777	ns
		t_H	–1.176	–1.176	–2.500	ns
	GCLK PLL	t_{SU}	2.853	2.853	6.220	ns
		t_H	–2.748	–2.748	–5.943	ns

Table 4–69 lists I/O timing specifications.

Table 4–69. EP1AGX60 Column Pins Output Timing Parameters (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	3.036	3.036	6.963	ns
		GCLK PLL	t_{CO}	1.466	1.466	3.528	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.891	2.891	6.591	ns
		GCLK PLL	t_{CO}	1.321	1.321	3.156	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.824	2.824	6.591	ns
		GCLK PLL	t_{CO}	1.254	1.254	3.156	ns
3.3-V LVTTL	16 mA	GCLK	t_{CO}	2.798	2.798	6.422	ns
		GCLK PLL	t_{CO}	1.228	1.228	2.987	ns
3.3-V LVTTL	20 mA	GCLK	t_{CO}	2.776	2.776	6.297	ns
		GCLK PLL	t_{CO}	1.206	1.206	2.862	ns
3.3-V LVTTL	24 mA	GCLK	t_{CO}	2.769	2.769	6.299	ns
		GCLK PLL	t_{CO}	1.199	1.199	2.864	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.891	2.891	6.591	ns
		GCLK PLL	t_{CO}	1.321	1.321	3.156	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.799	2.799	6.296	ns
		GCLK PLL	t_{CO}	1.229	1.229	2.861	ns
3.3-V LVCMOS	12 mA	GCLK	t_{CO}	2.771	2.771	6.218	ns
		GCLK PLL	t_{CO}	1.201	1.201	2.783	ns
3.3-V LVCMOS	16 mA	GCLK	t_{CO}	2.778	2.778	6.186	ns
		GCLK PLL	t_{CO}	1.208	1.208	2.751	ns
3.3-V LVCMOS	20 mA	GCLK	t_{CO}	2.765	2.765	6.168	ns
		GCLK PLL	t_{CO}	1.195	1.195	2.733	ns
3.3-V LVCMOS	24 mA	GCLK	t_{CO}	2.754	2.754	6.146	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.711	ns
2.5 V	4 mA	GCLK	t_{CO}	2.853	2.853	6.623	ns
		GCLK PLL	t_{CO}	1.283	1.283	3.188	ns
2.5 V	8 mA	GCLK	t_{CO}	2.801	2.801	6.361	ns
		GCLK PLL	t_{CO}	1.231	1.231	2.926	ns
2.5 V	12 mA	GCLK	t_{CO}	2.780	2.780	6.244	ns
		GCLK PLL	t_{CO}	1.210	1.210	2.809	ns
2.5 V	16 mA	GCLK	t_{CO}	2.762	2.762	6.170	ns
		GCLK PLL	t_{CO}	1.192	1.192	2.735	ns
1.8 V	2 mA	GCLK	t_{CO}	2.893	2.893	7.615	ns
		GCLK PLL	t_{CO}	1.323	1.323	4.180	ns
1.8 V	4 mA	GCLK	t_{CO}	2.898	2.898	6.841	ns
		GCLK PLL	t_{CO}	1.328	1.328	3.406	ns

Table 4–73. EP1AGX90 Column Pins Input Timing Parameters (Part 2 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
1.8 V	GCLK	t_{SU}	1.094	1.094	2.482	ns
		t_H	–0.989	–0.989	–2.205	ns
	GCLK PLL	t_{SU}	3.158	3.158	6.617	ns
		t_H	–3.053	–3.053	–6.340	ns
1.5 V	GCLK	t_{SU}	1.097	1.097	2.575	ns
		t_H	–0.992	–0.992	–2.298	ns
	GCLK PLL	t_{SU}	3.161	3.161	6.710	ns
		t_H	–3.056	–3.056	–6.433	ns
SSTL-2 CLASS I	GCLK	t_{SU}	0.844	0.844	1.751	ns
		t_H	–0.739	–0.739	–1.474	ns
	GCLK PLL	t_{SU}	2.908	2.908	5.886	ns
		t_H	–2.803	–2.803	–5.609	ns
SSTL-2 CLASS II	GCLK	t_{SU}	0.844	0.844	1.751	ns
		t_H	–0.739	–0.739	–1.474	ns
	GCLK PLL	t_{SU}	2.908	2.908	5.886	ns
		t_H	–2.803	–2.803	–5.609	ns
SSTL-18 CLASS I	GCLK	t_{SU}	0.880	0.880	1.854	ns
		t_H	–0.775	–0.775	–1.577	ns
	GCLK PLL	t_{SU}	2.944	2.944	5.989	ns
		t_H	–2.839	–2.839	–5.712	ns
SSTL-18 CLASS II	GCLK	t_{SU}	0.883	0.883	1.858	ns
		t_H	–0.778	–0.778	–1.581	ns
	GCLK PLL	t_{SU}	2.947	2.947	5.993	ns
		t_H	–2.842	–2.842	–5.716	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	0.880	0.880	1.854	ns
		t_H	–0.775	–0.775	–1.577	ns
	GCLK PLL	t_{SU}	2.944	2.944	5.989	ns
		t_H	–2.839	–2.839	–5.712	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	0.883	0.883	1.858	ns
		t_H	–0.778	–0.778	–1.581	ns
	GCLK PLL	t_{SU}	2.947	2.947	5.993	ns
		t_H	–2.842	–2.842	–5.716	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	0.898	0.898	1.982	ns
		t_H	–0.793	–0.793	–1.705	ns
	GCLK PLL	t_{SU}	2.962	2.962	6.117	ns
		t_H	–2.857	–2.857	–5.840	ns