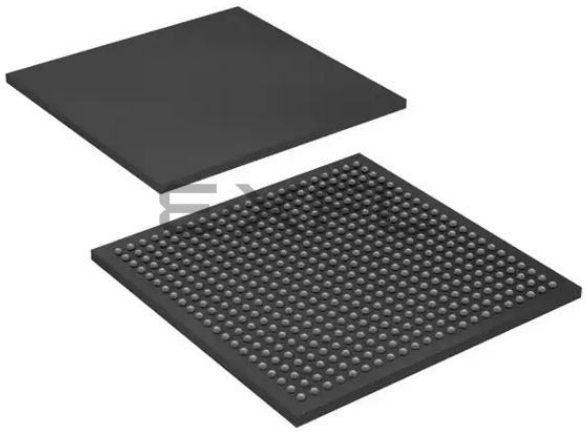

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

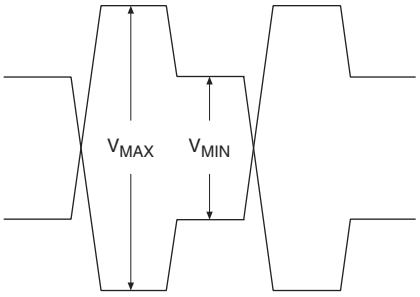
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1676
Number of Logic Elements/Cells	33520
Total RAM Bits	1348416
Number of I/O	230
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1agx35cf484c6

Programmable Pre-Emphasis

The programmable pre-emphasis module controls the output driver to boost high frequency components and compensate for losses in the transmission medium, as shown in Figure 2–10. Pre-emphasis is set statically using the ALTGXB megafunction.

Figure 2–10. Pre-Emphasis Signaling



$$\text{Pre-Emphasis \%} = \left(\frac{V_{MAX}}{V_{MIN}} - 1\right) \times 100$$

Pre-emphasis percentage is defined as $(V_{MAX}/V_{MIN} - 1) \times 100$, where V_{MAX} is the differential emphasized voltage (peak-to-peak) and V_{MIN} is the differential steady-state voltage (peak-to-peak).

PCI Express (PIPE) Receiver Detect

The Arria GX transmitter buffer has a built-in receiver detection circuit for use in PCI Express (PIPE) mode. This circuit provides the ability to detect if there is a receiver downstream by sending out a pulse on the channel and monitoring the reflection. This mode requires a tri-stated transmitter buffer (in electrical idle mode).

PCI Express (PIPE) Electric Idles (or Individual Transmitter Tri-State)

The Arria GX transmitter buffer supports PCI Express (PIPE) electrical idles. This feature is only active in PCI Express (PIPE) mode. The `tx_forceelecidle` port puts the transmitter buffer in electrical idle mode. This port is available in all PCI Express (PIPE) power-down modes and has specific usage in each mode.

Receiver Path

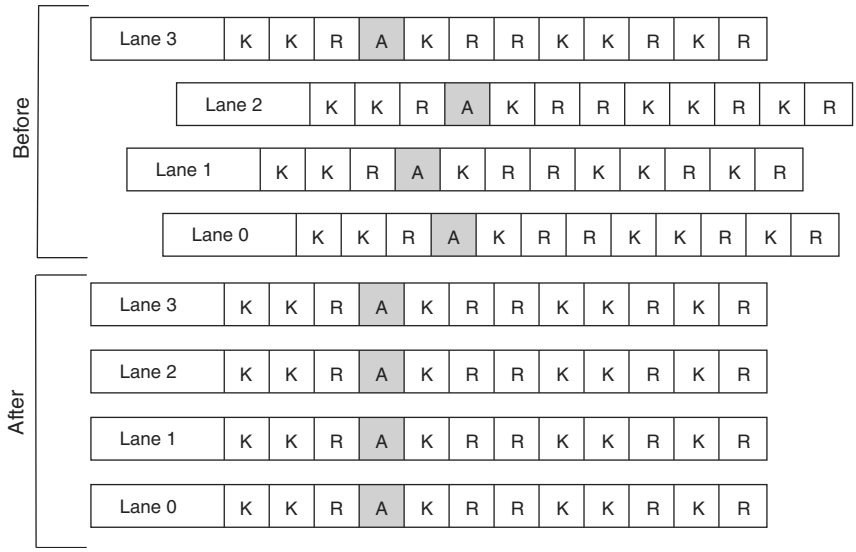
This section describes the data path through the Arria GX receiver. The sub-blocks are described in order from the receiver buffer to the PLD-receiver parallel interface.

Receiver Buffer

The Arria GX receiver input buffer supports the 1.2-V and 1.5-V PCML I/O standards at rates up to 3.125 Gbps. The common mode voltage of the receiver input buffer is programmable between 0.85 V and 1.2 V. You must select the 0.85 V common mode voltage for AC- and DC-coupled PCML links and 1.2 V common mode voltage for DC-coupled LVDS links.

Figure 2–16 shows misaligned channels before the channel aligner and the aligned channels after the channel aligner.

Figure 2–16. Before and After the Channel Aligner



Rate Matcher

In asynchronous systems, the upstream transmitter and local receiver can be clocked with independent reference clock sources. Frequency differences in the order of a few hundred PPM can potentially corrupt the data at the receiver.

The rate matcher compensates for small clock frequency differences between the upstream transmitter and the local receiver clocks by inserting or removing skip characters from the inter packet gap (IPG) or idle streams. It inserts a skip character if the local receiver is running a faster clock than the upstream transmitter. It deletes a skip character if the local receiver is running a slower clock than the upstream transmitter. The Quartus II software automatically configures the appropriate skip character as specified in the IEEE 802.3 for GIGE mode and PCI-Express Base Specification for PCI Express (PIPE) mode. The rate matcher is bypassed in Serial RapidIO and must be implemented in the PLD logic array or external circuits depending on your system design.

Table 2–5 lists the maximum frequency difference that the rate matcher can tolerate in XAUI, PCI Express (PIPE), GIGE, and Basic functional modes.

Table 2–5. Rate Matcher PPM Tolerance

Function Mode	PPM
XAUI	± 100
PCI Express (PIPE)	± 300
GIGE	± 100
Basic	± 300

XAUI Mode

In XAUI mode, the rate matcher adheres to clause 48 of the IEEE 802.3ae specification for clock rate compensation. The rate matcher performs clock compensation on columns of /R/ (/K28.0/), denoted by //R//. An //R// is added or deleted automatically based on the number of words in the FIFO buffer.

PCI Express (PIPE) Mode Rate Matcher

In PCI Express (PIPE) mode, the rate matcher can compensate up to ± 300 PPM (600 PPM total) frequency difference between the upstream transmitter and the receiver. The rate matcher logic looks for skip ordered sets (SOS), which contains a /K28.5/ comma followed by three /K28.0/ skip characters. The rate matcher logic deletes or inserts /K28.0/ skip characters as necessary from/to the rate matcher FIFO.

The rate matcher in PCI Express (PIPE) mode has a FIFO buffer overflow and underflow protection. In the event of a FIFO buffer overflow, the rate matcher deletes any data after detecting the overflow condition to prevent FIFO pointer corruption until the rate matcher is not full. In an underflow condition, the rate matcher inserts 9'h1FE (/K30.7/) until the FIFO buffer is not empty. These measures ensure that the FIFO buffer can gracefully exit the overflow and underflow condition without requiring a FIFO reset. The rate matcher FIFO overflow and underflow condition is indicated on the `pipestatus` port.

You can bypass the rate matcher in PCI Express (PIPE) mode if you have a synchronous system where the upstream transmitter and local receiver derive their reference clocks from the same source.

GIGE Mode Rate Matcher

In GIGE mode, the rate matcher can compensate up to ± 100 PPM (200 PPM total) frequency difference between the upstream transmitter and the receiver. The rate matcher logic inserts or deletes /I2/ idle ordered sets to/from the rate matcher FIFO during the inter-frame or inter-packet gap (IFG or IPG). /I2/ is selected as the rate matching ordered set because it maintains the running disparity, unlike /I1/ that alters the running disparity. Because the /I2/ ordered-set contains two 10-bit code groups (/K28.5/, /D16.2/), 20 bits are inserted or deleted at a time for rate matching.

The rate matcher logic has the capability to insert or delete /C1/ or /C2/ configuration ordered sets when 'GIGE Enhanced' mode is chosen as the sub-protocol in the MegaWizard Plug-In Manager.

If the frequency PPM difference between the upstream transmitter and the local receiver is high, or if the packet size is too large, the rate matcher FIFO buffer can face an overflow or underflow situation.

Basic Mode

In basic mode, you can program the skip and control pattern for rate matching. There is no restriction on the deletion of a skip character in a cluster. The rate matcher deletes the skip characters as long as they are available. For insertion, the rate matcher inserts skip characters such that the number of skip characters at the output of rate matcher does not exceed five.

In GIGE and Serial RapidIO modes, you can dynamically put each transceiver channel individually in serial loopback by controlling the `rx_seriallpbken` port. A high on the `rx_seriallpbken` port puts the transceiver into serial loopback and a low takes the transceiver out of serial loopback.

As seen in Figure 2–18, the serial data output from the transmitter serializer is looped back to the receiver CRU in serial loopback. The transmitter data path from the PLD interface to the serializer in serial loopback is the same as in non-loopback mode. The receiver data path from the clock recovery unit to the PLD interface in serial loopback is the same as in non-loopback mode. Because the entire transceiver data path is available in serial loopback, this option is often used to diagnose the data path as a probable cause of link errors.

☞ When serial loopback is enabled, the transmitter output buffer is still active and drives the serial data out on the `tx_dataout` port.

Reverse Serial Loopback

Reverse serial loopback mode uses the analog portion of the transceiver. An external source (pattern generator or transceiver) generates the source data. The high-speed serial source data arrives at the high-speed differential receiver input buffer, passes through the CRU unit and the retimed serial data is looped back, and is transmitted though the high-speed differential transmitter output buffer.

Figure 2–19 shows the data path in reverse serial loopback mode.

Figure 2–19. Arria GX Block in Reverse Serial Loopback Mode

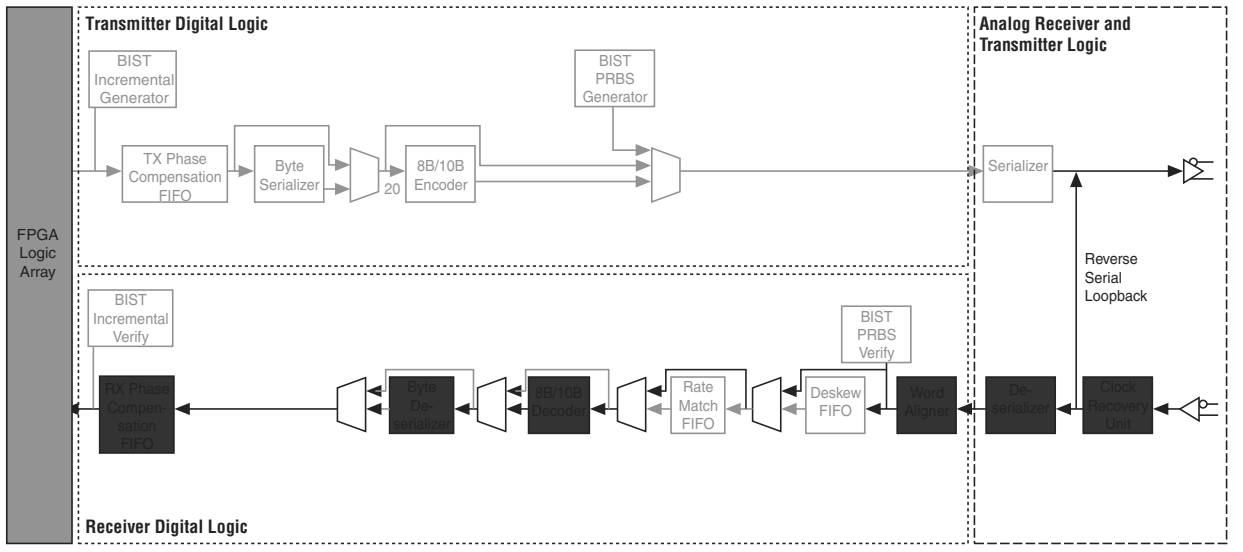
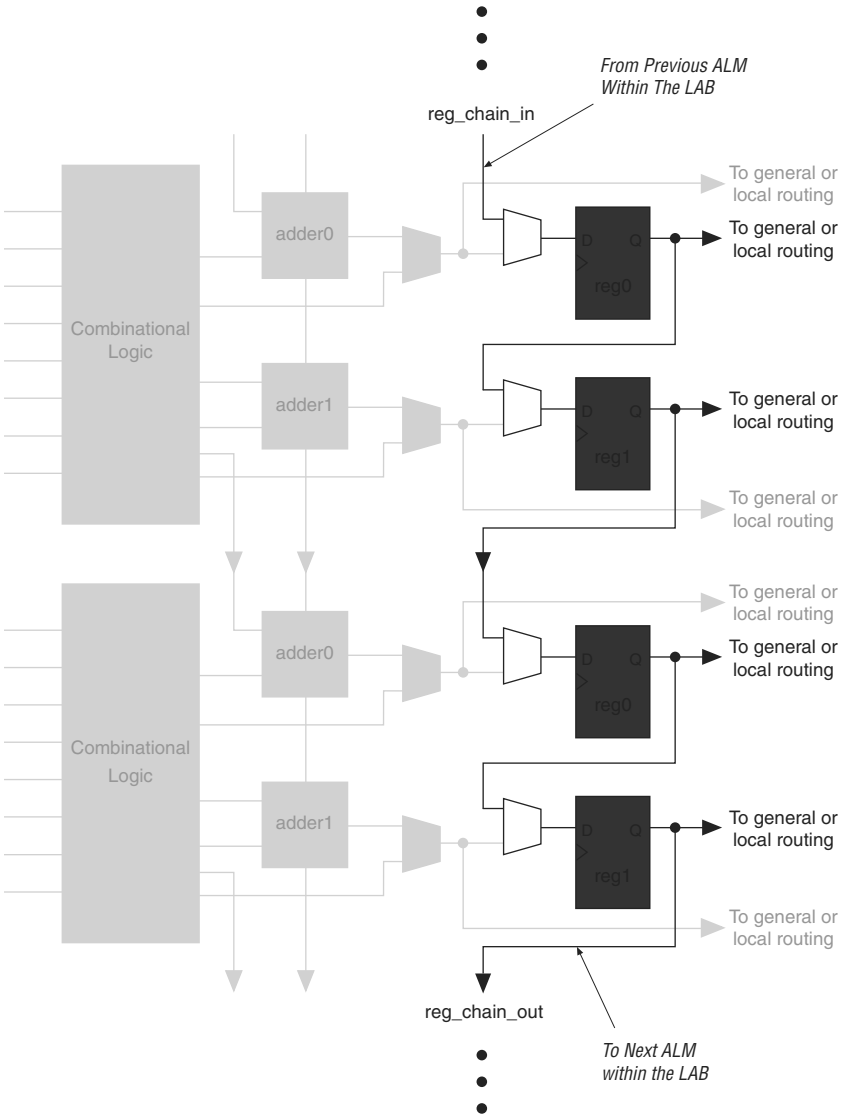


Figure 2–38. Register Chain within a LAB *(Note 1)*



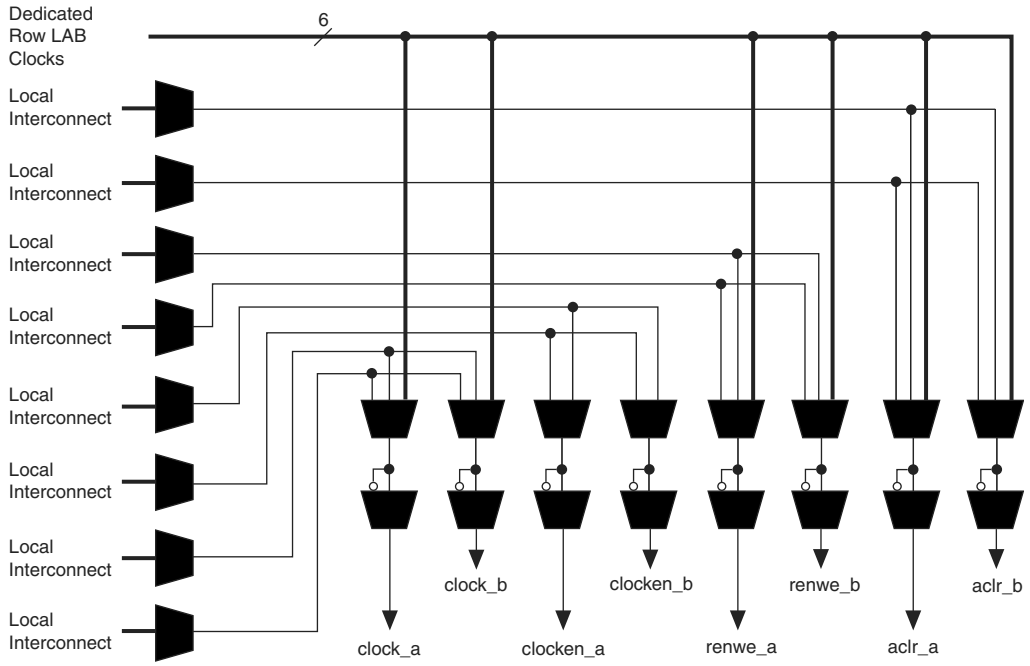
Note to Figure 2–38:

(1) The combinational or adder logic can be used to implement an unrelated, unregistered function.

Clear and Preset Logic Control

LAB-wide signals control the logic for the register's clear and load/preset signals. The ALM directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. The direct asynchronous preset does not require a NOT gate push-back technique. Arria GX devices support simultaneous asynchronous load/preset and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one load/preset signal.

Figure 2–44. M4K RAM Block Control Signals



The R4, C4, and direct link interconnects from adjacent LABs drive the M4K RAM block local interconnect. The M4K RAM blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 16 direct link input connections to the M4K RAM block are possible from the left adjacent LABs and another 16 are possible from the right adjacent LAB. M4K RAM block outputs can also connect to left and right LABs through direct link interconnect. Figure 2–45 shows the M4K RAM block to logic array interface.

Modes of Operation

The adder, subtractor, and accumulate functions of a DSP block have four modes of operation:

- Simple multiplier
- Multiply-accumulator
- Two-multipliers adder
- Four-multipliers adder

Table 2–14 shows the different number of multipliers possible in each DSP block mode according to size. These modes allow the DSP blocks to implement numerous applications for DSP including FFTs, complex FIR, FIR, 2D FIR filters, equalizers, IIR, correlators, matrix multiplication, and many other functions. DSP blocks also support mixed modes and mixed multiplier sizes in the same block. For example, half of one DSP block can implement one 18 × 18-bit multiplier in multiply-accumulator mode, while the other half of the DSP block implements four 9 × 9-bit multipliers in simple multiplier mode.

Table 2–14. Multiplier Size and Configurations per DSP Block

DSP Block Mode	9 × 9	18 × 18	36 × 36
Multiplier	Eight multipliers with eight product outputs	Four multipliers with four product outputs	One multiplier with one product output
Multiply-accumulator	—	Two 52-bit multiply-accumulate blocks	—
Two-multipliers adder	Four two-multiplier adder (two 9 × 9 complex multiply)	Two two-multiplier adder (one 18 × 18 complex multiply)	—
Four-multipliers adder	Two four-multiplier adder	One four-multiplier adder	—

DSP Block Interface

The Arria GX device DSP block input registers can generate a shift register that can cascade down in the same DSP block column. Dedicated connections between DSP blocks provide fast connections between shift register inputs to cascade shift register chains. You can cascade registers within multiple DSP blocks for 9 × 9- or 18 × 18-bit FIR filters larger than four taps, with additional adder stages implemented in ALMs. If the DSP block is configured as 36 × 36 bits, the adder, subtractor, or accumulator stages are implemented in ALMs. Each DSP block can route the shift register chain out of the block to cascade multiple columns of DSP blocks.

The DSP block is divided into four block units that interface with four LAB rows on the left and right. Each block unit can be considered one complete 18 × 18-bit multiplier with 36 inputs and 36 outputs. A local interconnect region is associated with each DSP block. Like an LAB, this interconnect region can be fed with 16 direct link interconnects from the LAB to the left or right of the DSP block in the same row. R4 and C4 routing resources can access the DSP block's local interconnect region.

The outputs also work similarly to LAB outputs. Eighteen outputs from the DSP block can drive to the left LAB through direct link interconnects and 18 can drive to the right LAB though direct link interconnects. All 36 outputs can drive to R4 and C4 routing interconnects. Outputs can drive right- or left-column routing.

Table 2–15. DSP Block Signal Sources and Destinations

LAB Row at Interface	Control Signals Generated	Data Inputs	Data Outputs
0	clock0 aclr0 ena0 mult01_saturate addnsub1_round/ accum_round addnsub1 signa sourcea sourceb	A1[17..0] B1[17..0]	OA[17..0] OB[17..0]
1	clock1 aclr1 ena1 accum_saturate mult01_round accum_sload sourcea sourceb mode0	A2[17..0] B2[17..0]	OC[17..0] OD[17..0]
2	clock2 aclr2 ena2 mult23_saturate addnsub3_round/ accum_round addnsub3 sign_b sourcea sourceb	A3[17..0] B3[17..0]	OE[17..0] OF[17..0]
3	clock3 aclr3 ena3 accum_saturate mult23_round accum_sload sourcea sourceb mode1	A4[17..0] B4[17..0]	OG[17..0] OH[17..0]

PLLs and Clock Networks

Arria GX devices provide a hierarchical clock structure and multiple PLLs with advanced features. The large number of clocking resources in combination with the clock synthesis precision provided by enhanced and fast PLLs provides a complete clock management solution.

Global and Hierarchical Clocking

Arria GX devices provide 16 dedicated global clock networks and 32 regional clock networks (eight per device quadrant). These clocks are organized into a hierarchical clock structure that allows for up to 24 clocks per device region with low skew and delay. This hierarchical clocking scheme provides up to 48 unique clock domains in Arria GX devices.

There are 12 dedicated clock pins (`CLK[15..12]` and `CLK[7..0]`) to drive either the global or regional clock networks. Four clock pins drive each side of the device except the right side, as shown in Figure 2–54 and Figure 2–55. Internal logic and enhanced and fast PLL outputs can also drive the global and regional clock networks. Each global and regional clock has a clock control block, which controls the selection of the clock source and dynamically enables or disables the clock to reduce power consumption. Table 2–16 lists the global and regional clock features.

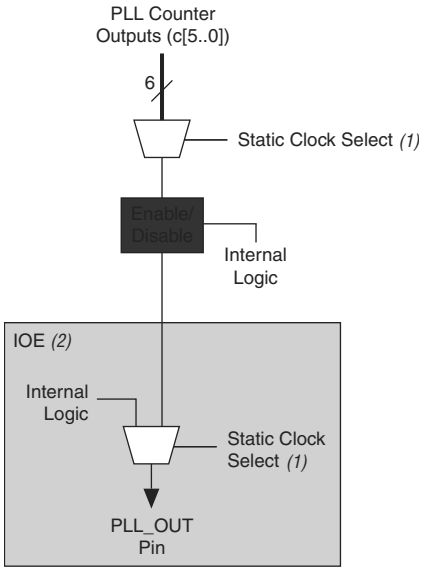
Table 2–16. Global and Regional Clock Features

Feature	Global Clocks	Regional Clocks
Number per device	16	32
Number available per quadrant	16	8
Sources	Clock pins, PLL outputs, core routings, inter-transceiver clocks	Clock pins, PLL outputs, core routings, inter-transceiver clocks
Dynamic clock source selection	✓	—
Dynamic enable/disable	✓	✓

Global Clock Network

These clocks drive throughout the entire device, feeding all device quadrants. GCLK networks can be used as clock sources for all resources in the device IOEs, ALMs, DSP blocks, and all memory blocks. These resources can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin. The global clock networks can also be driven by internal logic for internally generated global clocks and asynchronous clears, clock enables, or other control signals with large fanout. Figure 2–54 shows the 12 dedicated `CLK` pins driving global clock networks.

Figure 2–60. External PLL Output Clock Control Blocks



Notes to Figure 2–60:

(1) These clock select signals can only be set through a configuration file (**.sof** or **.pof**) and cannot be dynamically controlled during user mode operation.

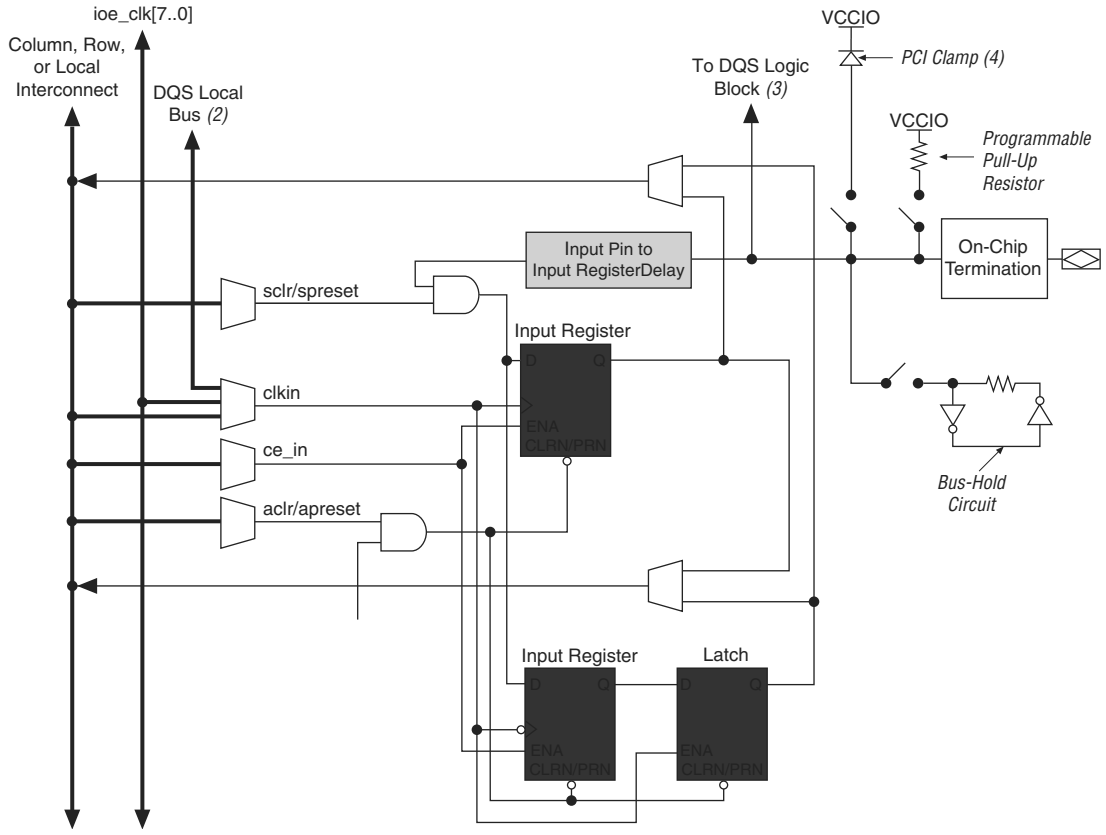
(2) The clock control block feeds to a multiplexer within the PLL_OUT pin's IOE. The PLL_OUT pin is a dual-purpose pin. Therefore, this multiplexer selects either an internal signal or the output of the clock control block.

For the global clock control block, clock source selection can be controlled either statically or dynamically. You have the option of statically selecting the clock source by using the Quartus II software to set specific configuration bits in the configuration file (**.sof** or **.pof**) or controlling the selection dynamically by using internal logic to drive the multiplexer select inputs. When selecting statically, the clock source can be set to any of the inputs to the select multiplexer. When selecting the clock source dynamically, you can either select between two PLL outputs (such as the C0 or C1 outputs from one PLL), between two PLLs (such as the C0/C1 clock output of one PLL or the C0/C1 clock output of the other PLL), between two clock pins (such as CLK0 or CLK1), or between a combination of clock pins or PLL outputs.

For the regional and PLL_OUT clock control block, clock source selection can only be controlled statically using configuration bits. Any of the inputs to the clock select multiplexer can be set as the clock source.

Arria GX clock networks can be disabled (powered down) by both static and dynamic approaches. When a clock net is powered down, all logic fed by the clock net is in an off-state thereby reducing the overall power consumption of the device. GCLK and RCLK networks can be powered down statically through a setting in the configuration file (**.sof** or **.pof**). Clock networks that are not used are automatically powered down through configuration bit settings in the configuration file generated by the Quartus II software. The dynamic clock enable or disable feature allows the internal logic to control power up/down synchronously on GCLK and RCLK nets and PLL_OUT pins. This function is independent of the PLL and is applied directly on the clock network or PLL_OUT pin, as shown in Figure 2–58 through Figure 2–60.

Figure 2–73. Arria GX IOE in DDR Input I/O Configuration *(Note 1)*



Notes to Figure 2–73:

(1) All input signals to the IOE can be inverted at the IOE.
(2) This signal connection is only allowed on dedicated DQ function pins.
(3) This signal is for dedicated DQS function pins only.
(4) The optional PCI clamp is only available on column I/O pins.

Figure 2–74. Input Timing Diagram in DDR Mode

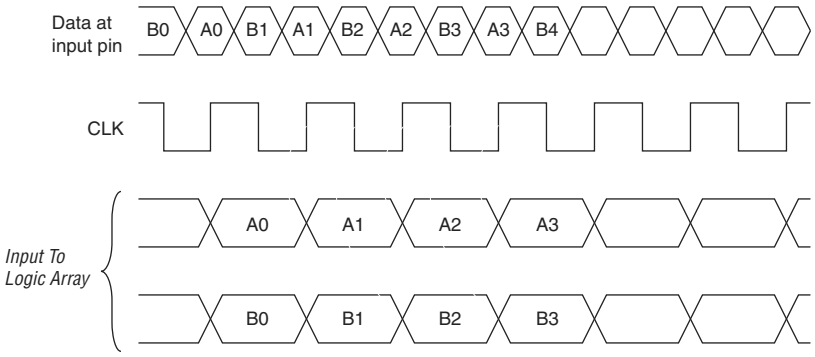
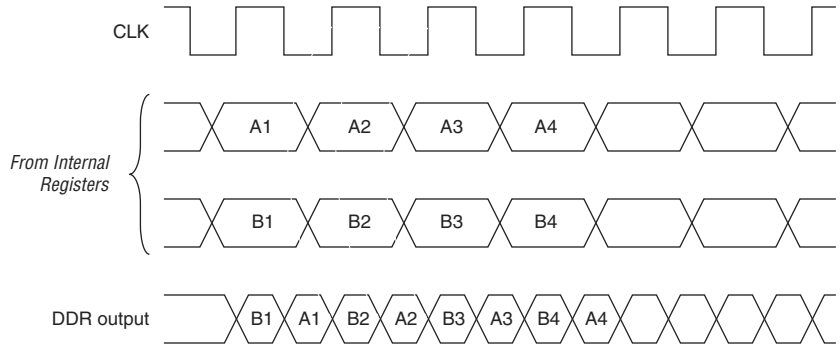


Figure 2–76. Output Timing Diagram in DDR Mode



The Arria GX IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations. The negative-edge-clocked OE register holds the OE signal inactive until the falling edge of the clock to meet DDR SDRAM timing requirements.

External RAM Interfacing

In addition to the six I/O registers in each IOE, Arria GX devices also have dedicated phase-shift circuitry for interfacing with external memory interfaces, including DDR, DDR2 SDRAM, and SDR SDRAM. In every Arria GX device, the I/O banks at the top (Banks 3 and 4) and bottom (Banks 7 and 8) of the device support DQ and DQS signals with DQ bus modes of ×4, ×8/×9, ×16/×18, or ×32/×36. Table 2–23 shows the number of DQ and DQS buses that are supported per device.

Table 2–23. DQS and DQ Bus Mode Support *(Note 1)*

Device	Package	Number of ×4 Groups	Number of ×8/×9 Groups	Number of ×16/×18 Groups	Number of ×32/×36 Groups
EP1AGX20	484-pin FineLine BGA	2	0	0	0
EP1AGX35	484-pin FineLine BGA	2	0	0	0
	780-pin FineLine BGA	18	8	4	0
EP1AGX50/60	484-pin FineLine BGA	2	0	0	0
	780-pin FineLine BGA	18	8	4	0
	1,152-pin FineLine BGA	36	18	8	4
EP1AGX90	1,152-pin FineLine BGA	36	18	8	4

Note to Table 2–23:

(1) Numbers are preliminary until devices are available.

A compensated delay element on each DQS pin automatically aligns input DQS synchronization signals with the data window of their corresponding DQ data signals. The DQS signals drive a local DQS bus in the top and bottom I/O banks. This DQS bus is an additional resource to the I/O clocks and is used to clock DQ input registers with the DQS signal.

Table 4–21. 3.3-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO} *(1)*	I/O supply voltage for top and bottom PLL banks (9, 10, 11, and 12)	—	3.135	3.3	3.465	V
V_{ID}	Input differential voltage swing (single-ended)	—	100	350	900	mV
V_{ICM}	Input common mode voltage	—	200	1,250	1,800	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	250	—	710	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	840	—	1,570	mV
R_L	Receiver differential input discrete resistor (external to Arria GX devices)	—	90	100	110	Ω

Note to Table 4–21:

(1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT}, not V_{CCIO}. The PLL clock output/feedback differential buffers are powered by VCC_PLL_OUT. For differential clock output/feedback operation, connect VCC_PLL_OUT to 3.3 V.

Table 4–22. 3.3-V PCML Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage	3.135	3.3	3.465	V
V_{ID}	Input differential voltage swing (single-ended)	300	—	600	mV
V_{ICM}	Input common mode voltage	1.5	—	3.465	V
V_{OD}	Output differential voltage (single-ended)	300	370	500	mV
ΔV_{OD}	Change in V_{OD} between high and low	—	—	50	mV
V_{OCM}	Output common mode voltage	2.5	2.85	3.3	V
ΔV_{OCM}	Change in V_{OCM} between high and low	—	—	50	mV
V_T	Output termination voltage	—	V_{CCIO}	—	V
R_1	Output external pull-up resistors	45	50	55	Ω
R_2	Output external pull-up resistors	45	50	55	Ω

Table 4–23. LVPECL Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units	Parameter
V_{CCIO} *(1)*	I/O supply voltage	—	3.135	3.3	3.465	V
V_{ID}	Input differential voltage swing (single-ended)	—	300	600	1,000	mV
V_{ICM}	Input common mode voltage	—	1.0	—	2.5	V
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	525	—	970	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	1,650	—	2,250	mV
R_L	Receiver differential input resistor	—	90	100	110	Ω

Note to Table 4–23:

(1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT}, not V_{CCIO}. The PLL clock output/feedback differential buffers are powered by VCC_PLL_OUT. For differential clock output/feedback operation, connect VCC_PLL_OUT to 3.3 V.

Table 4–51. EP1AGX20 Column Pins Output Timing Parameters (Part 3 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
SSTL-18 CLASS II	16 mA	GCLK	t_{CO}	2.609	2.609	5.603	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.491	ns
SSTL-18 CLASS II	18 mA	GCLK	t_{CO}	2.605	2.605	5.611	ns
		GCLK PLL	t_{CO}	1.160	1.160	2.499	ns
SSTL-18 CLASS II	20 mA	GCLK	t_{CO}	2.605	2.605	5.609	ns
		GCLK PLL	t_{CO}	1.160	1.160	2.497	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.629	2.629	5.664	ns
		GCLK PLL	t_{CO}	1.187	1.187	2.558	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.634	2.634	5.649	ns
		GCLK PLL	t_{CO}	1.189	1.189	2.537	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.612	2.612	5.638	ns
		GCLK PLL	t_{CO}	1.167	1.167	2.526	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.616	2.616	5.644	ns
		GCLK PLL	t_{CO}	1.171	1.171	2.532	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.608	2.608	5.637	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.525	ns
1.8-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.591	2.591	5.401	ns
		GCLK PLL	t_{CO}	1.146	1.146	2.289	ns
1.8-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.593	2.593	5.412	ns
		GCLK PLL	t_{CO}	1.148	1.148	2.300	ns
1.8-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.593	2.593	5.421	ns
		GCLK PLL	t_{CO}	1.148	1.148	2.309	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.629	2.629	5.663	ns
		GCLK PLL	t_{CO}	1.187	1.187	2.557	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.633	2.633	5.641	ns
		GCLK PLL	t_{CO}	1.188	1.188	2.529	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.615	2.615	5.643	ns
		GCLK PLL	t_{CO}	1.170	1.170	2.531	ns
1.5-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.615	2.615	5.645	ns
		GCLK PLL	t_{CO}	1.170	1.170	2.533	ns
1.5-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.609	2.609	5.643	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.531	ns
1.5-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.596	2.596	5.455	ns
		GCLK PLL	t_{CO}	1.151	1.151	2.343	ns
1.5-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.599	2.599	5.465	ns
		GCLK PLL	t_{CO}	1.154	1.154	2.353	ns
1.5-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.601	2.601	5.478	ns
		GCLK PLL	t_{CO}	1.156	1.156	2.366	ns

Table 4–55. EP1AGX35 Column Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.131	1.131	2.607	ns
		t_H	–1.026	–1.026	–2.330	ns
	GCLK PLL	t_{SU}	2.573	2.573	5.713	ns
		t_H	–2.468	–2.468	–5.436	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.132	1.132	2.607	ns
		t_H	–1.027	–1.027	–2.330	ns
	GCLK PLL	t_{SU}	2.574	2.574	5.715	ns
		t_H	–2.469	–2.469	–5.438	ns
3.3-V PCI	GCLK	t_{SU}	1.256	1.256	2.903	ns
		t_H	–1.151	–1.151	–2.626	ns
	GCLK PLL	t_{SU}	2.698	2.698	6.009	ns
		t_H	–2.593	–2.593	–5.732	ns
3.3-V PCI-X	GCLK	t_{SU}	1.256	1.256	2.903	ns
		t_H	–1.151	–1.151	–2.626	ns
	GCLK PLL	t_{SU}	2.698	2.698	6.009	ns
		t_H	–2.593	–2.593	–5.732	ns
LVDS	GCLK	t_{SU}	1.106	1.106	2.489	ns
		t_H	–1.001	–1.001	–2.212	ns
	GCLK PLL	t_{SU}	2.530	2.530	5.564	ns
		t_H	–2.425	–2.425	–5.287	ns

Table 4–56 lists I/O timing specifications.

Table 4–56. EP1AGX35 Row Pins Output Timing Parameters (Part 1 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	2.904	2.904	6.699	ns
		GCLK PLL	t_{CO}	1.485	1.485	3.627	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.776	2.776	6.059	ns
		GCLK PLL	t_{CO}	1.357	1.357	2.987	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.720	2.720	6.022	ns
		GCLK PLL	t_{CO}	1.301	1.301	2.950	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.776	2.776	6.059	ns
		GCLK PLL	t_{CO}	1.357	1.357	2.987	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.670	2.670	5.753	ns
		GCLK PLL	t_{CO}	1.251	1.251	2.681	ns
2.5 V	4 mA	GCLK	t_{CO}	2.759	2.759	6.033	ns
		GCLK PLL	t_{CO}	1.340	1.340	2.961	ns

Table 4–59 lists column pin delay adders when using the regional clock in Arria GX devices.

Table 4–59. EP1AGX35 Column Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.099	0.099	0.254	ns
RCLK PLL input adder	–0.012	–0.012	–0.01	ns
RCLK output adder	–0.086	–0.086	–0.244	ns
RCLK PLL output adder	1.253	1.253	3.133	ns

EP1AGX50 I/O Timing Parameters

Table 4–60 through Table 4–63 list the maximum I/O timing parameters for EP1AGX50 devices for I/O standards which support general purpose I/O pins.

Table 4–60 lists I/O timing specifications.

Table 4–60. EP1AGX50 Row Pins Input Timing Parameters (Part 1 of 2)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.550	1.550	3.542	ns
		t_H	–1.445	–1.445	–3.265	ns
	GCLK PLL	t_{SU}	2.978	2.978	6.626	ns
		t_H	–2.873	–2.873	–6.349	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.550	1.550	3.542	ns
		t_H	–1.445	–1.445	–3.265	ns
	GCLK PLL	t_{SU}	2.978	2.978	6.626	ns
		t_H	–2.873	–2.873	–6.349	ns
2.5 V	GCLK	t_{SU}	1.562	1.562	3.523	ns
		t_H	–1.457	–1.457	–3.246	ns
	GCLK PLL	t_{SU}	2.990	2.990	6.607	ns
		t_H	–2.885	–2.885	–6.330	ns
1.8 V	GCLK	t_{SU}	1.628	1.628	3.730	ns
		t_H	–1.523	–1.523	–3.453	ns
	GCLK PLL	t_{SU}	3.056	3.056	6.814	ns
		t_H	–2.951	–2.951	–6.537	ns
1.5 V	GCLK	t_{SU}	1.631	1.631	3.825	ns
		t_H	–1.526	–1.526	–3.548	ns
	GCLK PLL	t_{SU}	3.059	3.059	6.909	ns
		t_H	–2.954	–2.954	–6.632	ns

Table 4–73. EP1AGX90 Column Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
1.5-V HSTL CLASS II	GCLK	t_{SU}	0.901	0.901	1.986	ns
		t_H	–0.796	–0.796	–1.709	ns
	GCLK PLL	t_{SU}	2.965	2.965	6.121	ns
		t_H	–2.860	–2.860	–5.844	ns
3.3-V PCI	GCLK	t_{SU}	1.023	1.023	2.278	ns
		t_H	–0.918	–0.918	–2.001	ns
	GCLK PLL	t_{SU}	3.087	3.087	6.413	ns
		t_H	–2.982	–2.982	–6.136	ns
3.3-V PCI-X	GCLK	t_{SU}	1.023	1.023	2.278	ns
		t_H	–0.918	–0.918	–2.001	ns
	GCLK PLL	t_{SU}	3.087	3.087	6.413	ns
		t_H	–2.982	–2.982	–6.136	ns
LVDS	GCLK	t_{SU}	0.891	0.891	1.920	ns
		t_H	–0.786	–0.786	–1.643	ns
	GCLK PLL	t_{SU}	2.963	2.963	6.066	ns
		t_H	–2.858	–2.858	–5.789	ns

Table 4–74 lists I/O timing specifications.

Table 4–74. EP1AGX90 Row Pins Output Timing Parameters (Part 1 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	3.170	3.170	7.382	ns
		GCLK PLL	t_{CO}	1.099	1.099	3.238	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	3.042	3.042	6.742	ns
		GCLK PLL	t_{CO}	0.971	0.971	2.598	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.986	2.986	6.705	ns
		GCLK PLL	t_{CO}	0.915	0.915	2.561	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	3.042	3.042	6.742	ns
		GCLK PLL	t_{CO}	0.971	0.971	2.598	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.936	2.936	6.436	ns
		GCLK PLL	t_{CO}	0.865	0.865	2.292	ns
2.5 V	4 mA	GCLK	t_{CO}	3.025	3.025	6.716	ns
		GCLK PLL	t_{CO}	0.954	0.954	2.572	ns
2.5 V	8 mA	GCLK	t_{CO}	2.922	2.922	6.458	ns
		GCLK PLL	t_{CO}	0.851	0.851	2.314	ns
2.5 V	12 mA	GCLK	t_{CO}	2.903	2.903	6.344	ns
		GCLK PLL	t_{CO}	0.832	0.832	2.200	ns

Table 4–74. EP1AGX90 Row Pins Output Timing Parameters (Part 3 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.857	2.857	6.106	ns
		GCLK PLL	t_{CO}	0.779	0.779	1.950	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.842	2.842	6.098	ns
		GCLK PLL	t_{CO}	0.764	0.764	1.942	ns
LVDS	—	GCLK	t_{CO}	2.898	2.898	6.265	ns
		GCLK PLL	t_{CO}	0.831	0.831	2.129	ns

Table 4–75 lists I/O timing specifications.

Table 4–75. EP1AGX90 Column Pins Output Timing Parameters (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	3.141	3.141	7.164	ns
		GCLK PLL	t_{CO}	1.077	1.077	3.029	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.996	2.996	6.792	ns
		GCLK PLL	t_{CO}	0.932	0.932	2.657	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.929	2.929	6.792	ns
		GCLK PLL	t_{CO}	0.865	0.865	2.657	ns
3.3-V LVTTL	16 mA	GCLK	t_{CO}	2.903	2.903	6.623	ns
		GCLK PLL	t_{CO}	0.839	0.839	2.488	ns
3.3-V LVTTL	20 mA	GCLK	t_{CO}	2.881	2.881	6.498	ns
		GCLK PLL	t_{CO}	0.817	0.817	2.363	ns
3.3-V LVTTL	24 mA	GCLK	t_{CO}	2.874	2.874	6.500	ns
		GCLK PLL	t_{CO}	0.810	0.810	2.365	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.996	2.996	6.792	ns
		GCLK PLL	t_{CO}	0.932	0.932	2.657	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.904	2.904	6.497	ns
		GCLK PLL	t_{CO}	0.840	0.840	2.362	ns
3.3-V LVCMOS	12 mA	GCLK	t_{CO}	2.876	2.876	6.419	ns
		GCLK PLL	t_{CO}	0.812	0.812	2.284	ns
3.3-V LVCMOS	16 mA	GCLK	t_{CO}	2.883	2.883	6.387	ns
		GCLK PLL	t_{CO}	0.819	0.819	2.252	ns
3.3-V LVCMOS	20 mA	GCLK	t_{CO}	2.870	2.870	6.369	ns
		GCLK PLL	t_{CO}	0.806	0.806	2.234	ns
3.3-V LVCMOS	24 mA	GCLK	t_{CO}	2.859	2.859	6.347	ns
		GCLK PLL	t_{CO}	0.795	0.795	2.212	ns
2.5 V	4 mA	GCLK	t_{CO}	2.958	2.958	6.824	ns
		GCLK PLL	t_{CO}	0.894	0.894	2.689	ns

Table 4–75. EP1AGX90 Column Pins Output Timing Parameters (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
2.5 V	8 mA	GCLK	t_{CO}	2.906	2.906	6.562	ns
		GCLK PLL	t_{CO}	0.842	0.842	2.427	ns
2.5 V	12 mA	GCLK	t_{CO}	2.885	2.885	6.445	ns
		GCLK PLL	t_{CO}	0.821	0.821	2.310	ns
2.5 V	16 mA	GCLK	t_{CO}	2.867	2.867	6.371	ns
		GCLK PLL	t_{CO}	0.803	0.803	2.236	ns
1.8 V	2 mA	GCLK	t_{CO}	2.998	2.998	7.816	ns
		GCLK PLL	t_{CO}	0.934	0.934	3.681	ns
1.8 V	4 mA	GCLK	t_{CO}	3.003	3.003	7.042	ns
		GCLK PLL	t_{CO}	0.939	0.939	2.907	ns
1.8 V	6 mA	GCLK	t_{CO}	2.927	2.927	6.778	ns
		GCLK PLL	t_{CO}	0.863	0.863	2.643	ns
1.8 V	8 mA	GCLK	t_{CO}	2.929	2.929	6.687	ns
		GCLK PLL	t_{CO}	0.865	0.865	2.552	ns
1.8 V	10 mA	GCLK	t_{CO}	2.883	2.883	6.610	ns
		GCLK PLL	t_{CO}	0.819	0.819	2.475	ns
1.8 V	12 mA	GCLK	t_{CO}	2.884	2.884	6.553	ns
		GCLK PLL	t_{CO}	0.820	0.820	2.418	ns
1.5 V	2 mA	GCLK	t_{CO}	2.978	2.978	7.346	ns
		GCLK PLL	t_{CO}	0.914	0.914	3.211	ns
1.5 V	4 mA	GCLK	t_{CO}	2.914	2.914	6.777	ns
		GCLK PLL	t_{CO}	0.850	0.850	2.642	ns
1.5 V	6 mA	GCLK	t_{CO}	2.917	2.917	6.659	ns
		GCLK PLL	t_{CO}	0.853	0.853	2.524	ns
1.5 V	8 mA	GCLK	t_{CO}	2.876	2.876	6.606	ns
		GCLK PLL	t_{CO}	0.812	0.812	2.471	ns
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.859	2.859	6.381	ns
		GCLK PLL	t_{CO}	0.797	0.797	2.250	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.842	2.842	6.331	ns
		GCLK PLL	t_{CO}	0.780	0.780	2.200	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.820	2.820	6.258	ns
		GCLK PLL	t_{CO}	0.758	0.758	2.127	ns
SSTL-2 CLASS II	20 mA	GCLK	t_{CO}	2.821	2.821	6.245	ns
		GCLK PLL	t_{CO}	0.759	0.759	2.114	ns
SSTL-2 CLASS II	24 mA	GCLK	t_{CO}	2.817	2.817	6.243	ns
		GCLK PLL	t_{CO}	0.755	0.755	2.112	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.858	2.858	6.356	ns
		GCLK PLL	t_{CO}	0.794	0.794	2.221	ns

Table 4–107. Arria GX Maximum Output Clock Rate for Dedicated Clock Pins (Part 2 of 4)

I/O Standards	Drive Strength	–6 Speed Grade	Units
SSTL-2 CLASS I	8 mA	280	MHz
	12 mA	327	MHz
SSTL-2 CLASS II	16 mA	280	MHz
	20 mA	327	MHz
	24 mA	327	MHz
SSTL-18 CLASS I	4 mA	140	MHz
	6 mA	186	MHz
	8 mA	280	MHz
	10 mA	373	MHz
	12 mA	373	MHz
SSTL-18 CLASS II	8 mA	140	MHz
	16 mA	327	MHz
	18 mA	373	MHz
	20 mA	420	MHz
1.8-V HSTL CLASS I	4 mA	280	MHz
	6 mA	420	MHz
	8 mA	561	MHz
	10 mA	561	MHz
	12 mA	607	MHz
1.8-V HSTL CLASS II	16 mA	420	MHz
	18 mA	467	MHz
	20 mA	514	MHz
1.5-V HSTL CLASS I	4 mA	280	MHz
	6 mA	420	MHz
	8 mA	561	MHz
	10mA	607	MHz
	12 mA	654	MHz
1.5-V HSTL CLASS II	16 mA	514	MHz
	18 mA	561	MHz
	20 mA	561	MHz
	24 mA	278	MHz
DIFFERENTIAL SSTL-2	8 mA	280	MHz
	12 mA	327	MHz
DIFFERENTIAL 2.5-V SSTL CLASS II	16 mA	280	MHz
	20 mA	327	MHz
	24 mA	327	MHz