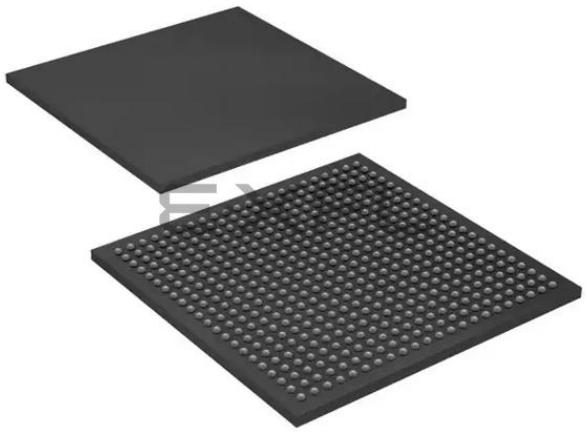

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1676
Number of Logic Elements/Cells	33520
Total RAM Bits	1348416
Number of I/O	230
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1agx35cf484i6

Table 1–1. Arria GX Device Features (Part 2 of 2)

Feature	EP1AGX20C	EP1AGX35C/D		EP1AGX50C/D		EP1AGX60C/D/E			EP1AGX90E
	C	C	D	C	D	C	D	E	E
Source-synchronous transmit channels	29	29	29	29	29, 42	29	29	42	45
M512 RAM blocks (32 × 18 bits)	166	197		313		326			478
M4K RAM blocks (128 × 36 bits)	118	140		242		252			400
M-RAM blocks (4096 × 144 bits)	1	1		2		2			4
Total RAM bits	1,229,184	1,348,416		2,475,072		2,528,640			4,477,824
Embedded multipliers (18 × 18)	40	56		104		128			176
DSP blocks	10	14		26		32			44
PLLs	4	4		4	4, 8	4		8	8
Maximum user I/O pins	230, 341	230	341	229	350, 514	229	350	514	538

Arria GX devices are available in space-saving FBGA packages (refer to Table 1–2). All Arria GX devices support vertical migration within the same package. With vertical migration support, designers can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities. For I/O pin migration across densities, the designer must cross-reference the available I/O pins with the device pin-outs for all planned densities of a given package type to identify which I/O pins are migratable.

Table 1–2. Arria GX Package Options (Pin Counts and Transceiver Channels) (Part 1 of 2)

Device	Transceiver Channels	Source-Synchronous Channels		Maximum User I/O Pin Count		
		Receive	Transmit	484-Pin FBGA (23 mm)	780-Pin FBGA (29 mm)	1152-Pin FBGA (35 mm)
EP1AGX20C	4	31	29	230	341	—
EP1AGX35C	4	31	29	230	—	—
EP1AGX50C	4	31	29	229	—	—
EP1AGX60C	4	31	29	229	—	—
EP1AGX35D	8	31	29	—	341	—
EP1AGX50D	8	31, 42	29, 42	—	350	514

In GIGE and Serial RapidIO modes, you can dynamically put each transceiver channel individually in serial loopback by controlling the `rx_seriallpbken` port. A high on the `rx_seriallpbken` port puts the transceiver into serial loopback and a low takes the transceiver out of serial loopback.

As seen in Figure 2–18, the serial data output from the transmitter serializer is looped back to the receiver CRU in serial loopback. The transmitter data path from the PLD interface to the serializer in serial loopback is the same as in non-loopback mode. The receiver data path from the clock recovery unit to the PLD interface in serial loopback is the same as in non-loopback mode. Because the entire transceiver data path is available in serial loopback, this option is often used to diagnose the data path as a probable cause of link errors.

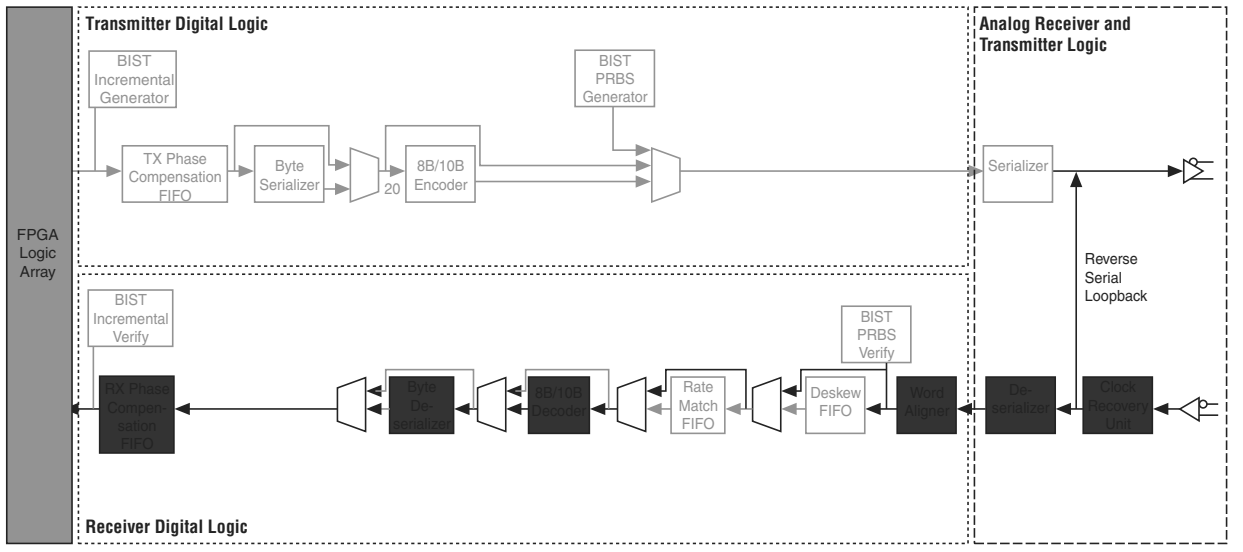
☞ When serial loopback is enabled, the transmitter output buffer is still active and drives the serial data out on the `tx_dataout` port.

Reverse Serial Loopback

Reverse serial loopback mode uses the analog portion of the transceiver. An external source (pattern generator or transceiver) generates the source data. The high-speed serial source data arrives at the high-speed differential receiver input buffer, passes through the CRU unit and the retimed serial data is looped back, and is transmitted though the high-speed differential transmitter output buffer.

Figure 2–19 shows the data path in reverse serial loopback mode.

Figure 2–19. Arria GX Block in Reverse Serial Loopback Mode



For more information about transceiver clocking in all supported functional modes, refer to the *Arria GX Transceiver Architecture* chapter.

PLD Clock Utilization by Transceiver Blocks

Arria GX devices have up to 16 global clock (GCLK) lines and 16 regional clock (RCLK) lines that are used to route the transceiver clocks. The following transceiver clocks use the available global and regional clock resources:

- `pll_inclk` (if driven from an FPGA input pin)
- `rx_cruclk` (if driven from an FPGA input pin)
- `tx_clkout/coreclkout` (CMU low-speed parallel clock forwarded to the PLD)
- Recovered clock from each channel (`rx_clkout`) in non-rate matcher mode
- Calibration clock (`cal_blk_clk`)
- Fixed clock (`fixedclk` used for receiver detect circuitry in PCI Express [PIPE] mode only)

Figure 2–23 and Figure 2–24 show the available GCLK and RCLK resources in Arria GX devices.

Figure 2–23. Global Clock Resources in Arria GX Devices

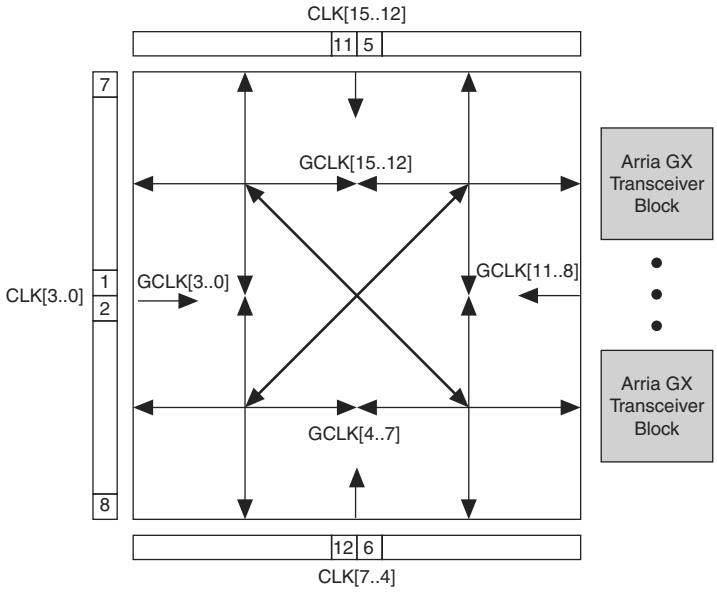
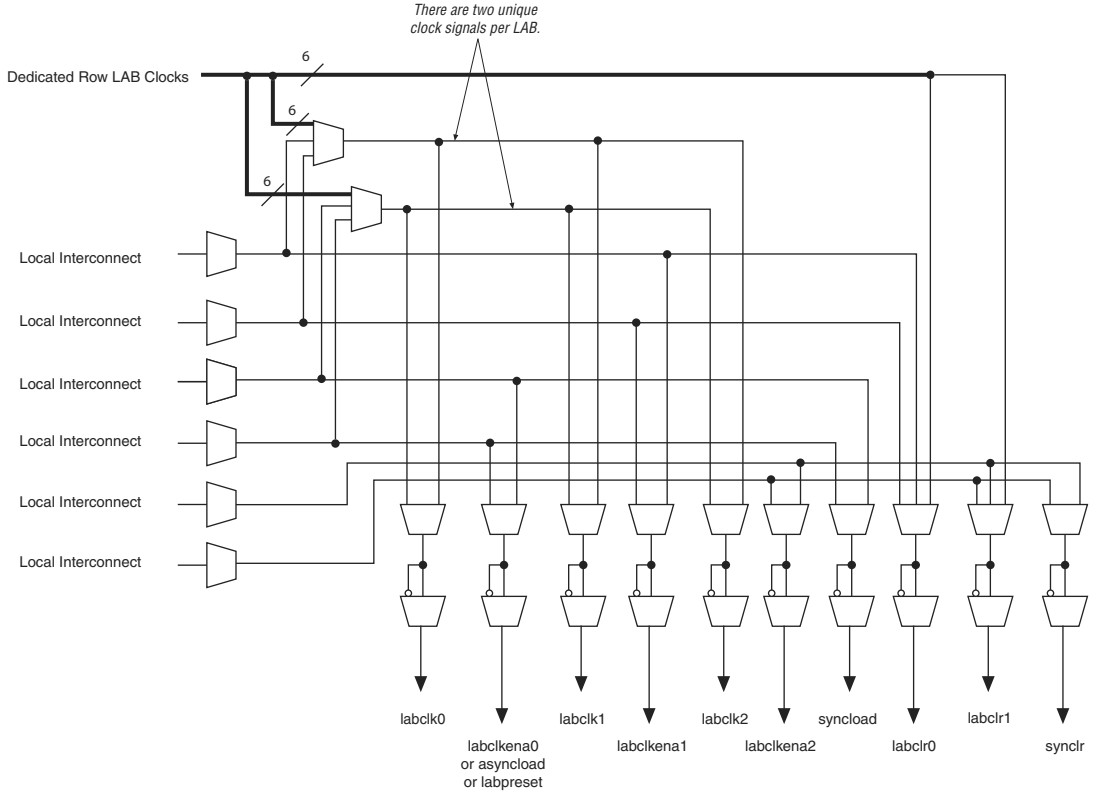


Figure 2–27 shows the LAB control signal generation circuit.

Figure 2–27. LAB-Wide Control Signals

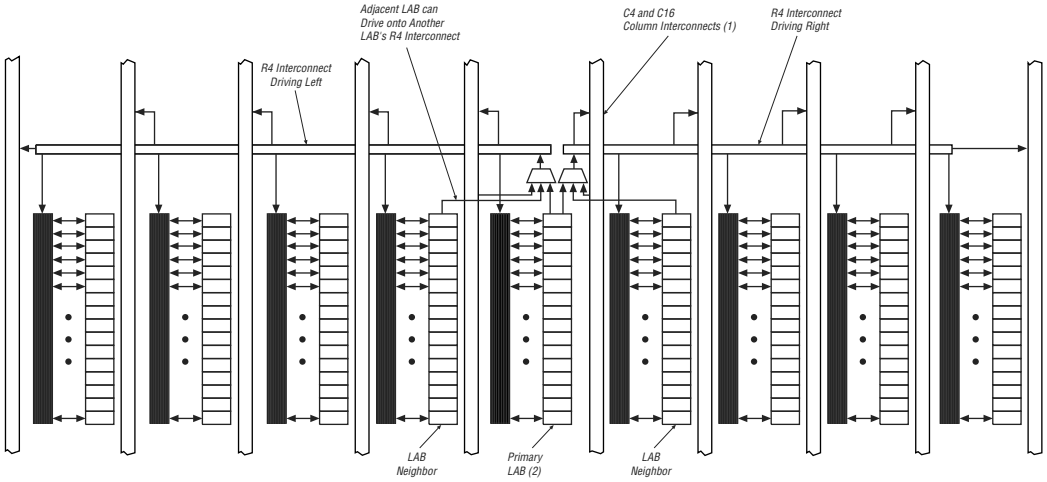


Adaptive Logic Modules

The basic building block of logic in the Arria GX architecture is the ALM. The ALM provides advanced features with efficient logic utilization. Each ALM contains a variety of look-up table (LUT)-based resources that can be divided between two adaptive LUTs (ALUTs). With up to eight inputs to the two ALUTs, one ALM can implement various combinations of two functions. This adaptability allows the ALM to be completely backward-compatible with four-input LUT architectures. One ALM can also implement any function of up to six inputs and certain seven-input functions.

In addition to the adaptive LUT-based resources, each ALM contains two programmable registers, two dedicated full adders, a carry chain, a shared arithmetic chain, and a register chain. Through these dedicated resources, the ALM can efficiently implement various arithmetic functions and shift registers. Each ALM drives all types of interconnects: local, row, column, carry chain, shared arithmetic chain, register chain, and direct link interconnects. Figure 2–28 shows a high-level block diagram of the Arria GX ALM while Figure 2–29 shows a detailed view of all the connections in the ALM.

Figure 2–39. R4 Interconnect Connections *(Note 1), (2), (3)*



Notes to Figure 2–39:

(1) C4 and C16 interconnects can drive R4 interconnects.

(2) This pattern is repeated for every LAB in the LAB row.

(3) The LABs in Figure 2–39 show the 16 possible logical outputs per LAB.

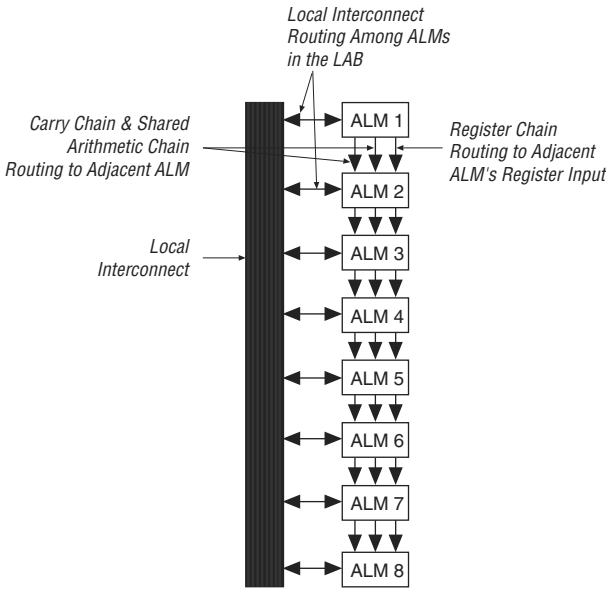
R24 row interconnects span 24 LABs and provide the fastest resource for long row connections between LABs, TriMatrix memory, DSP blocks, and row IOEs. The R24 row interconnects can cross M-RAM blocks. R24 row interconnects drive to other row or column interconnects at every fourth LAB and do not drive directly to LAB local interconnects. R24 row interconnects drive LAB local interconnects via R4 and C4 interconnects. R24 interconnects can drive R24, R4, C16, and C4 interconnects. The column interconnect operates similarly to the row interconnect and vertically routes signals to and from LABs, TriMatrix memory, DSP blocks, and IOEs. Each column of LABs is served by a dedicated column interconnect.

These column resources include:

- Shared arithmetic chain interconnects in a LAB
- Carry chain interconnects in a LAB and from LAB to LAB
- Register chain interconnects in a LAB
- C4 interconnects traversing a distance of four blocks in up and down direction
- C16 column interconnects for high-speed vertical routing through the device

Arria GX devices include an enhanced interconnect structure in LABs for routing shared arithmetic chains and carry chains for efficient arithmetic functions. The register chain connection allows the register output of one ALM to connect directly to the register input of the next ALM in the LAB for fast shift registers. These ALM-to-ALM connections bypass the local interconnect. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–40 shows shared arithmetic chain, carry chain, and register chain interconnects.

Figure 2–40. Shared Arithmetic Chain, Carry Chain and Register Chain Interconnects



C4 interconnects span four LABs, M512, or M4K blocks up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. Figure 2–41 shows the C4 interconnect connections from a LAB in a column. C4 interconnects can drive and be driven by all types of architecture blocks, including DSP blocks, TriMatrix memory blocks, and column and row IOEs. For LAB interconnection, a primary LAB or its LAB neighbor can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

Figure 2–49. M-RAM Row Unit Interface to Interconnect

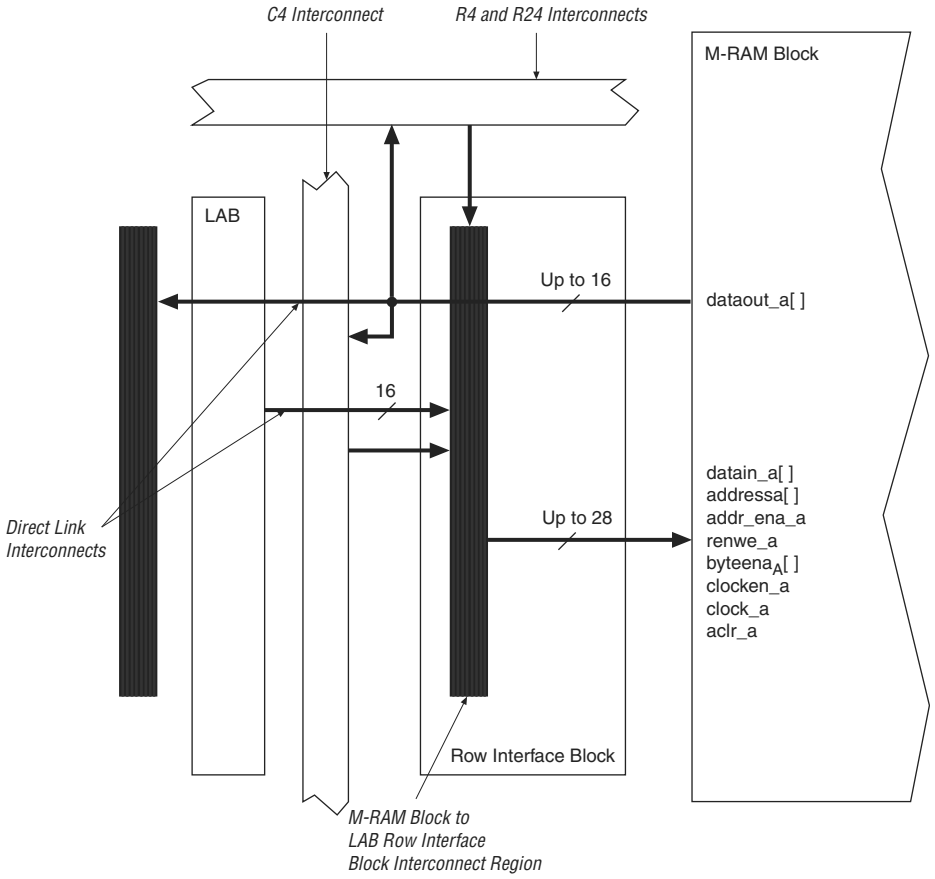


Table 2–12 lists the input and output data signal connections along with the address and control signal input connections to the row unit interfaces (L0 to L5 and R0 to R5).

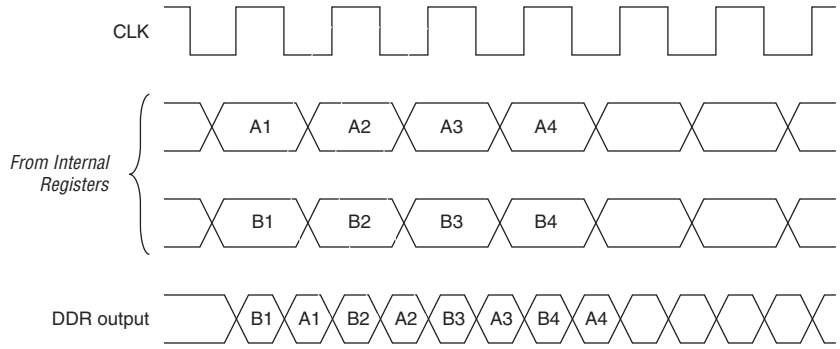
Table 2–12. M-RAM Row Interface Unit Signals (Part 1 of 2)

Unit Interface Block	Input Signals	Output Signals
L0	datain_a[14..0] byteena_a[1..0]	dataout_a[11..0]
L1	datain_a[29..15] byteena_a[3..2]	dataout_a[23..12]
L2	datain_a[35..30] addressa[4..0] addr_ena_a clock_a clocken_a renwe_a aclr_a	dataout_a[35..24]
L3	addressa[15..5] datain_a[41..36]	dataout_a[47..36]

Table 2–15. DSP Block Signal Sources and Destinations

LAB Row at Interface	Control Signals Generated	Data Inputs	Data Outputs
0	clock0 aclr0 ena0 mult01_saturate addnsub1_round/ accum_round addnsub1 signa sourcea sourceb	A1[17..0] B1[17..0]	OA[17..0] OB[17..0]
1	clock1 aclr1 ena1 accum_saturate mult01_round accum_sload sourcea sourceb mode0	A2[17..0] B2[17..0]	OC[17..0] OD[17..0]
2	clock2 aclr2 ena2 mult23_saturate addnsub3_round/ accum_round addnsub3 sign_b sourcea sourceb	A3[17..0] B3[17..0]	OE[17..0] OF[17..0]
3	clock3 aclr3 ena3 accum_saturate mult23_round accum_sload sourcea sourceb mode1	A4[17..0] B4[17..0]	OG[17..0] OH[17..0]

Figure 2–76. Output Timing Diagram in DDR Mode



The Arria GX IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations. The negative-edge-clocked OE register holds the OE signal inactive until the falling edge of the clock to meet DDR SDRAM timing requirements.

External RAM Interfacing

In addition to the six I/O registers in each IOE, Arria GX devices also have dedicated phase-shift circuitry for interfacing with external memory interfaces, including DDR, DDR2 SDRAM, and SDR SDRAM. In every Arria GX device, the I/O banks at the top (Banks 3 and 4) and bottom (Banks 7 and 8) of the device support DQ and DQS signals with DQ bus modes of ×4, ×8/×9, ×16/×18, or ×32/×36. Table 2–23 shows the number of DQ and DQS buses that are supported per device.

Table 2–23. DQS and DQ Bus Mode Support *(Note 1)*

Device	Package	Number of ×4 Groups	Number of ×8/×9 Groups	Number of ×16/×18 Groups	Number of ×32/×36 Groups
EP1AGX20	484-pin FineLine BGA	2	0	0	0
EP1AGX35	484-pin FineLine BGA	2	0	0	0
	780-pin FineLine BGA	18	8	4	0
EP1AGX50/60	484-pin FineLine BGA	2	0	0	0
	780-pin FineLine BGA	18	8	4	0
	1,152-pin FineLine BGA	36	18	8	4
EP1AGX90	1,152-pin FineLine BGA	36	18	8	4

Note to Table 2–23:

(1) Numbers are preliminary until devices are available.

A compensated delay element on each DQS pin automatically aligns input DQS synchronization signals with the data window of their corresponding DQ data signals. The DQS signals drive a local DQS bus in the top and bottom I/O banks. This DQS bus is an additional resource to the I/O clocks and is used to clock DQ input registers with the DQS signal.

Table 2–24 shows the possible settings for I/O standards with drive strength control.

Table 2–24. Programmable Drive Strength *(Note 1)*

I/O Standard	I_{OH} / I_{OL} Current Strength Setting (mA) for Column I/O Pins	I_{OH} / I_{OL} Current Strength Setting (mA) for Row I/O Pins
3.3-V LVTTL	24, 20, 16, 12, 8, 4	12, 8, 4
3.3-V LVCMOS	24, 20, 16, 12, 8, 4	8, 4
2.5-V LVTTL/LVCMOS	16, 12, 8, 4	12, 8, 4
1.8-V LVTTL/LVCMOS	12, 10, 8, 6, 4, 2	8, 6, 4, 2
1.5-V LVCMOS	8, 6, 4, 2	4, 2
SSTL-2 Class I	12, 8	12, 8
SSTL-2 Class II	24, 20, 16	16
SSTL-18 Class I	12, 10, 8, 6, 4	10, 8, 6, 4
SSTL-18 Class II	20, 18, 16, 8	—
HSTL-18 Class I	12, 10, 8, 6, 4	12, 10, 8, 6, 4
HSTL-18 Class II	20, 18, 16	—
HSTL-15 Class I	12, 10, 8, 6, 4	8, 6, 4
HSTL-15 Class II	20, 18, 16	—

Note to Table 2–24:

(1) The Quartus II software default current setting is the maximum setting for each I/O standard.

Open-Drain Output

Arria GX devices provide an optional open-drain (equivalent to an open collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (for example, interrupt and write enable signals) that can be asserted by any of several devices.

Bus Hold

Each Arria GX device I/O pin provides an optional bus-hold feature. Bus-hold circuitry can hold the signal on an I/O pin at its last-driven state. Because the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not needed to hold a signal level when the bus is tri-stated.

Bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output drives no higher than V_{CCIO} to prevent overdriving signals. If the bus-hold feature is enabled, the programmable pull-up option cannot be used. Disable the bus-hold feature when the I/O pin has been configured for differential signals.

Bus-hold circuitry uses a resistor with a nominal resistance (RBH) of approximately 7 kΩ to pull the signal level to the last-driven state. This information is provided for each V_{CCIO} voltage level. Bus-hold circuitry is active only after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

Arria GX devices provide two types of termination:

- On-chip differential termination (R_D OCT)
- On-chip series termination (R_S OCT)

Table 2–26 lists the Arria GX OCT support per I/O bank.

Table 2–26. On-Chip Termination Support by I/O Banks

On-Chip Termination Support	I/O Standard Support	Top and Bottom Banks (3, 4, 7, 8)	Left Bank (1, 2)
Series termination	3.3-V LVTTL	✓	✓
	3.3-V LVCMOS	✓	✓
	2.5-V LVTTL	✓	✓
	2.5-V LVCMOS	✓	✓
	1.8-V LVTTL	✓	✓
	1.8-V LVCMOS	✓	✓
	1.5-V LVTTL	✓	✓
	1.5-V LVCMOS	✓	✓
	SSTL-2 class I and II	✓	✓
	SSTL-18 class I	✓	✓
	SSTL-18 class II	✓	—
	1.8-V HSTL class I	✓	✓
	1.8-V HSTL class II	✓	—
	1.5-V HSTL class I	✓	✓
	1.2-V HSTL	✓	—
Differential termination *(1)*	LVDS	—	✓
	HyperTransport technology	—	✓

Note to Table 2–26:

(1) Clock pins `CLK1` and `CLK3`, and pins `FPLL[7..8]CLK` do not support differential on-chip termination. Clock pins `CLK0` and `CLK2`, do support differential on-chip termination. Clock pins in the top and bottom banks (`CLK[4..7, 12..15]`) do not support differential on-chip termination.

On-Chip Differential Termination (R_D OCT)

Arria GX devices support internal differential termination with a nominal resistance value of 100 Ω for LVDS input receiver buffers. LVPECL input signals (supported on clock pins only) require an external termination resistor. R_D OCT is supported across the full range of supported differential data rates as shown in the *High-Speed I/O Specifications* section of the *DC & Switching Characteristics* chapter.

For more information about R_D OCT, refer to the *High-Speed Differential I/O Interfaces with DPA in Arria GX Devices* chapter.

For more information about tolerance specifications for R_D OCT, refer to the *DC & Switching Characteristics* chapter.

The Arria GX device instruction register length is 10 bits and the USERCODE register length is 32 bits. Table 3–2 and Table 3–3 show the boundary-scan register length and device IDCODE information for Arria GX devices.

Table 3–2. Arria GX Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP1AGX20	1320
EP1AGX35	1320
EP1AGX50	1668
EP1AGX60	1668
EP1AGX90	2016

Table 3–3. 2-Bit Arria GX Device IDCODE

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit)
EP1AGX20	0000	0010 0001 0010 0001	000 0110 1110	1
EP1AGX35	0000	0010 0001 0010 0001	000 0110 1110	1
EP1AGX50	0000	0010 0001 0010 0010	000 0110 1110	1
EP1AGX60	0000	0010 0001 0010 0010	000 0110 1110	1
EP1AGX90	0000	0010 0001 0010 0011	000 0110 1110	1

SignalTap II Embedded Logic Analyzer

Arria GX devices feature the SignalTap II embedded logic analyzer, which monitors design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry. You can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages, such as FineLine BGA (FBGA) packages, because it can be difficult to add a connection to a pin during the debugging process after a board is designed and manufactured.

Configuration

The logic, circuitry, and interconnects in the Arria GX architecture are configured with CMOS SRAM elements. Altera® FPGAs are reconfigurable and every device is tested with a high coverage production test program so you do not have to perform fault testing and can instead focus on simulation and design verification.

Arria GX devices are configured at system power up with data stored in an Altera configuration device or provided by an external controller (for example, a MAX® II device or microprocessor). You can configure Arria GX devices using the fast passive parallel (FPP), active serial (AS), passive serial (PS), passive parallel asynchronous (PPA), and JTAG configuration schemes. Each Arria GX device has an optimized interface that allows microprocessors to configure it serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat Arria GX devices as memory and configure them by writing to a virtual memory location, making reconfiguration easy.

Figure 4–1. Lock Time Parameters for Manual Mode

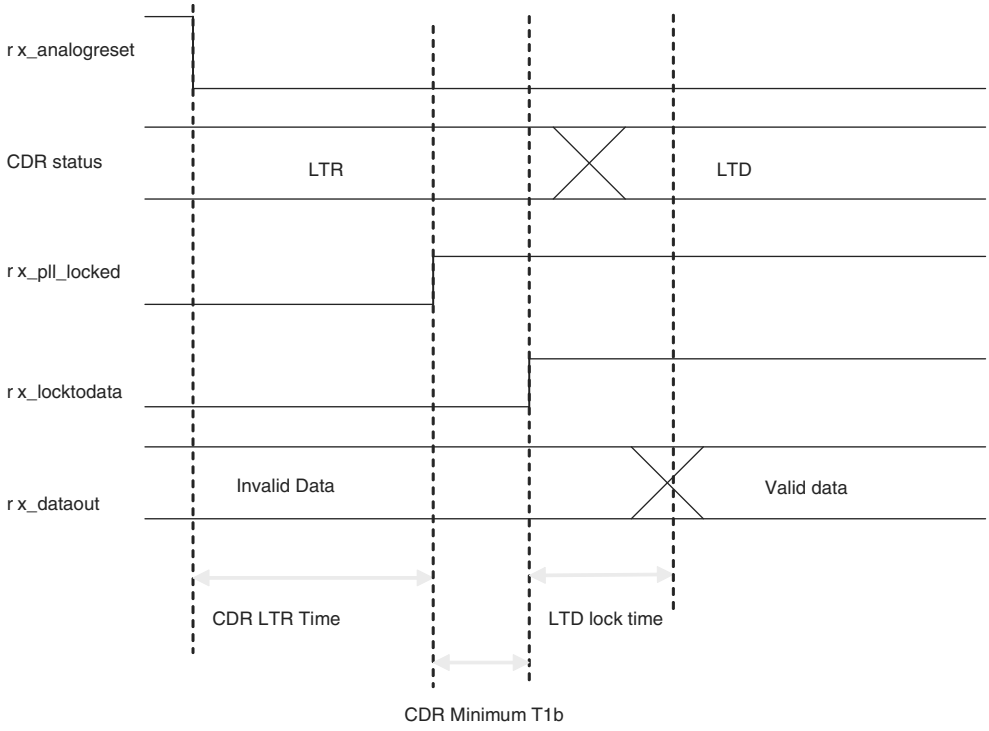


Figure 4–2. Lock Time Parameters for Automatic Mode

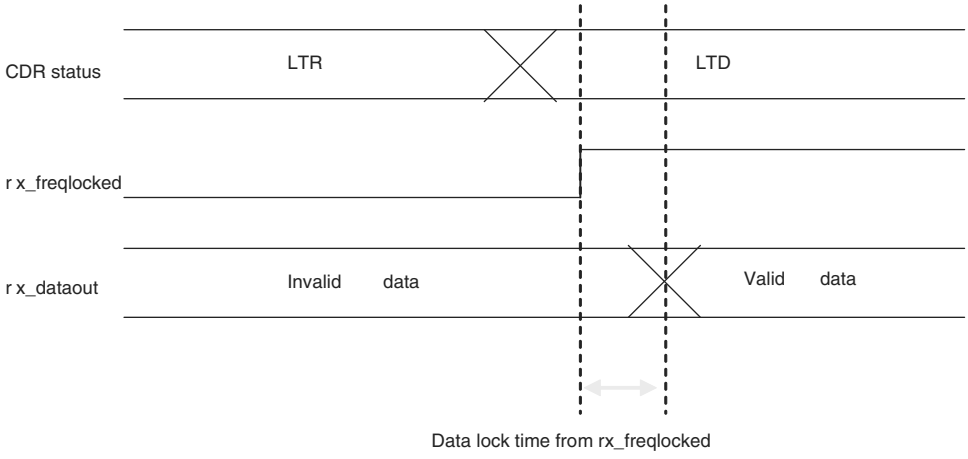


Table 4–7. Arria GX Transceiver Block AC Specification *(Note 1), (2), (3)* (Part 2 of 4)

Description	Condition	–6 Speed Grade Commercial & Industrial	Units
Deterministic jitter at 3.125 Gbps	REFCLK = 156.25 MHz Pattern = CJPAT V_{OD} = 1200 mV No Pre-emphasis	0.17	UI
XAUI Receiver Jitter Tolerance *(4)*			
Total jitter	Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.65	UI
Deterministic jitter	Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.37	UI
Peak-to-peak jitter	Jitter frequency = 22.1 KHz	> 8.5	UI
Peak-to-peak jitter	Jitter frequency = 1.875 MHz	> 0.1	UI
Peak-to-peak jitter	Jitter frequency = 20 MHz	> 0.1	UI
PCI Express (PIPE) Transmitter Jitter Generation *(5)*			
Total Transmitter Jitter Generation	Compliance Pattern; V_{OD} = 800 mV; Pre-emphasis = 49%	< 0.25	UI p-p
PCI Express (PIPE) Receiver Jitter Tolerance *(5)*			
Total Receiver Jitter Tolerance	Compliance Pattern; DC Gain = 3 db	> 0.6	UI p-p
Gigabit Ethernet (GIGE) Transmitter Jitter Generation *(7)*			
Total Transmitter Jitter Generation (TJ)	CRPAT: V_{OD} = 800 mV; Pre-emphasis = 0%	< 0.279	UI p-p
Deterministic Transmitter Jitter Generation (DJ)	CRPAT; V_{OD} = 800 mV; Pre-emphasis = 0%	< 0.14	UI p-p
Gigabit Ethernet (GIGE) Receiver Jitter Tolerance			
Total Jitter Tolerance	CJPAT Compliance Pattern; DC Gain = 0 dB	> 0.66	UI p-p
Deterministic Jitter Tolerance	CJPAT Compliance Pattern; DC Gain = 0 dB	> 0.4	UI p-p
Serial RapidIO (1.25 Gbps, 2.5 Gbps, and 3.125 Gbps) Transmitter Jitter Generation *(6)*			
Total Transmitter Jitter Generation (TJ)	CJPAT Compliance Pattern; V_{OD} = 800 mV; Pre-emphasis = 0%	< 0.35	UI p-p
Deterministic Transmitter Jitter Generation (DJ)	CJPAT Compliance Pattern; V_{OD} = 800 mV; Pre-emphasis = 0%	< 0.17	UI p-p

Table 4–51. EP1AGX20 Column Pins Output Timing Parameters (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
1.8 V	6 mA	GCLK	t_{CO}	2.695	2.695	6.155	ns
		GCLK PLL	t_{CO}	1.253	1.253	3.049	ns
1.8 V	8 mA	GCLK	t_{CO}	2.697	2.697	6.064	ns
		GCLK PLL	t_{CO}	1.255	1.255	2.958	ns
1.8 V	10 mA	GCLK	t_{CO}	2.651	2.651	5.987	ns
		GCLK PLL	t_{CO}	1.209	1.209	2.881	ns
1.8 V	12 mA	GCLK	t_{CO}	2.652	2.652	5.930	ns
		GCLK PLL	t_{CO}	1.210	1.210	2.824	ns
1.5 V	2 mA	GCLK	t_{CO}	2.746	2.746	6.723	ns
		GCLK PLL	t_{CO}	1.304	1.304	3.617	ns
1.5 V	4 mA	GCLK	t_{CO}	2.682	2.682	6.154	ns
		GCLK PLL	t_{CO}	1.240	1.240	3.048	ns
1.5 V	6 mA	GCLK	t_{CO}	2.685	2.685	6.036	ns
		GCLK PLL	t_{CO}	1.243	1.243	2.930	ns
1.5 V	8 mA	GCLK	t_{CO}	2.644	2.644	5.983	ns
		GCLK PLL	t_{CO}	1.202	1.202	2.877	ns
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.629	2.629	5.762	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.650	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.612	2.612	5.712	ns
		GCLK PLL	t_{CO}	1.167	1.167	2.600	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.590	2.590	5.639	ns
		GCLK PLL	t_{CO}	1.145	1.145	2.527	ns
SSTL-2 CLASS II	20 mA	GCLK	t_{CO}	2.591	2.591	5.626	ns
		GCLK PLL	t_{CO}	1.146	1.146	2.514	ns
SSTL-2 CLASS II	24 mA	GCLK	t_{CO}	2.587	2.587	5.624	ns
		GCLK PLL	t_{CO}	1.142	1.142	2.512	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.626	2.626	5.733	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.627	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.630	2.630	5.694	ns
		GCLK PLL	t_{CO}	1.185	1.185	2.582	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.609	2.609	5.675	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.563	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.614	2.614	5.673	ns
		GCLK PLL	t_{CO}	1.169	1.169	2.561	ns
SSTL-18 CLASS I	12 mA	GCLK	t_{CO}	2.608	2.608	5.659	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.547	ns
SSTL-18 CLASS II	8 mA	GCLK	t_{CO}	2.597	2.597	5.625	ns
		GCLK PLL	t_{CO}	1.152	1.152	2.513	ns

Table 4–55. EP1AGX35 Column Pins Input Timing Parameters (Part 2 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
2.5 V	GCLK	t_{SU}	1.261	1.261	2.897	ns
		t_H	–1.156	–1.156	–2.620	ns
	GCLK PLL	t_{SU}	2.703	2.703	6.003	ns
		t_H	–2.598	–2.598	–5.726	ns
1.8 V	GCLK	t_{SU}	1.327	1.327	3.107	ns
		t_H	–1.222	–1.222	–2.830	ns
	GCLK PLL	t_{SU}	2.769	2.769	6.213	ns
		t_H	–2.664	–2.664	–5.936	ns
1.5 V	GCLK	t_{SU}	1.330	1.330	3.200	ns
		t_H	–1.225	–1.225	–2.923	ns
	GCLK PLL	t_{SU}	2.772	2.772	6.306	ns
		t_H	–2.667	–2.667	–6.029	ns
SSTL-2 CLASS I	GCLK	t_{SU}	1.075	1.075	2.372	ns
		t_H	–0.970	–0.970	–2.095	ns
	GCLK PLL	t_{SU}	2.517	2.517	5.480	ns
		t_H	–2.412	–2.412	–5.203	ns
SSTL-2 CLASS II	GCLK	t_{SU}	1.075	1.075	2.372	ns
		t_H	–0.970	–0.970	–2.095	ns
	GCLK PLL	t_{SU}	2.517	2.517	5.480	ns
		t_H	–2.412	–2.412	–5.203	ns
SSTL-18 CLASS I	GCLK	t_{SU}	1.113	1.113	2.479	ns
		t_H	–1.008	–1.008	–2.202	ns
	GCLK PLL	t_{SU}	2.555	2.555	5.585	ns
		t_H	–2.450	–2.450	–5.308	ns
SSTL-18 CLASS II	GCLK	t_{SU}	1.114	1.114	2.479	ns
		t_H	–1.009	–1.009	–2.202	ns
	GCLK PLL	t_{SU}	2.556	2.556	5.587	ns
		t_H	–2.451	–2.451	–5.310	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	1.113	1.113	2.479	ns
		t_H	–1.008	–1.008	–2.202	ns
	GCLK PLL	t_{SU}	2.555	2.555	5.585	ns
		t_H	–2.450	–2.450	–5.308	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	1.114	1.114	2.479	ns
		t_H	–1.009	–1.009	–2.202	ns
	GCLK PLL	t_{SU}	2.556	2.556	5.587	ns
		t_H	–2.451	–2.451	–5.310	ns

Table 4–63. EP1AGX50 Column Pins Output Timing Parameters (Part 4 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
1.8-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.602	2.602	5.574	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.314	ns
1.8-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.604	2.604	5.578	ns
		GCLK PLL	t_{CO}	1.166	1.166	2.325	ns
1.8-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.604	2.604	5.577	ns
		GCLK PLL	t_{CO}	1.166	1.166	2.334	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.637	2.637	5.675	ns
		GCLK PLL	t_{CO}	1.196	1.196	2.569	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.644	2.644	5.651	ns
		GCLK PLL	t_{CO}	1.206	1.206	2.554	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.626	2.626	5.653	ns
		GCLK PLL	t_{CO}	1.188	1.188	2.556	ns
1.5-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.626	2.626	5.655	ns
		GCLK PLL	t_{CO}	1.188	1.188	2.558	ns
1.5-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.620	2.620	5.653	ns
		GCLK PLL	t_{CO}	1.182	1.182	2.556	ns
1.5-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.607	2.607	5.573	ns
		GCLK PLL	t_{CO}	1.169	1.169	2.368	ns
1.5-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.610	2.610	5.571	ns
		GCLK PLL	t_{CO}	1.172	1.172	2.378	ns
1.5-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.612	2.612	5.581	ns
		GCLK PLL	t_{CO}	1.174	1.174	2.391	ns
3.3-V PCI	—	GCLK	t_{CO}	2.786	2.786	5.803	ns
		GCLK PLL	t_{CO}	1.322	1.322	2.697	ns
3.3-V PCI-X	—	GCLK	t_{CO}	2.786	2.786	5.803	ns
		GCLK PLL	t_{CO}	1.322	1.322	2.697	ns
LVDS	—	GCLK	t_{CO}	3.621	3.621	6.969	ns
		GCLK PLL	t_{CO}	2.190	2.190	3.880	ns

Table 4–64 through Table 4–65 list EP1AGX50 regional clock (RCLK) adder values that should be added to the GCLK values. These adder values are used to determine I/O timing when the I/O pin is driven using the regional clock. This applies for all I/O standards supported by Arria GX with general purpose I/O pins.

Table 4–69. EP1AGX60 Column Pins Output Timing Parameters (Part 3 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
SSTL-18 CLASS II	16 mA	GCLK	t_{CO}	2.737	2.737	6.025	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.585	ns
SSTL-18 CLASS II	18 mA	GCLK	t_{CO}	2.733	2.733	6.033	ns
		GCLK PLL	t_{CO}	1.160	1.160	2.593	ns
SSTL-18 CLASS II	20 mA	GCLK	t_{CO}	2.733	2.733	6.031	ns
		GCLK PLL	t_{CO}	1.160	1.160	2.591	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.756	2.756	6.086	ns
		GCLK PLL	t_{CO}	1.186	1.186	2.651	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.762	2.762	6.071	ns
		GCLK PLL	t_{CO}	1.189	1.189	2.631	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.740	2.740	6.060	ns
		GCLK PLL	t_{CO}	1.167	1.167	2.620	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.744	2.744	6.066	ns
		GCLK PLL	t_{CO}	1.171	1.171	2.626	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.736	2.736	6.059	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.619	ns
1.8-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.719	2.719	5.823	ns
		GCLK PLL	t_{CO}	1.146	1.146	2.383	ns
1.8-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.721	2.721	5.834	ns
		GCLK PLL	t_{CO}	1.148	1.148	2.394	ns
1.8-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.721	2.721	5.843	ns
		GCLK PLL	t_{CO}	1.148	1.148	2.403	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.756	2.756	6.085	ns
		GCLK PLL	t_{CO}	1.186	1.186	2.650	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.761	2.761	6.063	ns
		GCLK PLL	t_{CO}	1.188	1.188	2.623	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.743	2.743	6.065	ns
		GCLK PLL	t_{CO}	1.170	1.170	2.625	ns
1.5-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.743	2.743	6.067	ns
		GCLK PLL	t_{CO}	1.170	1.170	2.627	ns
1.5-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.737	2.737	6.065	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.625	ns
1.5-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.724	2.724	5.877	ns
		GCLK PLL	t_{CO}	1.151	1.151	2.437	ns
1.5-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.727	2.727	5.887	ns
		GCLK PLL	t_{CO}	1.154	1.154	2.447	ns
1.5-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.729	2.729	5.900	ns
		GCLK PLL	t_{CO}	1.156	1.156	2.460	ns

Table 4–74. EP1AGX90 Row Pins Output Timing Parameters (Part 3 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.857	2.857	6.106	ns
		GCLK PLL	t_{CO}	0.779	0.779	1.950	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.842	2.842	6.098	ns
		GCLK PLL	t_{CO}	0.764	0.764	1.942	ns
LVDS	—	GCLK	t_{CO}	2.898	2.898	6.265	ns
		GCLK PLL	t_{CO}	0.831	0.831	2.129	ns

Table 4–75 lists I/O timing specifications.

Table 4–75. EP1AGX90 Column Pins Output Timing Parameters (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	3.141	3.141	7.164	ns
		GCLK PLL	t_{CO}	1.077	1.077	3.029	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.996	2.996	6.792	ns
		GCLK PLL	t_{CO}	0.932	0.932	2.657	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.929	2.929	6.792	ns
		GCLK PLL	t_{CO}	0.865	0.865	2.657	ns
3.3-V LVTTL	16 mA	GCLK	t_{CO}	2.903	2.903	6.623	ns
		GCLK PLL	t_{CO}	0.839	0.839	2.488	ns
3.3-V LVTTL	20 mA	GCLK	t_{CO}	2.881	2.881	6.498	ns
		GCLK PLL	t_{CO}	0.817	0.817	2.363	ns
3.3-V LVTTL	24 mA	GCLK	t_{CO}	2.874	2.874	6.500	ns
		GCLK PLL	t_{CO}	0.810	0.810	2.365	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.996	2.996	6.792	ns
		GCLK PLL	t_{CO}	0.932	0.932	2.657	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.904	2.904	6.497	ns
		GCLK PLL	t_{CO}	0.840	0.840	2.362	ns
3.3-V LVCMOS	12 mA	GCLK	t_{CO}	2.876	2.876	6.419	ns
		GCLK PLL	t_{CO}	0.812	0.812	2.284	ns
3.3-V LVCMOS	16 mA	GCLK	t_{CO}	2.883	2.883	6.387	ns
		GCLK PLL	t_{CO}	0.819	0.819	2.252	ns
3.3-V LVCMOS	20 mA	GCLK	t_{CO}	2.870	2.870	6.369	ns
		GCLK PLL	t_{CO}	0.806	0.806	2.234	ns
3.3-V LVCMOS	24 mA	GCLK	t_{CO}	2.859	2.859	6.347	ns
		GCLK PLL	t_{CO}	0.795	0.795	2.212	ns
2.5 V	4 mA	GCLK	t_{CO}	2.958	2.958	6.824	ns
		GCLK PLL	t_{CO}	0.894	0.894	2.689	ns

Table 4–75. EP1AGX90 Column Pins Output Timing Parameters (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
2.5 V	8 mA	GCLK	t_{CO}	2.906	2.906	6.562	ns
		GCLK PLL	t_{CO}	0.842	0.842	2.427	ns
2.5 V	12 mA	GCLK	t_{CO}	2.885	2.885	6.445	ns
		GCLK PLL	t_{CO}	0.821	0.821	2.310	ns
2.5 V	16 mA	GCLK	t_{CO}	2.867	2.867	6.371	ns
		GCLK PLL	t_{CO}	0.803	0.803	2.236	ns
1.8 V	2 mA	GCLK	t_{CO}	2.998	2.998	7.816	ns
		GCLK PLL	t_{CO}	0.934	0.934	3.681	ns
1.8 V	4 mA	GCLK	t_{CO}	3.003	3.003	7.042	ns
		GCLK PLL	t_{CO}	0.939	0.939	2.907	ns
1.8 V	6 mA	GCLK	t_{CO}	2.927	2.927	6.778	ns
		GCLK PLL	t_{CO}	0.863	0.863	2.643	ns
1.8 V	8 mA	GCLK	t_{CO}	2.929	2.929	6.687	ns
		GCLK PLL	t_{CO}	0.865	0.865	2.552	ns
1.8 V	10 mA	GCLK	t_{CO}	2.883	2.883	6.610	ns
		GCLK PLL	t_{CO}	0.819	0.819	2.475	ns
1.8 V	12 mA	GCLK	t_{CO}	2.884	2.884	6.553	ns
		GCLK PLL	t_{CO}	0.820	0.820	2.418	ns
1.5 V	2 mA	GCLK	t_{CO}	2.978	2.978	7.346	ns
		GCLK PLL	t_{CO}	0.914	0.914	3.211	ns
1.5 V	4 mA	GCLK	t_{CO}	2.914	2.914	6.777	ns
		GCLK PLL	t_{CO}	0.850	0.850	2.642	ns
1.5 V	6 mA	GCLK	t_{CO}	2.917	2.917	6.659	ns
		GCLK PLL	t_{CO}	0.853	0.853	2.524	ns
1.5 V	8 mA	GCLK	t_{CO}	2.876	2.876	6.606	ns
		GCLK PLL	t_{CO}	0.812	0.812	2.471	ns
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.859	2.859	6.381	ns
		GCLK PLL	t_{CO}	0.797	0.797	2.250	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.842	2.842	6.331	ns
		GCLK PLL	t_{CO}	0.780	0.780	2.200	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.820	2.820	6.258	ns
		GCLK PLL	t_{CO}	0.758	0.758	2.127	ns
SSTL-2 CLASS II	20 mA	GCLK	t_{CO}	2.821	2.821	6.245	ns
		GCLK PLL	t_{CO}	0.759	0.759	2.114	ns
SSTL-2 CLASS II	24 mA	GCLK	t_{CO}	2.817	2.817	6.243	ns
		GCLK PLL	t_{CO}	0.755	0.755	2.112	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.858	2.858	6.356	ns
		GCLK PLL	t_{CO}	0.794	0.794	2.221	ns