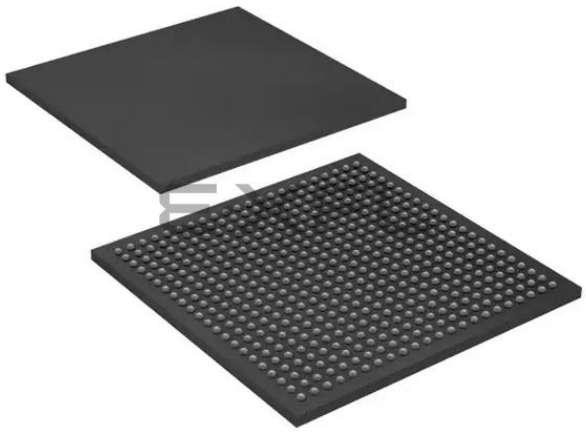

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1676
Number of Logic Elements/Cells	33520
Total RAM Bits	1348416
Number of I/O	230
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1agx35cf484i6n

- Main device features:
  - TriMatrix memory consisting of three RAM block sizes to implement true dual-port memory and first-in first-out (FIFO) buffers with performance up to 380 MHz
  - Up to 16 global clock networks with up to 32 regional clock networks per device
  - High-speed DSP blocks provide dedicated implementation of multipliers, multiply-accumulate functions, and finite impulse response (FIR) filters
  - Up to four enhanced phase-locked loops (PLLs) per device provide spread spectrum, programmable bandwidth, clock switch-over, and advanced multiplication and phase shifting
  - Support for numerous single-ended and differential I/O standards
  - High-speed source-synchronous differential I/O support on up to 47 channels
  - Support for source-synchronous bus standards, including SPI-4 Phase 2 (POS-PHY Level 4), SFI-4.1, XSBI, UTOPIA IV, NPSI, and CSIX-L1
  - Support for high-speed external memory including DDR and DDR2 SDRAM, and SDR SDRAM
  - Support for multiple intellectual property megafunctions from Altera® MegaCore® functions and Altera Megafunction Partners Program (AMPP^{SM})
  - Support for remote configuration updates

Table 1–1 lists Arria GX device features for FineLine BGA (FBGA) with flip chip packages.

Table 1–1. Arria GX Device Features (Part 1 of 2)

Feature	EP1AGX20C	EP1AGX35C/D		EP1AGX50C/D		EP1AGX60C/D/E			EP1AGX90E
	C	C	D	C	D	C	D	E	E
Package	484-pin, 780-pin (Flip chip)	484-pin (Flip chip)	780-pin (Flip chip)	484-pin (Flip chip)	780-pin, 1152-pin (Flip chip)	484-pin (Flip chip)	780-pin (Flip chip)	1152-pin (Flip chip)	1152-pin (Flip chip)
ALMs	8,632	13,408		20,064		24,040			36,088
Equivalent logic elements (LEs)	21,580	33,520		50,160		60,100			90,220
Transceiver channels	4	4	8	4	8	4	8	12	12
Transceiver data rate	600 Mbps to 3.125 Gbps	600 Mbps to 3.125 Gbps		600 Mbps to 3.125 Gbps		600 Mbps to 3.125 Gbps			600 Mbps to 3.125 Gbps
Source-synchronous receive channels	31	31	31	31	31, 42	31	31	42	47

Table 1–1. Arria GX Device Features (Part 2 of 2)

Feature	EP1AGX20C	EP1AGX35C/D		EP1AGX50C/D		EP1AGX60C/D/E			EP1AGX90E
	C	C	D	C	D	C	D	E	E
Source-synchronous transmit channels	29	29	29	29	29, 42	29	29	42	45
M512 RAM blocks (32 × 18 bits)	166	197		313		326			478
M4K RAM blocks (128 × 36 bits)	118	140		242		252			400
M-RAM blocks (4096 × 144 bits)	1	1		2		2			4
Total RAM bits	1,229,184	1,348,416		2,475,072		2,528,640			4,477,824
Embedded multipliers (18 × 18)	40	56		104		128			176
DSP blocks	10	14		26		32			44
PLLs	4	4		4	4, 8	4		8	8
Maximum user I/O pins	230, 341	230	341	229	350, 514	229	350	514	538

Arria GX devices are available in space-saving FBGA packages (refer to Table 1–2). All Arria GX devices support vertical migration within the same package. With vertical migration support, designers can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities. For I/O pin migration across densities, the designer must cross-reference the available I/O pins with the device pin-outs for all planned densities of a given package type to identify which I/O pins are migratable.

Table 1–2. Arria GX Package Options (Pin Counts and Transceiver Channels) (Part 1 of 2)

Device	Transceiver Channels	Source-Synchronous Channels		Maximum User I/O Pin Count		
		Receive	Transmit	484-Pin FBGA (23 mm)	780-Pin FBGA (29 mm)	1152-Pin FBGA (35 mm)
EP1AGX20C	4	31	29	230	341	—
EP1AGX35C	4	31	29	230	—	—
EP1AGX50C	4	31	29	229	—	—
EP1AGX60C	4	31	29	229	—	—
EP1AGX35D	8	31	29	—	341	—
EP1AGX50D	8	31, 42	29, 42	—	350	514

Bit-Slip Mode

The word aligner can operate in either pattern detection mode or in bit-slip mode.

The bit-slip mode provides the option to manually shift the word boundary through the FPGA. This feature is useful for:

- Longer synchronization patterns than the pattern detector can accommodate
- Scrambled data stream
- Input stream consisting of over-sampled data

The word aligner outputs a word boundary as it is received from the analog receiver after reset. You can examine the word and search its boundary in the FPGA. To do so, assert the `rx_bitslip` signal. The `rx_bitslip` signal should be toggled and held constant for at least two FPGA clock cycles.

For every rising edge of the `rx_bitslip` signal, the current word boundary is slipped by one bit. Every time a bit is slipped, the bit received earliest is lost. If bit slipping shifts a complete round of bus width, the word boundary is back to the original boundary.

The `rx_syncstatus` signal is not available in bit-slipping mode.

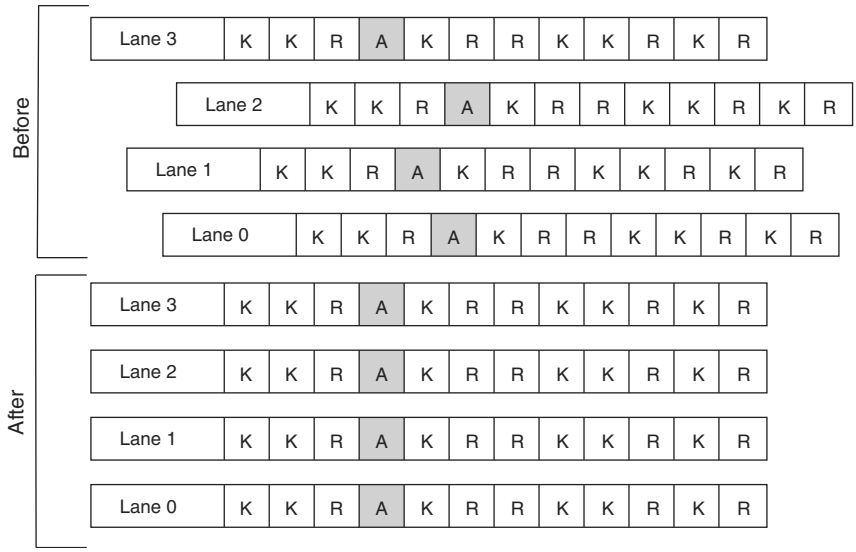
Channel Aligner

The channel aligner is available only in XAUI mode and aligns the signals of all four channels within a transceiver. The channel aligner follows the IEEE 802.3ae, clause 48 specification for channel bonding.

The channel aligner is a 16-word FIFO buffer with a state machine controlling the channel bonding process. The state machine looks for an /A/ (/K28.3/) in each channel and aligns all the /A/ code groups in the transceiver. When four columns of /A/ (denoted by //A//) are detected, the `rx_channelaligned` signal goes high, signifying that all the channels in the transceiver have been aligned. The reception of four consecutive misaligned /A/ code groups restarts the channel alignment sequence and sends the `rx_channelaligned` signal low.

Figure 2–16 shows misaligned channels before the channel aligner and the aligned channels after the channel aligner.

Figure 2–16. Before and After the Channel Aligner



Rate Matcher

In asynchronous systems, the upstream transmitter and local receiver can be clocked with independent reference clock sources. Frequency differences in the order of a few hundred PPM can potentially corrupt the data at the receiver.

The rate matcher compensates for small clock frequency differences between the upstream transmitter and the local receiver clocks by inserting or removing skip characters from the inter packet gap (IPG) or idle streams. It inserts a skip character if the local receiver is running a faster clock than the upstream transmitter. It deletes a skip character if the local receiver is running a slower clock than the upstream transmitter. The Quartus II software automatically configures the appropriate skip character as specified in the IEEE 802.3 for GIGE mode and PCI-Express Base Specification for PCI Express (PIPE) mode. The rate matcher is bypassed in Serial RapidIO and must be implemented in the PLD logic array or external circuits depending on your system design.

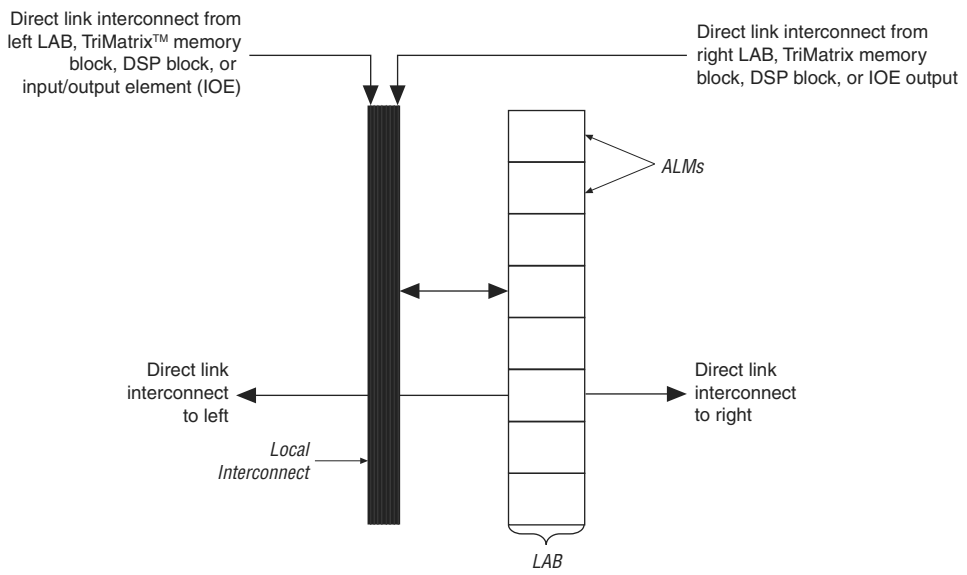
Table 2–5 lists the maximum frequency difference that the rate matcher can tolerate in XAUI, PCI Express (PIPE), GIGE, and Basic functional modes.

Table 2–5. Rate Matcher PPM Tolerance

Function Mode	PPM
XAUI	± 100
PCI Express (PIPE)	± 300
GIGE	± 100
Basic	± 300

Figure 2–26 shows the direct link connection.

Figure 2–26. Direct Link Connection



LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its ALMs. The control signals include three clocks, three clock enables, two asynchronous clears, synchronous clear, asynchronous preset or load, and synchronous load control signals, providing a maximum of 11 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use three clocks and three clock enable signals. However, there can only be up to two unique clocks per LAB, as shown in the LAB control signal generation circuit in Figure 2–27. Each LAB's clock and clock enable signals are linked. For example, any ALM in a particular LAB using the `labclk1` signal also uses `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses two LAB-wide clock signals. De-asserting the clock enable signal turns off the corresponding LAB-wide clock. Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. The asynchronous load acts as a preset when the asynchronous load data input is tied high. When the asynchronous load/preset signal is used, the `labclkena0` signal is no longer available.

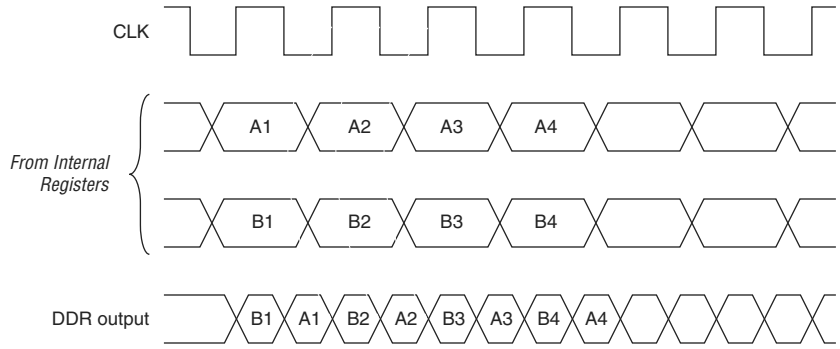
The LAB row clocks `[5..0]` and LAB local interconnect generate the LAB-wide control signals. The MultiTrack interconnects have inherently low skew. This low skew allows the MultiTrack interconnects to distribute clock and control signals in addition to data.

chains are also top- or bottom-half bypassable. This capability allows the shared arithmetic chain to cascade through half of the ALMs in a LAB while leaving the other half available for narrower fan-in functionality. Every other LAB column is top-half bypassable, while the other LAB columns are bottom-half bypassable. For more information about shared arithmetic chain interconnect, refer to "MultiTrack Interconnect" on page 2–44.

Register Chain

In addition to the general routing outputs, the ALMs in a LAB have register chain outputs. Register chain routing allows registers in the same LAB to be cascaded together. The register chain interconnect allows a LAB to use LUTs for a single combinational function and the registers to be used for an unrelated shift register implementation. These resources speed up connections between ALMs while saving local interconnect resources (refer to Figure 2–38). The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. For more information about register chain interconnect, refer to "MultiTrack Interconnect" on page 2–44.

Figure 2–76. Output Timing Diagram in DDR Mode



The Arria GX IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations. The negative-edge-clocked OE register holds the OE signal inactive until the falling edge of the clock to meet DDR SDRAM timing requirements.

External RAM Interfacing

In addition to the six I/O registers in each IOE, Arria GX devices also have dedicated phase-shift circuitry for interfacing with external memory interfaces, including DDR, DDR2 SDRAM, and SDR SDRAM. In every Arria GX device, the I/O banks at the top (Banks 3 and 4) and bottom (Banks 7 and 8) of the device support DQ and DQS signals with DQ bus modes of ×4, ×8/×9, ×16/×18, or ×32/×36. Table 2–23 shows the number of DQ and DQS buses that are supported per device.

Table 2–23. DQS and DQ Bus Mode Support *(Note 1)*

Device	Package	Number of ×4 Groups	Number of ×8/×9 Groups	Number of ×16/×18 Groups	Number of ×32/×36 Groups
EP1AGX20	484-pin FineLine BGA	2	0	0	0
EP1AGX35	484-pin FineLine BGA	2	0	0	0
	780-pin FineLine BGA	18	8	4	0
EP1AGX50/60	484-pin FineLine BGA	2	0	0	0
	780-pin FineLine BGA	18	8	4	0
	1,152-pin FineLine BGA	36	18	8	4
EP1AGX90	1,152-pin FineLine BGA	36	18	8	4

Note to Table 2–23:

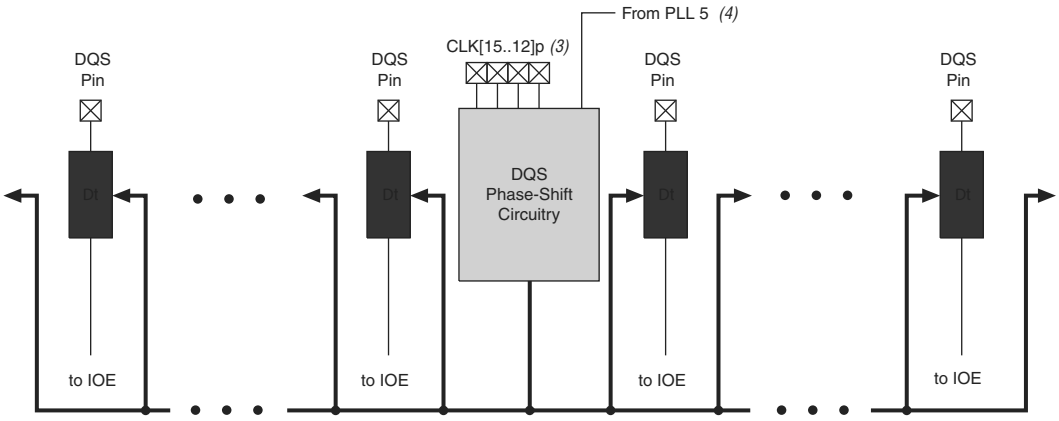
(1) Numbers are preliminary until devices are available.

A compensated delay element on each DQS pin automatically aligns input DQS synchronization signals with the data window of their corresponding DQ data signals. The DQS signals drive a local DQS bus in the top and bottom I/O banks. This DQS bus is an additional resource to the I/O clocks and is used to clock DQ input registers with the DQS signal.

The Arria GX device has two phase-shifting reference circuits, one on the top and one on the bottom of the device. The circuit on the top controls the compensated delay elements for all DQS pins on the top. The circuit on the bottom controls the compensated delay elements for all DQS pins on the bottom.

Each phase-shifting reference circuit is driven by a system reference clock, which must have the same frequency as the DQS signal. Clock pins `CLK[15..12]p` feed phase circuitry on the top of the device and clock pins `CLK[7..4]p` feed phase circuitry on the bottom of the device. In addition, PLL clock outputs can also feed the phase-shifting reference circuits. Figure 2–77 shows the phase-shift reference circuit control of each DQS delay shift on the top of the device. This same circuit is duplicated on the bottom of the device.

Figure 2–77. DQS Phase-Shift Circuitry *(Note 1)*, *(2)*



Notes to Figure 2–77:

(1) There are up to 18 pairs of DQS pins available on the top or bottom of the Arria GX device. There are up to 10 pairs on the right side and 8 pairs on the left side of the DQS phase-shift circuitry.

(2) The "t" module represents the DQS logic block.

(3) Clock pins `CLK[15..12]p` feed phase-shift circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase circuitry on the bottom of the device. You can also use a PLL clock output as a reference clock to phase shift circuitry.

(4) You can only use PLL 5 to feed the DQS phase-shift circuitry on the top of the device and PLL 6 to feed the DQS phase-shift circuitry on the bottom of the device.

These dedicated circuits combined with enhanced PLL clocking and phase-shift ability provide a complete hardware solution for interfacing to high-speed memory.

For more information about external memory interfaces, refer to the *External Memory Interfaces in Arria GX Devices* chapter.

Programmable Drive Strength

The output buffer for each Arria GX device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL, LVCMOS, SSTL, and HSTL standards have several levels of drive strength that you can control. The default setting used in the Quartus II software is the maximum current strength setting that is used to achieve maximum I/O performance. For all I/O standards, the minimum setting is the lowest drive strength that guarantees the I_{OH}/I_{OL} of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot.

Table 2–24 shows the possible settings for I/O standards with drive strength control.

Table 2–24. Programmable Drive Strength *(Note 1)*

I/O Standard	I_{OH} / I_{OL} Current Strength Setting (mA) for Column I/O Pins	I_{OH} / I_{OL} Current Strength Setting (mA) for Row I/O Pins
3.3-V LVTTL	24, 20, 16, 12, 8, 4	12, 8, 4
3.3-V LVCMOS	24, 20, 16, 12, 8, 4	8, 4
2.5-V LVTTL/LVCMOS	16, 12, 8, 4	12, 8, 4
1.8-V LVTTL/LVCMOS	12, 10, 8, 6, 4, 2	8, 6, 4, 2
1.5-V LVCMOS	8, 6, 4, 2	4, 2
SSTL-2 Class I	12, 8	12, 8
SSTL-2 Class II	24, 20, 16	16
SSTL-18 Class I	12, 10, 8, 6, 4	10, 8, 6, 4
SSTL-18 Class II	20, 18, 16, 8	—
HSTL-18 Class I	12, 10, 8, 6, 4	12, 10, 8, 6, 4
HSTL-18 Class II	20, 18, 16	—
HSTL-15 Class I	12, 10, 8, 6, 4	8, 6, 4
HSTL-15 Class II	20, 18, 16	—

Note to Table 2–24:

(1) The Quartus II software default current setting is the maximum setting for each I/O standard.

Open-Drain Output

Arria GX devices provide an optional open-drain (equivalent to an open collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (for example, interrupt and write enable signals) that can be asserted by any of several devices.

Bus Hold

Each Arria GX device I/O pin provides an optional bus-hold feature. Bus-hold circuitry can hold the signal on an I/O pin at its last-driven state. Because the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not needed to hold a signal level when the bus is tri-stated.

Bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output drives no higher than V_{CCIO} to prevent overdriving signals. If the bus-hold feature is enabled, the programmable pull-up option cannot be used. Disable the bus-hold feature when the I/O pin has been configured for differential signals.

Bus-hold circuitry uses a resistor with a nominal resistance (RBH) of approximately 7 kΩ to pull the signal level to the last-driven state. This information is provided for each V_{CCIO} voltage level. Bus-hold circuitry is active only after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

device, PLL 1 can drive a maximum of 16 transmitter channels in I/O Bank 2 or a maximum of 29 transmitter channels in I/O Banks 1 and 2. The Quartus II software can also merge receiver and transmitter PLLs when a receiver is driving a transmitter. In this case, one fast PLL can drive both the maximum numbers of receiver and transmitter channels.

For more information, refer to the "Differential Pin Placement Guidelines" section in the *High-Speed Differential I/O Interfaces with DPA in Arria GX Devices* chapter.

Table 2–30. EP1AGX20 Device Differential Channels *(Note 1)*

Package	Transmitter/Receiver	Total Channels	Center Fast PLLs	
			PLL1	PLL2
484-pin FineLine BGA	Transmitter	29	16	13
			13	16
	Receiver	31	17	14
			14	17
780-pin FineLine GBA	Transmitter	29	16	13
			13	16
	Receiver	31	17	14
			14	17

Note to Table 2–30:

(1) The total number of receiver channels includes the four non-dedicated clock channels that can be optionally used as data channels.

Table 2–31. EP1AGX35 Device Differential Channels *(Note 1)*

Package	Transmitter/Receiver	Total Channels	Center Fast PLLs	
			PLL1	PLL2
484-pin FineLine BGA	Transmitter	29	16	13
			13	16
	Receiver	31	17	14
			14	17
780-pin FineLine BGA	Transmitter	29	16	13
			13	16
	Receiver	31	17	14
			14	17

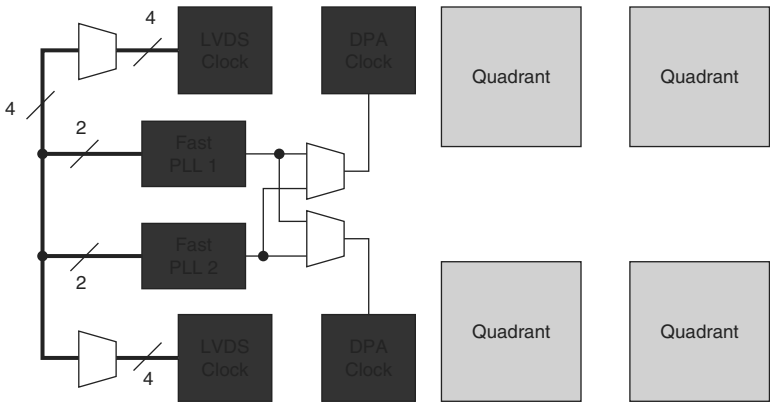
Note to Table 2–31:

(1) The total number of receiver channels includes the four non-dedicated clock channels that can be optionally used as data channels.

Fast PLL and Channel Layout

The receiver and transmitter channels are interleaved as such that each I/O bank on the left side of the device has one receiver channel and one transmitter channel per LAB row. Figure 2–81 shows the fast PLL and channel layout in the EP1AGX20C, EP1AGX35C/D, EP1AGX50C/D and EP1AGX60C/D devices. Figure 2–82 shows the fast PLL and channel layout in EP1AGX60E and EP1AGX90E devices.

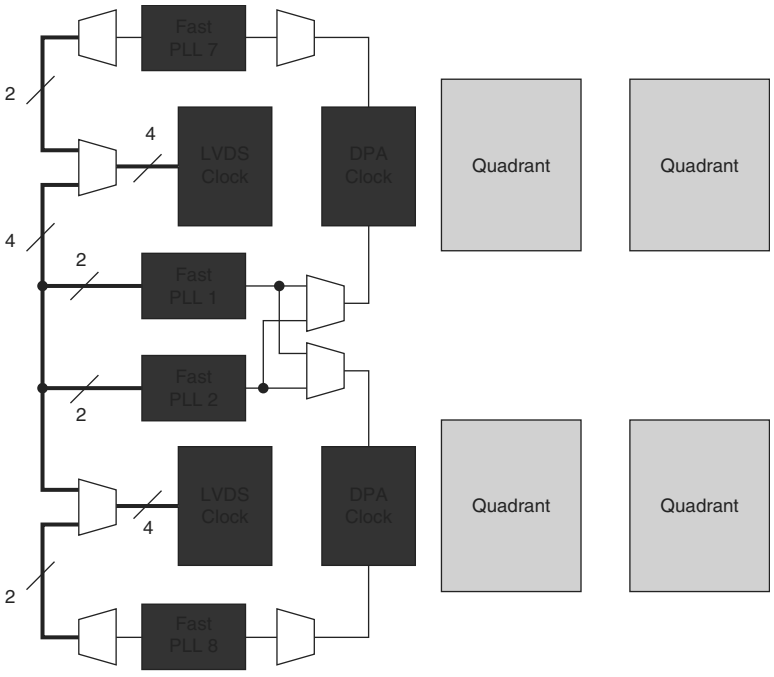
Figure 2–81. Fast PLL and Channel Layout in EP1AGX20C, EP1AGX35C/D, EP1AGX50C/D, EP1AGX60C/D Devices *(Note 1)*



Note to Figure 2–81:

(1) For the number of channels each device supports, refer to Table 2–30.

Figure 2–82. Fast PLL and Channel Layout in EP1AGX60E and EP1AGX90E Devices *(Note 1)*



Note to Figure 2–82:

(1) For the number of channels each device supports, refer to Table 2–30 through Table 2–34.

Table 3–1. Arria GX JTAG Instructions

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer.
EXTEST *(1)*	00 0000 1111	Allows external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing IDCODE to be serially shifted out of TDO.
HIGHZ *(1)*	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP *(1)*	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions	—	Used when configuring an Arria GX device via the JTAG port with a USB-Blaster™, MasterBlaster™, ByteBlasterMV™, EthernetBlaster™, or ByteBlaster II download cable, or when using a **.jam** or **.jbc** via an embedded processor or JRunner™.
PULSE_NCONFIG	00 0000 0001	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.
CONFIG_IO *(2)*	00 0000 1101	Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, during, or after configuration. Stops configuration if executed during configuration. Once issued, the CONFIG_IO instruction holds nSTATUS low to reset the configuration device. nSTATUS is held low until the IOE configuration register is loaded and the TAP controller state machine transitions to the UPDATE_DR state.

Notes to Table 3–1:

(1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

(2) For more information about using the CONFIG_IO instruction, refer to the *MorphIO: An I/O Reconfiguration Solution for Altera Devices* White Paper.

Table 4–45. Timing Measurement Methodology for Input Pins *(Note 1)*, *(2)*, *(3)*, *(4)* (Part 2 of 2)

I/O Standard	Measurement Conditions			Measurement Point
	V_{CCIO} (V)	V_{REF} (V)	Edge Rate (ns)	VMEAS (V)
Differential SSTL-18 Class II	1.660	0.830	1.660	0.83
1.5-V differential HSTL Class I	1.375	0.688	1.375	0.6875
1.5-V differential HSTL Class II	1.375	0.688	1.375	0.6875
1.8-V differential HSTL Class I	1.660	0.830	1.660	0.83
1.8-V differential HSTL Class II	1.660	0.830	1.660	0.83
LVDS	2.325	—	0.100	1.1625
LVPECL	3.135	—	0.100	1.5675

Notes to Table 4–45:

(1) Input buffer sees no load at buffer input.
(2) Input measuring point at buffer input is 0.5 V_{CCIO}.
(3) Output measuring point is 0.5 V_{CC} at internal node.
(4) Input edge rate is 1 V/ns.
(5) Less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V with less than 30-mV ripple.
(6) V_{CCPD} = 2.97 V, less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V.

Clock Network Skew Adders

The Quartus II software models skew within dedicated clock networks such as global and regional clocks. Therefore, the intra-clock network skew adder is not specified. Table 4–46 specifies the intra clock skew between any two clock networks driving any registers in the Arria GX device.

Table 4–46. Clock Network Specifications

Name	Description	Min	Typ	Max	Units
Clock skew adder EP1AGX20/35 *(1)*	Inter-clock network, same side	—	—	± 50	ps
	Inter-clock network, entire chip	—	—	± 100	ps
Clock skew adder EP1AGX50/60 *(1)*	Inter-clock network, same side	—	—	± 50	ps
	Inter-clock network, entire chip	—	—	± 100	ps
Clock skew adder EP1AGX90 *(1)*	Inter-clock network, same side	—	—	± 55	ps
	Inter-clock network, entire chip	—	—	± 110	ps

Note to Table 4–46:

(1) This is in addition to intra-clock network skew, which is modeled in the Quartus II software.

Default Capacitive Loading of Different I/O Standards

See Table 4–47 for default capacitive loading of different I/O standards.

Table 4–47. Default Loading of Different I/O Standards for Arria GX Devices (Part 1 of 2)

I/O Standard	Capacitive Load	Units
LVTTL	0	pF
LVCMOS	0	pF
2.5 V	0	pF

Table 4–51 describes I/O timing specifications.

Table 4–51. EP1AGX20 Column Pins Output Timing Parameters (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	2.909	2.909	6.541	ns
		GCLK PLL	t_{CO}	1.467	1.467	3.435	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.764	2.764	6.169	ns
		GCLK PLL	t_{CO}	1.322	1.322	3.063	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.697	2.697	6.169	ns
		GCLK PLL	t_{CO}	1.255	1.255	3.063	ns
3.3-V LVTTL	16 mA	GCLK	t_{CO}	2.671	2.671	6.000	ns
		GCLK PLL	t_{CO}	1.229	1.229	2.894	ns
3.3-V LVTTL	20 mA	GCLK	t_{CO}	2.649	2.649	5.875	ns
		GCLK PLL	t_{CO}	1.207	1.207	2.769	ns
3.3-V LVTTL	24 mA	GCLK	t_{CO}	2.642	2.642	5.877	ns
		GCLK PLL	t_{CO}	1.200	1.200	2.771	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.764	2.764	6.169	ns
		GCLK PLL	t_{CO}	1.322	1.322	3.063	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.672	2.672	5.874	ns
		GCLK PLL	t_{CO}	1.230	1.230	2.768	ns
3.3-V LVCMOS	12 mA	GCLK	t_{CO}	2.644	2.644	5.796	ns
		GCLK PLL	t_{CO}	1.202	1.202	2.690	ns
3.3-V LVCMOS	16 mA	GCLK	t_{CO}	2.651	2.651	5.764	ns
		GCLK PLL	t_{CO}	1.209	1.209	2.658	ns
3.3-V LVCMOS	20 mA	GCLK	t_{CO}	2.638	2.638	5.746	ns
		GCLK PLL	t_{CO}	1.196	1.196	2.640	ns
3.3-V LVCMOS	24 mA	GCLK	t_{CO}	2.627	2.627	5.724	ns
		GCLK PLL	t_{CO}	1.185	1.185	2.618	ns
2.5 V	4 mA	GCLK	t_{CO}	2.726	2.726	6.201	ns
		GCLK PLL	t_{CO}	1.284	1.284	3.095	ns
2.5 V	8 mA	GCLK	t_{CO}	2.674	2.674	5.939	ns
		GCLK PLL	t_{CO}	1.232	1.232	2.833	ns
2.5 V	12 mA	GCLK	t_{CO}	2.653	2.653	5.822	ns
		GCLK PLL	t_{CO}	1.211	1.211	2.716	ns
2.5 V	16 mA	GCLK	t_{CO}	2.635	2.635	5.748	ns
		GCLK PLL	t_{CO}	1.193	1.193	2.642	ns
1.8 V	2 mA	GCLK	t_{CO}	2.766	2.766	7.193	ns
		GCLK PLL	t_{CO}	1.324	1.324	4.087	ns
1.8 V	4 mA	GCLK	t_{CO}	2.771	2.771	6.419	ns
		GCLK PLL	t_{CO}	1.329	1.329	3.313	ns

Table 4–61. EP1AGX50 Column Pins Input Timing Parameters (Part 2 of 2)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
1.8-V HSTL CLASS I	GCLK	t_{SU}	1.104	1.104	2.466	ns
		t_H	–0.999	–0.999	–2.189	ns
	GCLK PLL	t_{SU}	2.546	2.546	5.573	ns
		t_H	–2.441	–2.441	–5.296	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	1.074	1.074	2.424	ns
		t_H	–0.969	–0.969	–2.147	ns
	GCLK PLL	t_{SU}	2.539	2.539	5.564	ns
		t_H	–2.434	–2.434	–5.287	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.122	1.122	2.594	ns
		t_H	–1.017	–1.017	–2.317	ns
	GCLK PLL	t_{SU}	2.564	2.564	5.701	ns
		t_H	–2.459	–2.459	–5.424	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.094	1.094	2.557	ns
		t_H	–0.989	–0.989	–2.280	ns
	GCLK PLL	t_{SU}	2.557	2.557	5.692	ns
		t_H	–2.452	–2.452	–5.415	ns
3.3-V PCI	GCLK	t_{SU}	1.247	1.247	2.890	ns
		t_H	–1.142	–1.142	–2.613	ns
	GCLK PLL	t_{SU}	2.689	2.689	5.997	ns
		t_H	–2.584	–2.584	–5.720	ns
3.3-V PCI-X	GCLK	t_{SU}	1.247	1.247	2.890	ns
		t_H	–1.142	–1.142	–2.613	ns
	GCLK PLL	t_{SU}	2.689	2.689	5.997	ns
		t_H	–2.584	–2.584	–5.720	ns
LVDS	GCLK	t_{SU}	1.106	1.106	2.489	ns
		t_H	–1.001	–1.001	–2.212	ns
	GCLK PLL	t_{SU}	2.530	2.530	5.564	ns
		t_H	–2.425	–2.425	–5.287	ns

Table 4–62 lists I/O timing specifications.

Table 4–62. EP1AGX50 Row Pins Output Timing Parameters (Part 1 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	2.915	2.915	6.713	ns
		GCLK PLL	t_{CO}	1.487	1.487	3.629	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.787	2.787	6.073	ns
		GCLK PLL	t_{CO}	1.359	1.359	2.989	ns

Table 4–64 lists row pin delay adders when using the regional clock in Arria GX devices.

Table 4–64. EP1AGX50 Row Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.151	0.151	0.329	ns
RCLK PLL input adder	0.011	0.011	0.016	ns
RCLK output adder	–0.151	–0.151	–0.329	ns
RCLK PLL output adder	–0.011	–0.011	–0.016	ns

Table 4–65 lists column pin delay adders when using the regional clock in Arria GX devices.

Table 4–65. EP1AGX50 Column Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.146	0.146	0.334	ns
RCLK PLL input adder	–1.713	–1.713	–3.645	ns
RCLK output adder	–0.146	–0.146	–0.336	ns
RCLK PLL output adder	1.716	1.716	4.488	ns

EP1AGX60 I/O Timing Parameters

Table 4–66 through Table 4–69 list the maximum I/O timing parameters for EP1AGX60 devices for I/O standards which support general purpose I/O pins.

Table 4–66 lists I/O timing specifications.

Table 4–66. EP1AGX60 Row Pins Input Timing Parameters (Part 1 of 3)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.413	1.413	3.113	ns
		t_H	–1.308	–1.308	–2.836	ns
	GCLK PLL	t_{SU}	2.975	2.975	6.536	ns
		t_H	–2.870	–2.870	–6.259	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.413	1.413	3.113	ns
		t_H	–1.308	–1.308	–2.836	ns
	GCLK PLL	t_{SU}	2.975	2.975	6.536	ns
		t_H	–2.870	–2.870	–6.259	ns
2.5 V	GCLK	t_{SU}	1.425	1.425	3.094	ns
		t_H	–1.320	–1.320	–2.817	ns
	GCLK PLL	t_{SU}	2.987	2.987	6.517	ns
		t_H	–2.882	–2.882	–6.240	ns

Table 4–66. EP1AGX60 Row Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.281	1.281	2.777	ns
		t_H	–1.176	–1.176	–2.500	ns
	GCLK PLL	t_{SU}	2.853	2.853	6.220	ns
		t_H	–2.748	–2.748	–5.943	ns
LVDS	GCLK	t_{SU}	1.208	1.208	2.664	ns
		t_H	–1.103	–1.103	–2.387	ns
	GCLK PLL	t_{SU}	2.767	2.767	6.083	ns
		t_H	–2.662	–2.662	–5.806	ns

Table 4–67 lists I/O timing specifications.

Table 4–67. EP1AGX60 Column Pins Input Timing Parameters (Part 1 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.124	1.124	2.493	ns
		t_H	–1.019	–1.019	-2.216	ns
	GCLK PLL	t_{SU}	2.694	2.694	5.928	ns
		t_H	–2.589	–2.589	-5.651	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.124	1.124	2.493	ns
		t_H	–1.019	–1.019	-2.216	ns
	GCLK PLL	t_{SU}	2.694	2.694	5.928	ns
		t_H	–2.589	–2.589	-5.651	ns
2.5 V	GCLK	t_{SU}	1.134	1.134	2.475	ns
		t_H	–1.029	–1.029	-2.198	ns
	GCLK PLL	t_{SU}	2.704	2.704	5.910	ns
		t_H	–2.599	–2.599	-5.633	ns
1.8 V	GCLK	t_{SU}	1.200	1.200	2.685	ns
		t_H	–1.095	–1.095	-2.408	ns
	GCLK PLL	t_{SU}	2.770	2.770	6.120	ns
		t_H	–2.665	–2.665	-5.843	ns
1.5 V	GCLK	t_{SU}	1.203	1.203	2.778	ns
		t_H	–1.098	–1.098	-2.501	ns
	GCLK PLL	t_{SU}	2.773	2.773	6.213	ns
		t_H	–2.668	–2.668	-5.936	ns
SSTL-2 CLASS I	GCLK	t_{SU}	0.948	0.948	1.951	ns
		t_H	–0.843	–0.843	-1.674	ns
	GCLK PLL	t_{SU}	2.519	2.519	5.388	ns
		t_H	–2.414	–2.414	-5.111	ns

Table 4–72. EP1AGX90 Row Pins Input Timing Parameters (Part 2 of 2)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
1.8-V HSTL CLASS I	GCLK	t_{SU}	1.159	1.159	2.447	ns
		t_H	–1.054	–1.054	–2.170	ns
	GCLK PLL	t_{SU}	3.212	3.212	6.565	ns
		t_H	–3.107	–3.107	–6.288	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	1.157	1.157	2.441	ns
		t_H	–1.052	–1.052	–2.164	ns
	GCLK PLL	t_{SU}	3.235	3.235	6.597	ns
		t_H	–3.130	–3.130	–6.320	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.185	1.185	2.575	ns
		t_H	–1.080	–1.080	–2.298	ns
	GCLK PLL	t_{SU}	3.238	3.238	6.693	ns
		t_H	–3.133	–3.133	–6.416	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.183	1.183	2.569	ns
		t_H	–1.078	–1.078	–2.292	ns
	GCLK PLL	t_{SU}	3.261	3.261	6.725	ns
		t_H	–3.156	–3.156	–6.448	ns
LVDS	GCLK	t_{SU}	1.098	1.098	2.439	ns
		t_H	–0.993	–0.993	–2.162	ns
	GCLK PLL	t_{SU}	3.160	3.160	6.566	ns
		t_H	–3.055	–3.055	–6.289	ns

Table 4–73 lists I/O timing specifications.

Table 4–73. EP1AGX90 Column Pins Input Timing Parameters (Part 1 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.018	1.018	2.290	ns
		t_H	–0.913	–0.913	–2.013	ns
	GCLK PLL	t_{SU}	3.082	3.082	6.425	ns
		t_H	–2.977	–2.977	–6.148	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.018	1.018	2.290	ns
		t_H	–0.913	–0.913	–2.013	ns
	GCLK PLL	t_{SU}	3.082	3.082	6.425	ns
		t_H	–2.977	–2.977	–6.148	ns
2.5 V	GCLK	t_{SU}	1.028	1.028	2.272	ns
		t_H	–0.923	–0.923	–1.995	ns
	GCLK PLL	t_{SU}	3.092	3.092	6.407	ns
		t_H	–2.987	–2.987	–6.130	ns

Table 4–99 lists performance notes.

Table 4–99. Arria GX Performance Notes

Applications		Resources Used			Performance
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	–6 Speed Grade
LE	16-to-1 multiplexer	5	0	0	168.41
	32-to-1 multiplexer	11	0	0	334.11
	16-bit counter	16	0	0	374.0
	64-bit counter	64	0	0	168.41
TriMatrix Memory M512 block	Simple dual-port RAM 32 x 18 bit	0	1	0	348.0
	FIFO 32 x 18 bit	0	1	0	333.22
TriMatrix Memory M4K block	Simple dual-port RAM 128 x 36 bit	0	1	0	344.71
	True dual-port RAM 128 x 18 bit	0	1	0	348.0
TriMatrix Memory MegaRAM block	Single port RAM 4K x 144 bit	0	2	0	244.0
	Simple dual-port RAM 4K x 144 bit	0	1	0	292.0
	True dual-port RAM 4K x 144 bit	0	2	0	244.0
	Single port RAM 8K x 72 bit	0	1	0	247.0
	Simple dual-port RAM 8K x 72 bit	0	1	0	292.0
	Single port RAM 16K x 36 bit	0	1	0	254.0
	Simple dual-port RAM 16K x 36 bit	0	1	0	292.0
	True dual-port RAM 16K x 36 bit	0	1	0	251.0
	Single port RAM 32K x 18 bit	0	1	0	317.36
	Simple dual-port RAM 32K x 18 bit	0	1	0	292.0
	True dual-port RAM 32K x 18 bit	0	1	0	251.0
	Single port RAM 64K x 9 bit	0	1	0	254.0
	Simple dual-port RAM 64K x 9 bit	0	1	0	292.0
	True dual-port RAM 64K x 9 bit	0	1	0	251.0

Table 4–110. Maximum DCD for DDIO Output on Row I/O Pins Without PLL in the Clock Path *Note (1)*

Maximum DCD (ps) for Row DDIO Output I/O Standard	Input I/O Standard (No PLL in the Clock Path)					Units
	TTL/CMOS		SSTL-2	SSTL/HSTL	LVDS	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	3.3V	
LVDS	180	180	180	180	180	ps

Note to Table 4–110:

(1) Table 4–110 assumes the input clock has zero DCD.

Table 4–111. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path *(Note 1)*

Maximum DCD (ps) for DDIO Column Output I/O Standard	Input IO Standard (No PLL in the Clock Path)				Units
	TTL/CMOS		SSTL-2	SSTL/HSTL	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	
3.3-V LVTTL	440	495	170	160	ps
3.3-V LVCMOS	390	450	120	110	ps
2.5 V	375	430	105	95	ps
1.8 V	325	385	90	100	ps
1.5-V LVCMOS	430	490	160	155	ps
SSTL-2 Class I	355	410	85	75	ps
SSTL-2 Class II	350	405	80	70	ps
SSTL-18 Class I	335	390	65	65	ps
SSTL-18 Class II	320	375	70	80	ps
1.8-V HSTL Class I	330	385	60	70	ps
1.8-V HSTL Class II	330	385	60	70	ps
1.5-V HSTL Class I	330	390	60	70	ps
1.5-V HSTL Class II	330	360	90	100	ps
LVPECL	180	180	180	180	ps

Note to Table 4–111:

(1) Table 4–111 assumes the input clock has zero DCD.

Table 4–112. Maximum DCD for DDIO Output on Row I/O Pins With PLL in the Clock Path

Maximum DCD (ps) for Row DDIO Output I/O Standard	Arria GX Devices (PLL Output Feeding DDIO)	Units
	–6 Speed Grade	
3.3-V LVTTL	105	ps
3.3-V LVCMOS	75	ps
2.5V	90	ps
1.8V	100	ps
1.5-V LVCMOS	100	ps
SSTL-2 Class I	75	ps
SSTL-2 Class II	70	ps