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Understanding Embedded - FPGAs (Field Programmable Gate Array)

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1676
Number of Logic Elements/Cells	33520
Total RAM Bits	1348416
Number of I/O	341
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep1agx35df780c6

AGX51002-2.0

Transceivers

Arria® GX devices incorporate up to 12 high-speed serial transceiver channels that build on the success of the Stratix® II GX device family. Arria GX transceivers are structured into full-duplex (transmitter and receiver) four-channel groups called transceiver blocks located on the right side of the device. You can configure the transceiver blocks to support the following serial connectivity protocols (functional modes):

- PCI Express (PIPE)
- Gigabit Ethernet (GIGE)
- XAUI
- Basic (600 Mbps to 3.125 Gbps)
- SDI (HD, 3G)
- Serial RapidIO (1.25 Gbps, 2.5 Gbps, 3.125 Gbps)

Transceivers within each block are independent and have their own set of dividers. Therefore, each transceiver can operate at different frequencies. Each block can select from two reference clocks to provide two clock domains that each transceiver can select from.

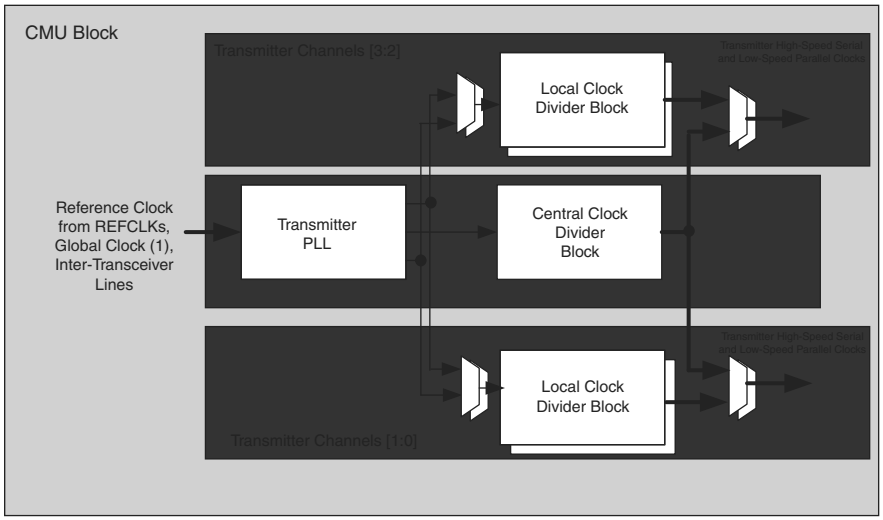
Table 2–1 lists the number of transceiver channels for each member of the Arria GX family.

Table 2–1. Arria GX Transceiver Channels

Device	Number of Transceiver Channels
EP1AGX20C	4
EP1AGX35C	4
EP1AGX35D	8
EP1AGX50C	4
EP1AGX50D	8
EP1AGX60C	4
EP1AGX60D	8
EP1AGX60E	12
EP1AGX90E	12

Figure 2–3 shows the block diagram of the clock multiplier unit.

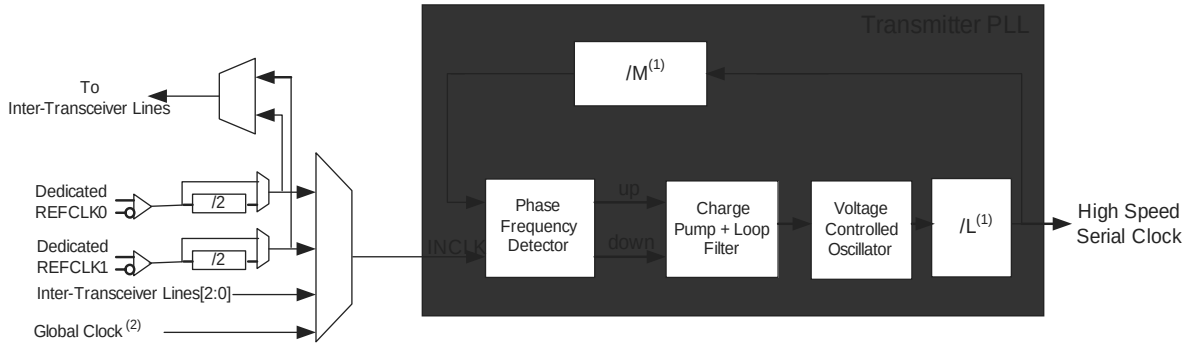
Figure 2–3. Clock Multiplier Unit



The transmitter PLL multiplies the input reference clock to generate the high-speed serial clock required to support the intended protocol. It implements a half-rate voltage controlled oscillator (VCO) that generates a clock at half the frequency of the serial data rate for which it is configured.

Figure 2–4 shows the block diagram of the transmitter PLL.

Figure 2–4. Transmitter PLL



Notes to Figure 2–4:

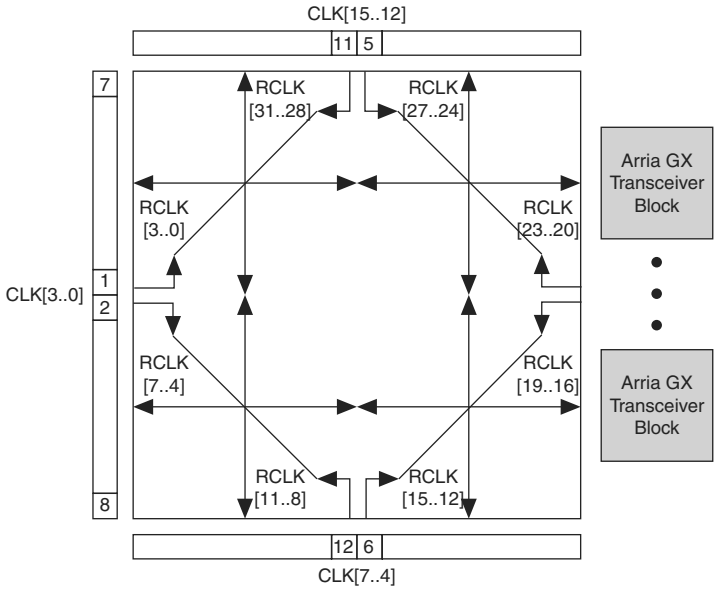
(1) You only need to select the protocol and the available input reference clock frequency in the ALTGXB MegaWizard Plug-In Manager. Based on your selections, the MegaWizard Plug-In Manager automatically selects the necessary /M and /L dividers (clock multiplication factors).

(2) The global clock line must be driven from an input pin only.

The reference clock input to the transmitter PLL can be derived from:

- One of two available dedicated reference clock input pins (`REFCLK0` or `REFCLK1`) of the associated transceiver block
- PLD global clock network (must be driven directly from an input clock pin and cannot be driven by user logic or enhanced PLL)

Figure 2–24. Regional Clock Resources in Arria GX Devices



For the RCLK or GCLK network to route into the transceiver, a local route input output (LRIO) channel is required. Each LRIO clock region has up to eight clock paths and each transceiver block has a maximum of eight clock paths for connecting with LRIO clocks. These resources are limited and determine the number of clocks that can be used between the PLD and transceiver blocks. Table 2–7 and Table 2–8 list the number of LRIO resources available for Arria GX devices with different numbers of transceiver blocks.

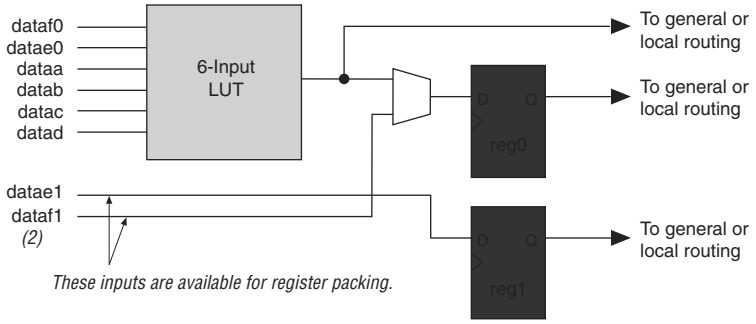
Table 2–7. Available Clocking Connections for Transceivers in EP1AGX35D, EP1AGX50D, and EP1AGX60D

Source	Clock Resource		Transceiver	
	Global Clock	Regional Clock	Bank13 8 Clock I/O	Bank14 8 Clock I/O
Region0 8 LRIO clock	✓	RCLK 20-27	✓	—
Region1 8 LRIO clock	✓	RCLK 12-19	—	✓

Table 2–8. Available Clocking Connections for Transceivers in EP1AGX60E and EP1AGX90E

Source	Clock Resource		Transceiver		
	Global Clock	Regional Clock	Bank13 8 Clock I/O	Bank14 8 Clock I/O	Bank15 8 Clock I/O
Region0 8 LRIO clock	✓	RCLK 20-27	✓	—	—
Region1 8 LRIO clock	✓	RCLK 20-27	✓	✓	—
Region2 8 LRIO clock	✓	RCLK 12-19	—	✓	✓
Region3 8 LRIO clock	✓	RCLK 12-19	—	—	✓

Figure 2–32. Six-Input Function in Normal Mode *Note (1), (2)*



Notes to Figure 2–32:

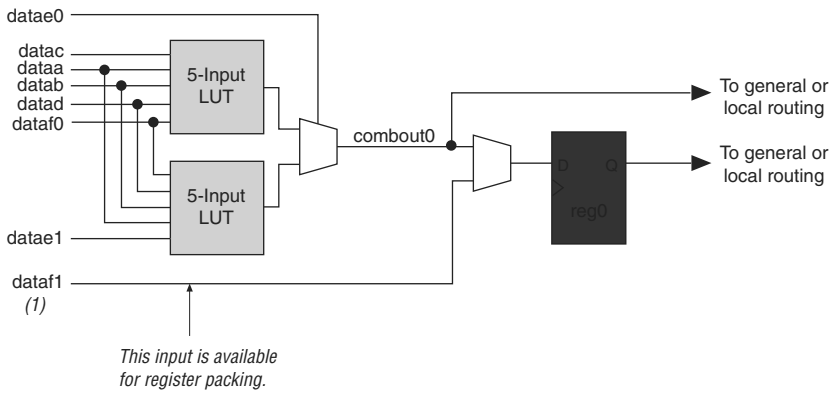
(1) If `datae1` and `dataf1` are used as inputs to the six-input function, `datae0` and `dataf0` are available for register packing.

(2) The `dataf1` input is available for register packing only if the six-input function is un-registered.

Extended LUT Mode

Extended LUT mode is used to implement a specific set of seven-input functions. The set must be a 2-to-1 multiplexer fed by two arbitrary five-input functions sharing four inputs. Figure 2–33 shows the template of supported seven-input functions utilizing extended LUT mode. In this mode, if the seven-input function is unregistered, the unused eighth input is available for register packing. Functions that fit into the template shown in Figure 2–33 occur naturally in designs. These functions often appear in designs as "if-else" statements in Verilog HDL or VHDL code.

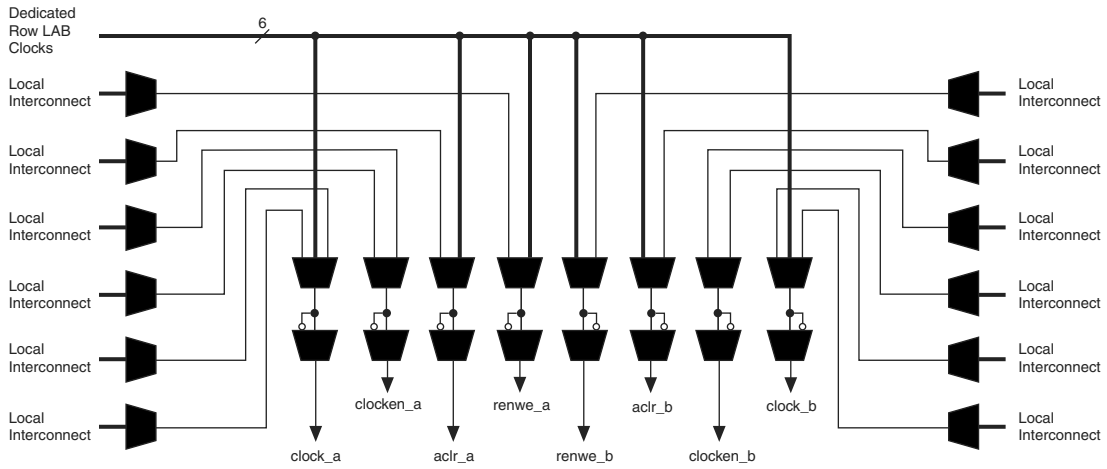
Figure 2–33. Template for Supported Seven-Input Functions in Extended LUT Mode



Note to Figure 2–33:

(1) If the seven-input function is unregistered, the unused eighth input is available for register packing. The second register, `reg1`, is not available.

Figure 2–46. M-RAM Block Control Signals



The R4, R24, C4, and direct link interconnects from adjacent LABs on either the right or left side drive the M-RAM block local interconnect. Up to 16 direct link input connections to the M-RAM block are possible from the left adjacent LABs and another 16 are possible from the right adjacent LAB. M-RAM block outputs can also connect to left and right LABs through direct link interconnect. Figure 2–47 shows an example floorplan for the EP1AGX90 device and the location of the M-RAM interfaces. Figure 2–48 and Figure 2–49 show the interface between the M-RAM block and the logic array.

PLLs and Clock Networks

Arria GX devices provide a hierarchical clock structure and multiple PLLs with advanced features. The large number of clocking resources in combination with the clock synthesis precision provided by enhanced and fast PLLs provides a complete clock management solution.

Global and Hierarchical Clocking

Arria GX devices provide 16 dedicated global clock networks and 32 regional clock networks (eight per device quadrant). These clocks are organized into a hierarchical clock structure that allows for up to 24 clocks per device region with low skew and delay. This hierarchical clocking scheme provides up to 48 unique clock domains in Arria GX devices.

There are 12 dedicated clock pins (`CLK[15..12]` and `CLK[7..0]`) to drive either the global or regional clock networks. Four clock pins drive each side of the device except the right side, as shown in Figure 2–54 and Figure 2–55. Internal logic and enhanced and fast PLL outputs can also drive the global and regional clock networks. Each global and regional clock has a clock control block, which controls the selection of the clock source and dynamically enables or disables the clock to reduce power consumption. Table 2–16 lists the global and regional clock features.

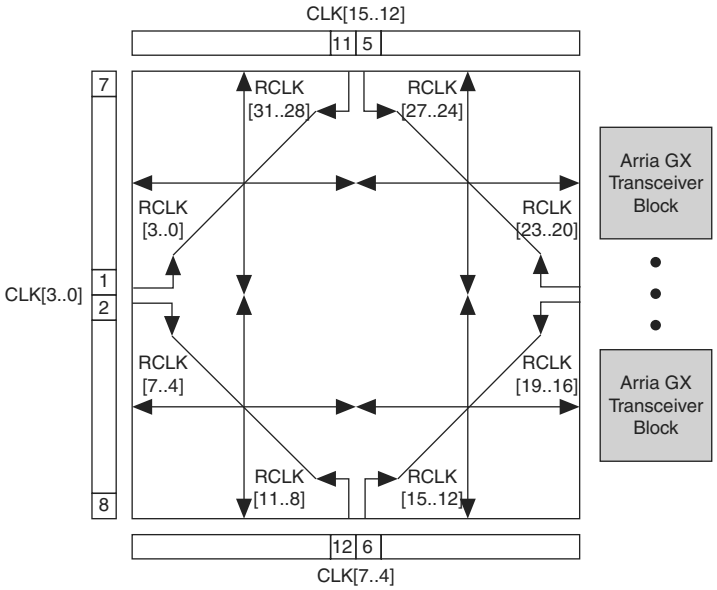
Table 2–16. Global and Regional Clock Features

Feature	Global Clocks	Regional Clocks
Number per device	16	32
Number available per quadrant	16	8
Sources	Clock pins, PLL outputs, core routings, inter-transceiver clocks	Clock pins, PLL outputs, core routings, inter-transceiver clocks
Dynamic clock source selection	✓	—
Dynamic enable/disable	✓	✓

Global Clock Network

These clocks drive throughout the entire device, feeding all device quadrants. GCLK networks can be used as clock sources for all resources in the device IOEs, ALMs, DSP blocks, and all memory blocks. These resources can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin. The global clock networks can also be driven by internal logic for internally generated global clocks and asynchronous clears, clock enables, or other control signals with large fanout. Figure 2–54 shows the 12 dedicated `CLK` pins driving global clock networks.

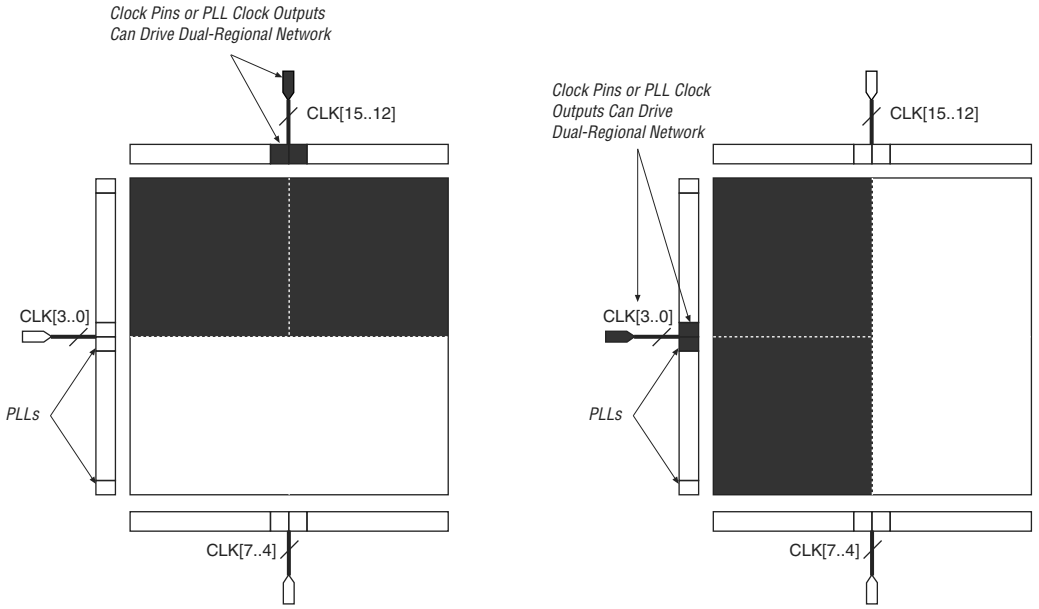
Figure 2–55. Regional Clocks



Dual-Regional Clock Network

A single source (CLK pin or PLL output) can generate a dual-RCLK by driving two RCLK network lines in adjacent quadrants (one from each quadrant), which allows logic that spans multiple quadrants to use the same low skew clock. The routing of this clock signal on an entire side has approximately the same speed but slightly higher clock skew when compared with a clock signal that drives a single quadrant. Internal logic-array routing can also drive a dual-regional clock. Clock pins and enhanced PLL outputs on the top and bottom can drive horizontal dual-regional clocks. Clock pins and fast PLL outputs on the left and right can drive vertical dual-regional clocks, as shown in Figure 2–56. Corner PLLs cannot drive dual-regional clocks.

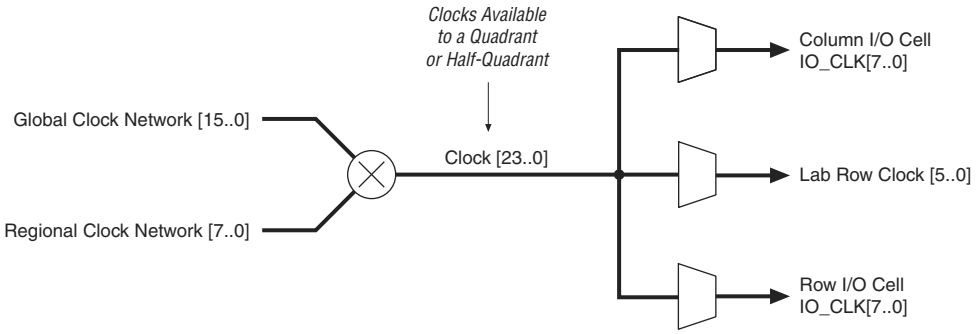
Figure 2–56. Dual-Regional Clocks



Combined Resources

Within each quadrant, there are 24 distinct dedicated clocking resources consisting of 16 global clock lines and eight regional clock lines. Multiplexers are used with these clocks to form buses to drive LAB row clocks, column IOE clocks, or row IOE clocks. Another multiplexer is used at the LAB level to select three of the six row clocks to feed the ALM registers in the LAB (refer to Figure 2–57).

Figure 2–57. Hierarchical Clock Networks Per Quadrant



You can use the Quartus II software to control whether a clock input pin drives either a GCLK, RCLK, or dual-RCLK network. The Quartus II software automatically selects the clocking resources if not specified.

Table 2–18. Arria GX PLL Features (Part 2 of 2)

Feature	Enhanced PLL	Fast PLL
Number of feedback clock inputs	One single-ended or differential *(7)*, *(8)*	—

Notes to Table 2–18:

(1) For enhanced PLLs, *m*, *n* range from 1 to 256 and post-scale counters range from 1 to 512 with 50% duty cycle.
(2) For fast PLLs, *m*, and post-scale counters range from 1 to 32. The *n* counter ranges from 1 to 4.
(3) The smallest phase shift is determined by the voltage controlled oscillator (V_{CO}) period divided by 8.
(4) For degree increments, Arria GX devices can shift all output frequencies in increments of at least 45. Smaller degree increments are possible depending on the frequency and divide parameters.
(5) Arria GX fast PLLs only support manual clock switchover.
(6) Fast PLLs can drive to any I/O pin as an external clock. For high-speed differential I/O pins, the device uses a data channel to generate `txclkout`.
(7) If the feedback input is used, you lose one (or two, if f_{BIN} is differential) external clock output pin.
(8) Every Arria GX device has at least two enhanced PLLs with one single-ended or differential external feedback input per PLL.

Figure 2–61 shows a top-level diagram of the Arria GX device and PLL floorplan.

Figure 2–61. PLL Locations

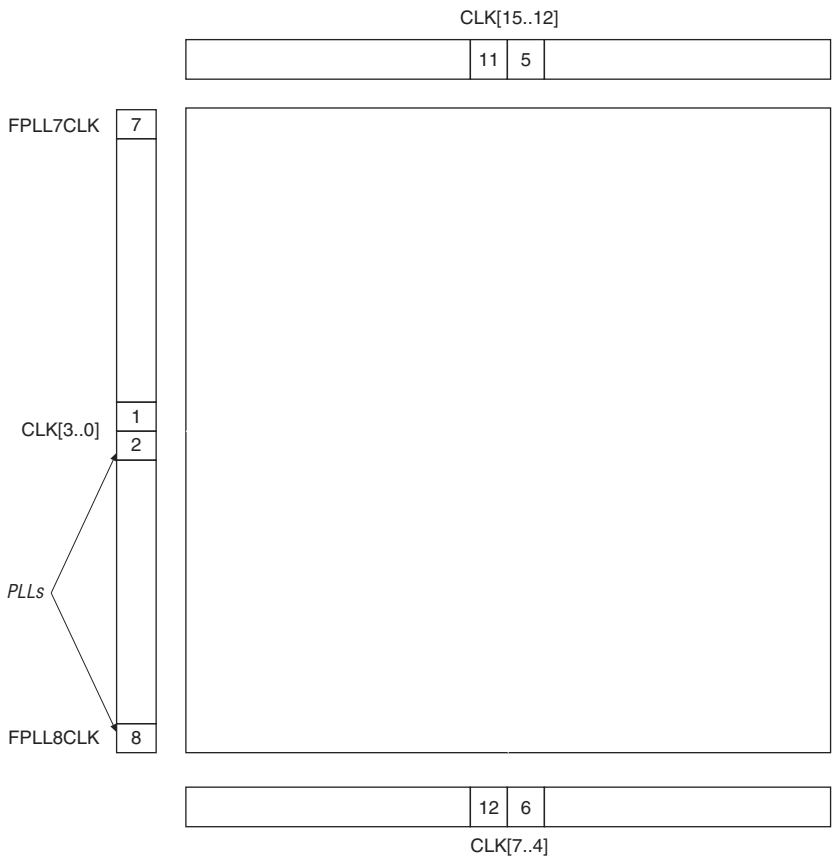
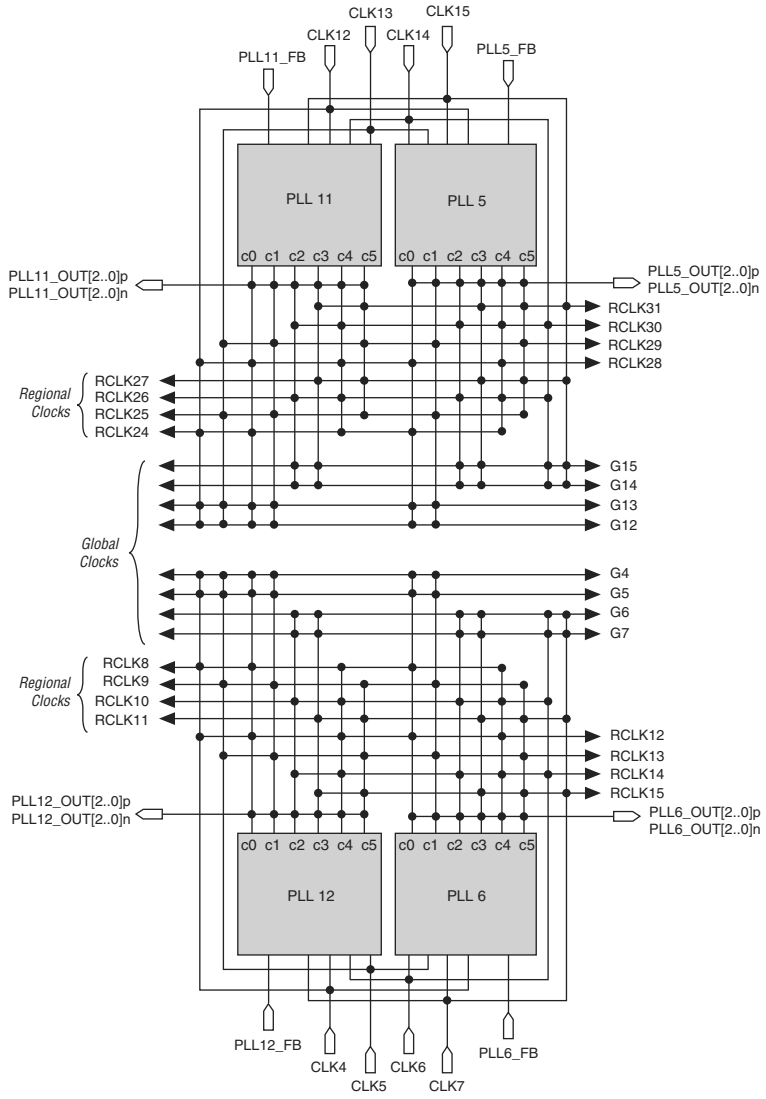


Figure 2–62 and Figure 2–63 shows global and regional clocking from the fast PLL outputs and side clock pins. The connections to the global and regional clocks from the fast PLL outputs, internal drivers, and `CLK` pins on the left side of the device are shown in Table 2–19.

Figure 2–64 shows the global and regional clocking from enhanced PLL outputs and top and bottom CLK pins.

Figure 2–64. Global and Regional Clock Connections from Top and Bottom Clock Pins and Enhanced PLL Outputs *(Note 1)*



Note to Figure 2–64:

(1) If the design uses the feedback input, you might lose one (or two if FBIN is differential) external clock output pin.

The connections to the global and regional clocks from the top clock pins and enhanced PLL outputs are shown in Table 2–20. The connections to the clocks from the bottom clock pins are shown in Table 2–21.

Table 4–6. Arria GX Transceiver Block AC Specification (Part 3 of 3)

Symbol / Description	Conditions	–6 Speed Grade Commercial and Industrial			Units
		Min	Typ	Max	
Transmitter PLL					
VCO frequency range	—	500	—	1562.5	MHz
Bandwidth at 3.125 Gbps	BW = Low	—	3	—	MHz
	BW = Med	—	5	—	
	BW = High	—	9	—	
Bandwidth at 2.5 Gbps	BW = Low	—	1	—	MHz
	BW = Med	—	2	—	
	BW = High	—	4	—	
TX PLL lock time from `gxb_powerdown` de-assertion *(9)*, *(14)*	—	—	—	100	us
PCS					
Interface speed per mode	—	25	—	156.25	MHz
Digital Reset Pulse Width	—	Minimum is 2 parallel clock cycles			—

Notes to Table 4–6:

(1) Spread spectrum clocking is allowed only in PCI Express (PIPE) mode if the upstream transmitter and the receiver share the same clock source.
(2) The reference clock DC coupling option is only available in PCI Express (PIPE) mode for the HCSL I/O standard.
(3) The `fixedclk` is used in PIPE mode receiver detect circuitry.
(4) The device cannot tolerate prolonged operation at this absolute maximum.
(5) The rate matcher supports only up to ± 300 PPM for PIPE mode and ± 100 PPM for GIGE mode.
(6) This parameter is measured by embedding the run length data in a PRBS sequence.
(7) Signal detect threshold detector circuitry is available only in PCI Express (PIPE mode).
(8) Time taken for `rx_pll_locked` to go high from `rx_analogreset` deassertion. Refer to Figure 4–1.
(9) For lock times specific to the protocols, refer to protocol characterization documents.
(10) Time for which the CDR needs to stay in LTR mode after `rx_pll_locked` is asserted and before `rx_locktodata` is asserted in manual mode. Refer to Figure 4–1.
(11) Time taken to recover valid data from GXB after the `rx_locktodata` signal is asserted in manual mode. Measurement results are based on PRBS31, for native data rates only. Refer to Figure 4–1.
(12) Time taken to recover valid data from GXB after the `rx_freqlocked` signal goes high in automatic mode. Measurement results are based on PRBS31, for native data rates only. Refer to Figure 4–2.
(13) This is applicable only to PCI Express (PIPE) ×4 and XAUI ×4 mode.
(14) Time taken to lock `TX PLL` from `gxb_powerdown` deassertion.
(15) The 1.2 V RX VICM settings is intended for DC-coupled LVDS links.

Figure 4–1 shows the lock time parameters in manual mode. Figure 4–2 shows the lock time parameters in automatic mode.

LTD = Lock to data
LTR = Lock to reference clock

Table 4–9. PCS Latency (Part 2 of 2) (Part 2 of 2)

Functional Mode	Configuration	Receiver PCS Latency									
		Word Aligner	Deskew FIFO	Rate Matcher *(3)*	8B/10B Decoder	Receiver State Machine	Byte Deserializer	Byte Order	Receiver Phase Comp FIFO	Receiver PIPE	Sum *(2)*
BASIC Single Width	8/10-bit channel width; with Rate Matcher	4–5	—	11–13	1	—	1	1	1–2	1	19–23
	8/10-bit channel width; without Rate Matcher	4–5	—	—	1	—	1	1	1–2	—	8–10
	16/20-bit channel width; with Rate Matcher	2–2.5	—	5.5–6.5	0.5	—	1	1	1–2	—	11–14
	16/20-bit channel width; without Rate Matcher	2–2.5	—	—	0.5	—	1	1	1–2	—	6–7

Notes to Table 4–9:

(1) The latency numbers are with respect to the PLD-transceiver interface clock cycles.

(2) The total latency number is rounded off in the Sum column.

(3) The rate matcher latency shown is the steady state latency. Actual latency may vary depending on the skip ordered set gap allowed by the protocol, actual PPM difference between the reference clocks, and so forth.

Table 4–10 through Table 4–13 show the typical V_{OD} for data rates from 600 Mbps to 3.125 Gbps. The specification is for measurement at the package ball.

Table 4–10. Typical V_{OD} Setting, TX Term = 100 Ω

V_{cc} HTX = 1.5 V	V_{OD} Setting (mV)				
	400	600	800	1000	1200
V_{OD} Typical (mV)	430	625	830	1020	1200

Table 4–11. Typical V_{OD} Setting, TX Term = 100 Ω

V_{cc} HTX = 1.2 V	V_{OD} Setting (mV)				
	320	480	640	800	960
V_{OD} Typical (mV)	344	500	664	816	960

Table 4–12. Typical Pre-Emphasis (First Post-Tap), *(Note 1)*

V_{cc} HTX = 1.5 V	First Post Tap Pre-Emphasis Level				
V_{OD} Setting (mV)	1	2	3	4	5
	TX Term = 100 Ω				
400	24%	62%	112%	184%	—
600	—	31%	56%	86%	122%
800	—	20%	35%	53%	73%

Table 4–27. SSTL-18 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	High-level output voltage	I_{OH} = –13.4 mA *(1)*	V_{CCIO} – 0.28	—	—	V
V_{OL}	Low-level output voltage	I_{OL} = 13.4 mA *(1)*	—	—	0.28	V

Note to Table 4–27:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Arria GX Architecture* chapter.

Table 4–28. SSTL-18 Class I & II Differential Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	1.71	1.8	1.89	V
V_{SWING} (DC)	DC differential input voltage	0.25	—	—	V
V_X (AC)	AC differential input cross point voltage	(V_{CCIO}/2) – 0.175	—	(V_{CCIO}/2) + 0.175	V
V_{SWING} (AC)	AC differential input voltage	0.5	—	—	V
V_{ISO}	Input clock signal offset voltage	—	0.5 V_{CCIO}	—	V
ΔV_{ISO}	Input clock signal offset voltage variation	—	200	—	mV
V_{OX} (AC)	AC differential cross point voltage	(V_{CCIO}/2) – 0.125	—	(V_{CCIO}/2) + 0.125	V

Table 4–29. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	2.375	2.5	2.625	V
V_{TT}	Termination voltage	—	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage	—	1.188	1.25	1.313	V
V_{IH} (DC)	High-level DC input voltage	—	V_{REF} + 0.18	—	3.0	V
V_{IL} (DC)	Low-level DC input voltage	—	–0.3	—	V_{REF} – 0.18	V
V_{IH} (AC)	High-level AC input voltage	—	V_{REF} + 0.35	—	—	V
V_{IL} (AC)	Low-level AC input voltage	—	—	—	V_{REF} – 0.35	V
V_{OH}	High-level output voltage	I_{OH} = –8.1 mA *(1)*	V_{TT} + 0.57	—		V
V_{OL}	Low-level output voltage	I_{OL} = 8.1 mA *(1)*	—	—	V_{TT} – 0.57	V

Note to Table 4–29:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Arria GX Architecture* chapter.

Table 4–30. SSTL-2 Class II Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	2.375	2.5	2.625	V
V_{TT}	Termination voltage	—	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage	—	1.188	1.25	1.313	V
V_{IH} (DC)	High-level DC input voltage	—	V_{REF} + 0.18	—	V_{CCIO} + 0.3	V

I/O Timing Measurement Methodology

Different I/O standards require different baseline loading techniques for reporting timing delays. Altera characterizes timing delays with the required termination for each I/O standard and with 0 pF (except for PCI and PCI-X which use 10 pF) loading and the timing is specified up to the output pin of the FPGA device. The Quartus II software calculates the I/O timing for each I/O standard with a default baseline loading as specified by the I/O standards.

The following measurements are made during device characterization. Altera measures clock-to-output delays (t_{CO}) at worst-case process, minimum voltage, and maximum temperature (PVT) for default loading conditions shown in Table 4–44.

Use the following equations to calculate clock pin to output pin timing for Arria GX devices:

Equation 4–1.

t_{CO} from clock pin to I/O pin = delay from clock pad to I/O output register + IOE output register clock-to-output delay + delay from output register to output pin + I/O output delay

t_{xz}/t_{zx} from clock pin to I/O pin = delay from clock pad to I/O output register + IOE output register clock-to-output delay + delay from output register to output pin + I/O output delay + output enable pin delay

Simulation using IBIS models is required to determine the delays on the PCB traces in addition to the output pin delay timing reported by the Quartus II software and the timing model in the device handbook.

1. Simulate the output driver of choice into the generalized test setup, using values from Table 4–44.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Standard Output Adder delays to yield the actual worst-case propagation delay (clock-to-output) of the PCB trace.

The Quartus II software reports the timing with the conditions shown in Table 4–44 using the above equation. Figure 4–7 shows the model of the circuit that is represented by the output timing of the Quartus II software.

Table 4–56. EP1AGX35 Row Pins Output Timing Parameters (Part 2 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
2.5 V	8 mA	GCLK	t_{CO}	2.656	2.656	5.775	ns
		GCLK PLL	t_{CO}	1.237	1.237	2.703	ns
2.5 V	12 mA	GCLK	t_{CO}	2.637	2.637	5.661	ns
		GCLK PLL	t_{CO}	1.218	1.218	2.589	ns
1.8 V	2 mA	GCLK	t_{CO}	2.829	2.829	7.052	ns
		GCLK PLL	t_{CO}	1.410	1.410	3.980	ns
1.8 V	4 mA	GCLK	t_{CO}	2.818	2.818	6.273	ns
		GCLK PLL	t_{CO}	1.399	1.399	3.201	ns
1.8 V	6 mA	GCLK	t_{CO}	2.707	2.707	5.972	ns
		GCLK PLL	t_{CO}	1.288	1.288	2.900	ns
1.8 V	8 mA	GCLK	t_{CO}	2.676	2.676	5.858	ns
		GCLK PLL	t_{CO}	1.257	1.257	2.786	ns
1.5 V	2 mA	GCLK	t_{CO}	2.789	2.789	6.551	ns
		GCLK PLL	t_{CO}	1.370	1.370	3.479	ns
1.5 V	4 mA	GCLK	t_{CO}	2.682	2.682	5.950	ns
		GCLK PLL	t_{CO}	1.263	1.263	2.878	ns
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.626	2.626	5.614	ns
		GCLK PLL	t_{CO}	1.207	1.207	2.542	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.602	2.602	5.538	ns
		GCLK PLL	t_{CO}	1.183	1.183	2.466	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.568	2.568	5.407	ns
		GCLK PLL	t_{CO}	1.149	1.149	2.335	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.614	2.614	5.556	ns
		GCLK PLL	t_{CO}	1.195	1.195	2.484	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.618	2.618	5.485	ns
		GCLK PLL	t_{CO}	1.199	1.199	2.413	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.594	2.594	5.468	ns
		GCLK PLL	t_{CO}	1.175	1.175	2.396	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.597	2.597	5.447	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.375	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.595	2.595	5.466	ns
		GCLK PLL	t_{CO}	1.176	1.176	2.394	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.598	2.598	5.430	ns
		GCLK PLL	t_{CO}	1.179	1.179	2.358	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.580	2.580	5.426	ns
		GCLK PLL	t_{CO}	1.161	1.161	2.354	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.584	2.584	5.415	ns
		GCLK PLL	t_{CO}	1.165	1.165	2.343	ns

Table 4–57. EP1AGX35 Column Pins Output Timing Parameters (Part 3 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
SSTL-2 CLASS II	24 mA	GCLK	t_{CO}	2.587	2.587	5.624	ns
		GCLK PLL	t_{CO}	1.142	1.142	2.512	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.626	2.626	5.733	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.627	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.630	2.630	5.694	ns
		GCLK PLL	t_{CO}	1.185	1.185	2.582	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.609	2.609	5.675	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.563	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.614	2.614	5.673	ns
		GCLK PLL	t_{CO}	1.169	1.169	2.561	ns
SSTL-18 CLASS I	12 mA	GCLK	t_{CO}	2.608	2.608	5.659	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.547	ns
SSTL-18 CLASS II	8 mA	GCLK	t_{CO}	2.597	2.597	5.625	ns
		GCLK PLL	t_{CO}	1.152	1.152	2.513	ns
SSTL-18 CLASS II	16 mA	GCLK	t_{CO}	2.609	2.609	5.603	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.491	ns
SSTL-18 CLASS II	18 mA	GCLK	t_{CO}	2.605	2.605	5.611	ns
		GCLK PLL	t_{CO}	1.160	1.160	2.499	ns
SSTL-18 CLASS II	20 mA	GCLK	t_{CO}	2.605	2.605	5.609	ns
		GCLK PLL	t_{CO}	1.160	1.160	2.497	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.629	2.629	5.664	ns
		GCLK PLL	t_{CO}	1.187	1.187	2.558	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.634	2.634	5.649	ns
		GCLK PLL	t_{CO}	1.189	1.189	2.537	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.612	2.612	5.638	ns
		GCLK PLL	t_{CO}	1.167	1.167	2.526	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.616	2.616	5.644	ns
		GCLK PLL	t_{CO}	1.171	1.171	2.532	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.608	2.608	5.637	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.525	ns
1.8-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.591	2.591	5.401	ns
		GCLK PLL	t_{CO}	1.146	1.146	2.289	ns
1.8-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.593	2.593	5.412	ns
		GCLK PLL	t_{CO}	1.148	1.148	2.300	ns
1.8-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.593	2.593	5.421	ns
		GCLK PLL	t_{CO}	1.148	1.148	2.309	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.629	2.629	5.663	ns
		GCLK PLL	t_{CO}	1.187	1.187	2.557	ns

Table 4–62. EP1AGX50 Row Pins Output Timing Parameters (Part 3 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.606	2.606	5.480	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.396	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.608	2.608	5.442	ns
		GCLK PLL	t_{CO}	1.181	1.181	2.360	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.590	2.590	5.438	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.356	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.594	2.594	5.427	ns
		GCLK PLL	t_{CO}	1.167	1.167	2.345	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.585	2.585	5.426	ns
		GCLK PLL	t_{CO}	1.158	1.158	2.344	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.605	2.605	5.457	ns
		GCLK PLL	t_{CO}	1.177	1.177	2.373	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.607	2.607	5.441	ns
		GCLK PLL	t_{CO}	1.180	1.180	2.359	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.592	2.592	5.433	ns
		GCLK PLL	t_{CO}	1.165	1.165	2.351	ns
LVDS	—	GCLK	t_{CO}	2.654	2.654	5.613	ns
		GCLK PLL	t_{CO}	1.226	1.226	2.530	ns

Table 4–63 lists I/O timing specifications.

Table 4–63. EP1AGX50 Column Pins Output Timing Parameters (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	2.948	2.948	6.608	ns
		GCLK PLL	t_{CO}	1.476	1.476	3.447	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.797	2.797	6.203	ns
		GCLK PLL	t_{CO}	1.331	1.331	3.075	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.722	2.722	6.204	ns
		GCLK PLL	t_{CO}	1.264	1.264	3.075	ns
3.3-V LVTTL	16 mA	GCLK	t_{CO}	2.694	2.694	6.024	ns
		GCLK PLL	t_{CO}	1.238	1.238	2.906	ns
3.3-V LVTTL	20 mA	GCLK	t_{CO}	2.670	2.670	5.896	ns
		GCLK PLL	t_{CO}	1.216	1.216	2.781	ns
3.3-V LVTTL	24 mA	GCLK	t_{CO}	2.660	2.660	5.895	ns
		GCLK PLL	t_{CO}	1.209	1.209	2.783	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.797	2.797	6.203	ns
		GCLK PLL	t_{CO}	1.331	1.331	3.075	ns

Table 4–69 lists I/O timing specifications.

Table 4–69. EP1AGX60 Column Pins Output Timing Parameters (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	3.036	3.036	6.963	ns
		GCLK PLL	t_{CO}	1.466	1.466	3.528	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.891	2.891	6.591	ns
		GCLK PLL	t_{CO}	1.321	1.321	3.156	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.824	2.824	6.591	ns
		GCLK PLL	t_{CO}	1.254	1.254	3.156	ns
3.3-V LVTTL	16 mA	GCLK	t_{CO}	2.798	2.798	6.422	ns
		GCLK PLL	t_{CO}	1.228	1.228	2.987	ns
3.3-V LVTTL	20 mA	GCLK	t_{CO}	2.776	2.776	6.297	ns
		GCLK PLL	t_{CO}	1.206	1.206	2.862	ns
3.3-V LVTTL	24 mA	GCLK	t_{CO}	2.769	2.769	6.299	ns
		GCLK PLL	t_{CO}	1.199	1.199	2.864	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.891	2.891	6.591	ns
		GCLK PLL	t_{CO}	1.321	1.321	3.156	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.799	2.799	6.296	ns
		GCLK PLL	t_{CO}	1.229	1.229	2.861	ns
3.3-V LVCMOS	12 mA	GCLK	t_{CO}	2.771	2.771	6.218	ns
		GCLK PLL	t_{CO}	1.201	1.201	2.783	ns
3.3-V LVCMOS	16 mA	GCLK	t_{CO}	2.778	2.778	6.186	ns
		GCLK PLL	t_{CO}	1.208	1.208	2.751	ns
3.3-V LVCMOS	20 mA	GCLK	t_{CO}	2.765	2.765	6.168	ns
		GCLK PLL	t_{CO}	1.195	1.195	2.733	ns
3.3-V LVCMOS	24 mA	GCLK	t_{CO}	2.754	2.754	6.146	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.711	ns
2.5 V	4 mA	GCLK	t_{CO}	2.853	2.853	6.623	ns
		GCLK PLL	t_{CO}	1.283	1.283	3.188	ns
2.5 V	8 mA	GCLK	t_{CO}	2.801	2.801	6.361	ns
		GCLK PLL	t_{CO}	1.231	1.231	2.926	ns
2.5 V	12 mA	GCLK	t_{CO}	2.780	2.780	6.244	ns
		GCLK PLL	t_{CO}	1.210	1.210	2.809	ns
2.5 V	16 mA	GCLK	t_{CO}	2.762	2.762	6.170	ns
		GCLK PLL	t_{CO}	1.192	1.192	2.735	ns
1.8 V	2 mA	GCLK	t_{CO}	2.893	2.893	7.615	ns
		GCLK PLL	t_{CO}	1.323	1.323	4.180	ns
1.8 V	4 mA	GCLK	t_{CO}	2.898	2.898	6.841	ns
		GCLK PLL	t_{CO}	1.328	1.328	3.406	ns

Table 4–105. Arria GX Maximum Output Toggle Rate for Column I/O Pins (Part 2 of 3)

I/O Standards	Drive Strength	–6 Speed Grade	Units
3.3-V LVCMOS	4 mA	215	MHz
	8 mA	411	MHz
	12 mA	626	MHz
	16 mA	819	MHz
	20 mA	874	MHz
	24 mA	934	MHz
2.5 V	4 mA	168	MHz
	8 mA	355	MHz
	12 mA	514	MHz
	16 mA	766	MHz
1.8 V	2 mA	97	MHz
	4 mA	215	MHz
	6 mA	336	MHz
	8 mA	486	MHz
	10 mA	706	MHz
	12 mA	925	MHz
1.5 V	2 mA	168	MHz
	4 mA	303	MHz
	6 mA	350	MHz
	8 mA	392	MHz
SSTL-2 CLASS I	8 mA	280	MHz
	12 mA	327	MHz
SSTL-2 CLASS II	16 mA	280	MHz
	20 mA	327	MHz
	24 mA	327	MHz
SSTL-18 CLASS I	4 mA	140	MHz
	6 mA	186	MHz
	8 mA	280	MHz
	10 mA	373	MHz
	12 mA	373	MHz
SSTL-18 CLASS II	8 mA	140	MHz
	16 mA	327	MHz
	18 mA	373	MHz
	20 mA	420	MHz
1.8-V HSTL CLASS I	4 mA	280	MHz
	6 mA	420	MHz
	8 mA	561	MHz
	10 mA	561	MHz
	12 mA	607	MHz

Table 4–117. Fast PLL Specifications (Part 2 of 2)

Name	Description	Min	Typ	Max	Units
$t_{ARESET\_RECONFIG}$	Minimum pulse width on the areset signal when using PLL reconfiguration. Reset the PLL after scandone goes high.	500	—	—	ns

Note to Table 4–117:

(1) This is limited by the I/O f_{MAX}.

External Memory Interface Specifications

Table 4–118 through Table 4–122 list Arria GX device specifications for the dedicated circuitry used for interfacing with external memory devices.

Table 4–118. DLL Frequency Range Specifications

Frequency Mode	Frequency Range (MHz)
0	100 to 175
1	150 to 230
2	200 to 310

Table 4–119. DQS Jitter Specifications for DLL-Delayed Clock (tDQS_JITTER) , *(Note 1)*

Number of DQS Delay Buffer Stages *(2)*	Commercial (ps)	Industrial (ps)
1	80	110
2	110	130
3	130	180
4	160	210

Notes to Table 4–119:

(1) Peak-to-peak period jitter on the phase-shifted DQS clock. For example, jitter on two delay stages under commercial conditions is 200 ps peak-to-peak or 100 ps.

(2) Delay stages used for requested DQS phase shift are reported in a project's Compilation Report in the Quartus II software.

Table 4–120. DQS Phase-Shift Error Specifications for DLL-Delayed Clock (t_{DQS_PSERR})

Number of DQS Delay Buffer Stages	–6 Speed Grade (ps)
1	35
2	70
3	105
4	140