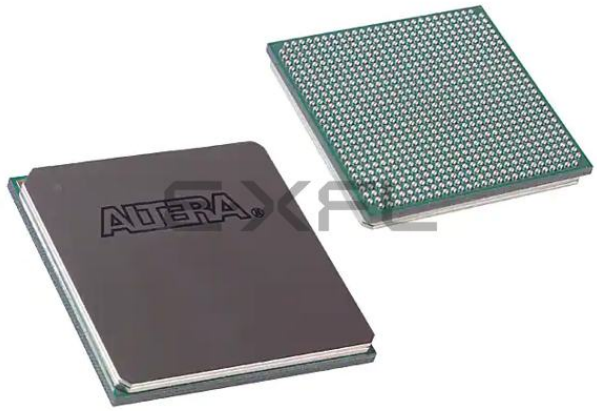
Intel - EP1AGX35DF780C6N Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1676
Number of Logic Elements/Cells	33520
Total RAM Bits	1348416
Number of I/O	341
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1agx35df780c6n

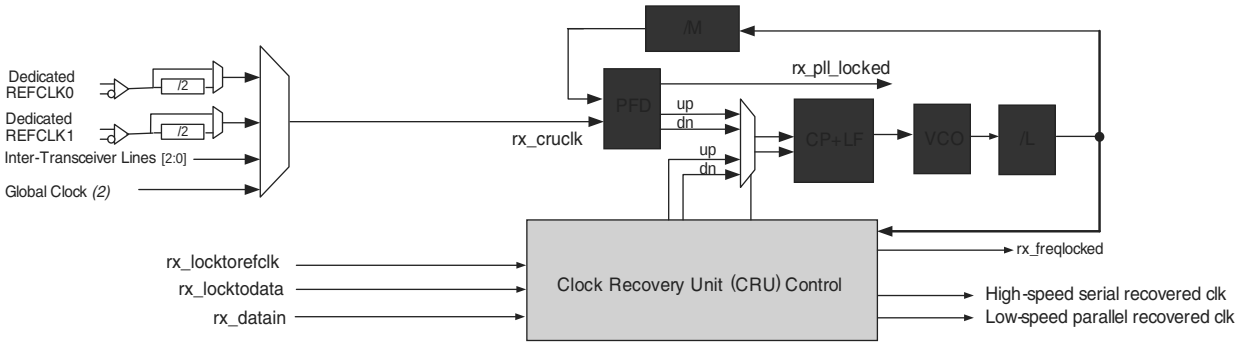
The receiver equalization circuit is comprised of a programmable amplifier. Each stage is a peaking equalizer with a different center frequency and programmable gain. This allows varying amounts of gain to be applied, depending on the overall frequency response of the channel loss. Channel loss is defined as the summation of all losses through the PCB traces, vias, connectors, and cables present in the physical link. The Quartus II software allows five equalization settings for Arria GX devices.

Receiver PLL and Clock Recovery Unit (CRU)

Each transceiver block has four receiver PLLs and CRU units, each of which is dedicated to a receiver channel. The receiver PLL is fed by an input reference clock. The receiver PLL, in conjunction with the CRU, generates two clocks: a high-speed serial recovered clock that clocks the deserializer and a low-speed parallel recovered clock that clocks the receiver's digital logic.

Figure 2–13 shows a block diagram of the receiver PLL and CRU circuits.

Figure 2–13. Receiver PLL and Clock Recovery Unit



Notes to Figure 2–13:

(1) You only need to select the protocol and the available input reference clock frequency in the ALTGXB MegaWizard Plug-In Manager. Based on your selections, the ALTGXB MegaWizard Plug-In Manager automatically selects the necessary /M and /L dividers.

(2) The global clock line must be driven from an input pin only.

The reference clock input to the receiver PLL can be derived from:

- One of the two available dedicated reference clock input pins (`REFCLK0` or `REFCLK1`) of the associated transceiver block
- PLD global clock network (must be driven directly from an input clock pin and cannot be driven by user logic or enhanced PLL)
- Inter-transceiver block lines driven by reference clock input pins of other transceiver blocks

All the parameters listed are programmable in the Quartus II software. The receiver PLL has the following features:

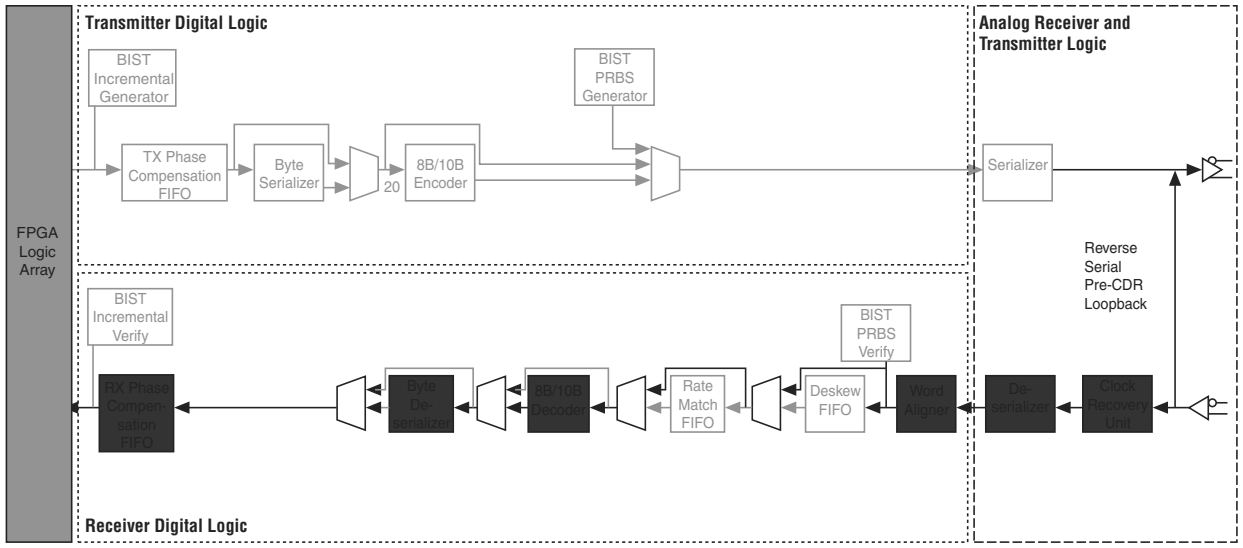
- Operates from 600 Mbps to 3.125 Gbps.
- Uses a reference clock between 50 MHz and 622.08 MHz.
- Programmable bandwidth settings: low, medium, and high.
- Programmable `rx_locktorefclk` (forces the receiver PLL to lock to reference clock) and `rx_locktodata` (forces the receiver PLL to lock to data).

Reverse Serial Pre-CDR Loopback

Reverse serial pre-CDR loopback mode uses the analog portion of the transceiver. An external source (pattern generator or transceiver) generates the source data. The high-speed serial source data arrives at the high-speed differential receiver input buffer, loops back before the CRU unit, and is transmitted though the high-speed differential transmitter output buffer. It is for test or verification use only to verify the signal being received after the gain and equalization improvements of the input buffer. The signal at the output is not exactly what is received because the signal goes through the output buffer and the V_{OD} is changed to the V_{OD} setting level. Pre-emphasis settings have no effect.

Figure 2–20 shows the Arria GX block in reverse serial pre-CDR loopback mode.

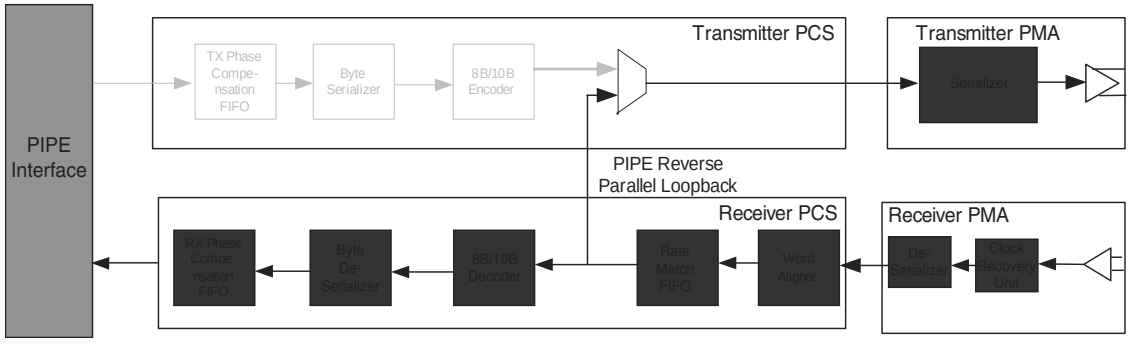
Figure 2–20. Arria GX Block in Reverse Serial Pre-CDR Loopback Mode



PCI Express (PIPE) Reverse Parallel Loopback

Figure 2–21 shows the data path for PCI Express (PIPE) reverse parallel loopback. The reverse parallel loopback configuration is compliant with the PCI Express (PIPE) specification and is available only on PCI Express (PIPE) mode.

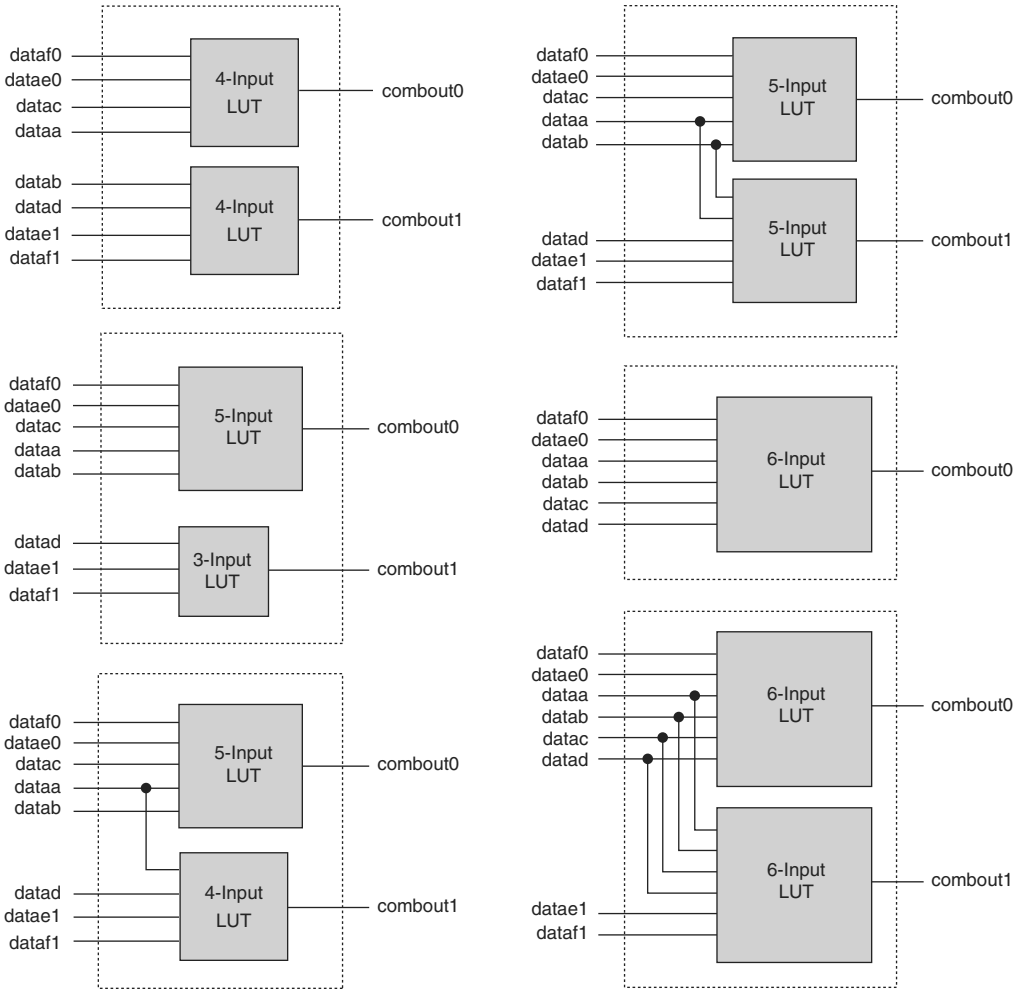
Figure 2–21. PCI Express (PIPE) Reverse Parallel Loopback



Normal Mode

Normal mode is suitable for general logic applications and combinational functions. In this mode, up to eight data inputs from the LAB local interconnect are inputs to the combinational logic. Normal mode allows two functions to be implemented in one Arria GX ALM, or an ALM to implement a single function of up to six inputs. The ALM can support certain combinations of completely independent functions and various combinations of functions which have common inputs. Figure 2–30 shows the supported LUT combinations in normal mode.

Figure 2–30. ALM in Normal Mode *(Note 1)*



Note to Figure 2–30:

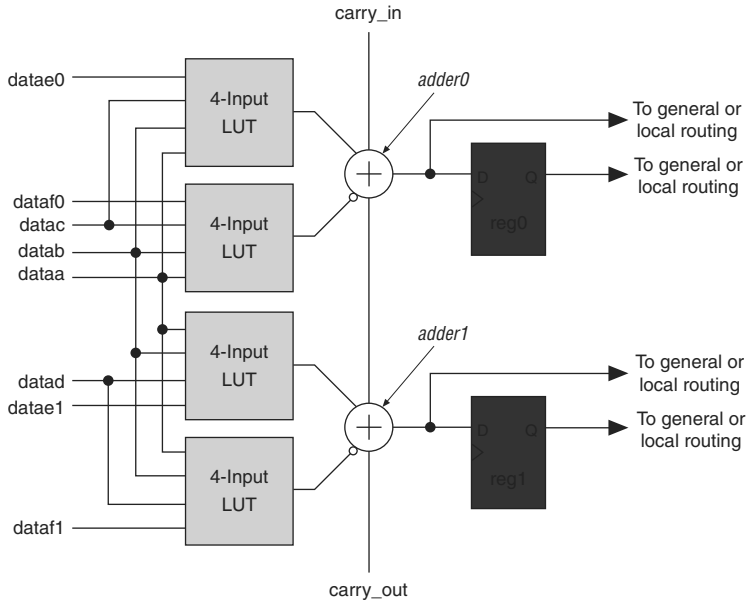
(1) Combinations of functions with less inputs than those shown are also supported. For example, combinations of functions with the following number of inputs are supported: 4 and 3, 3 and 3, 3 and 2, 5 and 2, and so on.

Normal mode provides complete backward compatibility with four-input LUT architectures. Two independent functions of four inputs or less can be implemented in one Arria GX ALM. In addition, a five-input function and an independent three-input function can be implemented without sharing inputs.

Arithmetic Mode

Arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. An ALM in arithmetic mode uses two sets of 2 four-input LUTs along with two dedicated full adders. The dedicated adders allow the LUTs to be available to perform pre-adder logic; therefore, each adder can add the output of two four-input functions. The four LUTs share the `dataa` and `datab` inputs. As shown in Figure 2–34, the carry-in signal feeds to `adder0`, and the carry-out from `adder0` feeds to carry-in of `adder1`. The carry-out from `adder1` drives to `adder0` of the next ALM in the LAB. ALMs in arithmetic mode can drive out registered and/or unregistered versions of the adder outputs.

Figure 2–34. ALM in Arithmetic Mode



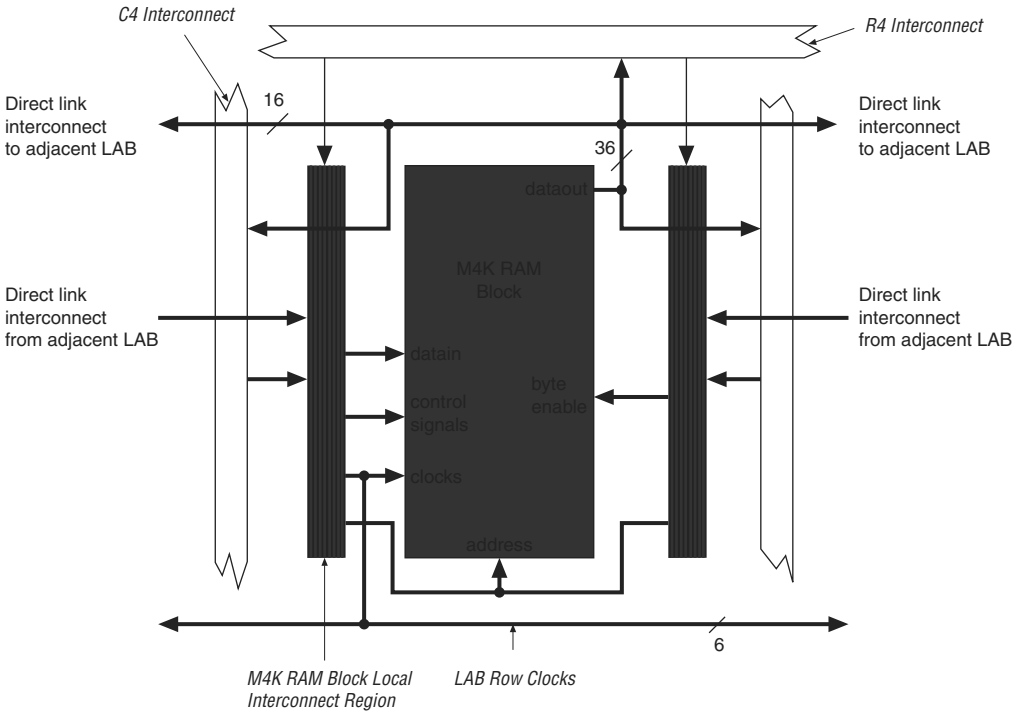
While operating in arithmetic mode, the ALM can support simultaneous use of the adder's carry output along with combinational logic outputs. In this operation, adder output is ignored. This usage of the adder with the combinational logic output provides resource savings of up to 50% for functions that can use this ability. An example of such functionality is a conditional operation, such as the one shown in Figure 2–35. The equation for this example is:

Equation 2–1.

$$R = (X < Y) ? Y : X$$

To implement this function, the adder is used to subtract 'Y' from 'X.' If 'X' is less than 'Y,' the `carry_out` signal is '1.' The `carry_out` signal is fed to an adder where it drives out to the LAB local interconnect. It then feeds to the LAB-wide `syncload` signal. When asserted, `syncload` selects the `syncdata` input. In this case, the data 'Y' drives the `syncdata` inputs to the registers. If 'X' is greater than or equal to 'Y,' the `syncload` signal is deasserted and 'X' drives the data port of the registers.

Figure 2–45. M4K RAM Block LAB Row Interface



M-RAM Block

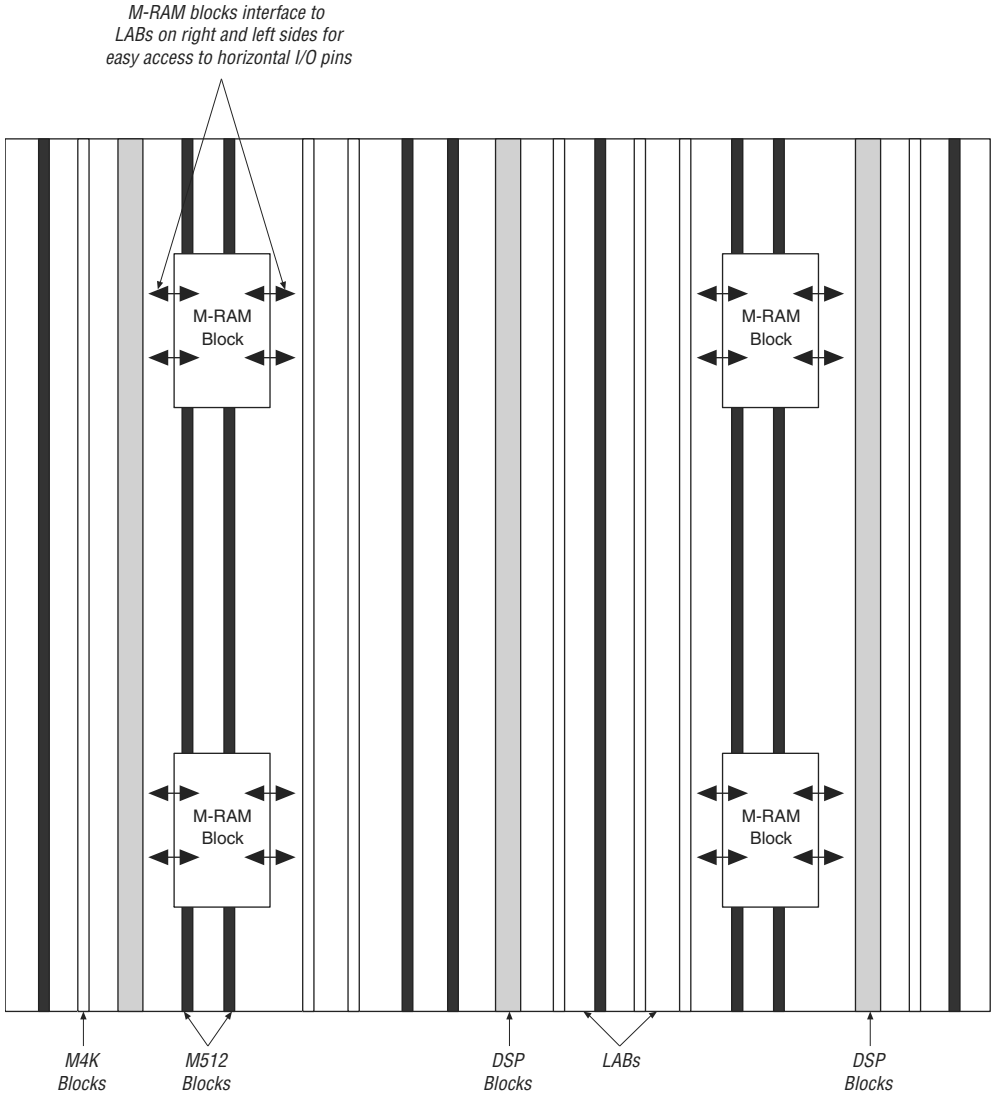
The largest TriMatrix memory block, the M-RAM block, is useful for applications where a large volume of data must be stored on-chip. Each block contains 589,824 RAM bits (including parity bits). The M-RAM block can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO

You cannot use an initialization file to initialize the contents of a M-RAM block. All M-RAM block contents power up to an undefined value. Only synchronous operation is supported in the M-RAM block, so all inputs are registered. Output registers can be bypassed.

Similar to all RAM blocks, M-RAM blocks can have different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M-RAM block registers (`renwe`, `address`, byte enable, `datain`, and output registers). You can bypass the output register. The six `labclk` signals or local interconnect can drive the control signals for the A and B ports of the M-RAM block. ALMs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, `clr_b`, `clocken_a`, and `clocken_b` signals, as shown in Figure 2–46.

Figure 2–47. EP1AGX90 Device with M-RAM Interface Locations *(Note 1)*



Note to Figure 2–47:

(1) The device shown is an EP1AGX90 device. The number and position of M-RAM blocks vary in other devices.

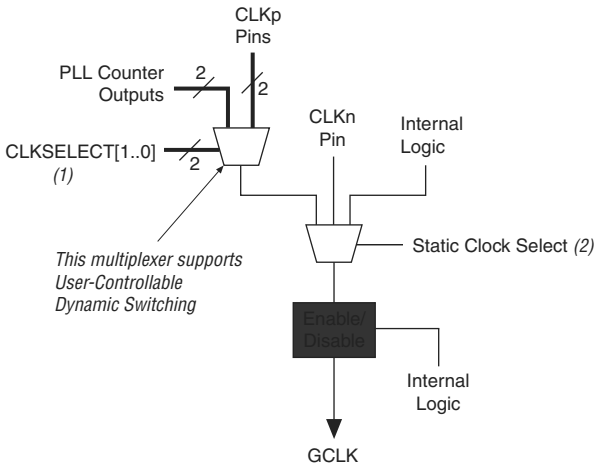
Clock Control Block

Each GCLK, RCLK, and PLL external clock output has its own clock control block. The control block has two functions:

- Clock source selection (dynamic selection for global clocks)
- Clock power-down (dynamic clock enable or disable)

Figure 2–58 through Figure 2–60 show the clock control block for the global clock, regional clock, and PLL external clock output, respectively.

Figure 2–58. Global Clock Control Blocks

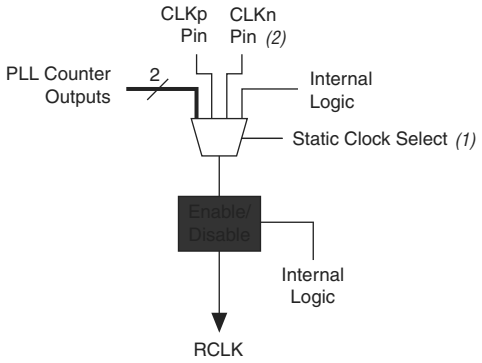


Notes to Figure 2–58:

(1) These clock select signals can be dynamically controlled through internal logic when the device is operating in user mode.

(2) These clock select signals can only be set through a configuration file (SRAM Object File [**.sof**] or Programmer Object File [**.pof**]) and cannot be dynamically controlled during user mode operation.

Figure 2–59. Regional Clock Control Blocks



Notes to Figure 2–59:

(1) These clock select signals can only be set through a configuration file (**.sof** or **.pof**) and cannot be dynamically controlled during user mode operation.

(2) Only the `CLKn` pins on the top and bottom of the device feed to regional clock select.

Enhanced and Fast PLLs

Arria GX devices provide robust clock management and synthesis using up to four enhanced PLLs and four fast PLLs. These PLLs increase performance and provide advanced clock interfacing and clock frequency synthesis. With features such as clock switchover, spread spectrum clocking, reconfigurable bandwidth, phase control, and reconfigurable phase shifting, the Arria GX device's enhanced PLLs provide you with complete control of your clocks and system timing. The fast PLLs provide general purpose clocking with multiplication and phase shifting as well as high-speed outputs for high-speed differential I/O support. Enhanced and fast PLLs work together with the Arria GX high-speed I/O and advanced clock architecture to provide significant improvements in system performance and bandwidth.

The Quartus II software enables the PLLs and their features without requiring any external devices. Table 2–17 lists the PLLs available for each Arria GX device and their type.

Table 2–17. Arria GX Device PLL Availability *(Note 1)*, *(2)*

Device	Fast PLLs								Enhanced PLLs			
	1	**2**	**3** *(3)*	**4** *(3)*	**7**	**8**	**9** *(3)*	**10** *(3)*	**5**	**6**	**11**	**12**
EP1AGX20	✓	✓	—	—	—	—	—	—	✓	✓	—	—
EP1AGX35	✓	✓	—	—	—	—	—	—	✓	✓	—	—
EP1AGX50 *(4)*	✓	✓	—	—	✓	✓	—	—	✓	✓	✓	✓
EP1AGX60 *(5)*	✓	✓	—	—	✓	✓	—	—	✓	✓	✓	✓
EP1AGX90	✓	✓	—	—	✓	✓	—	—	✓	✓	✓	✓

Notes to Table 2–17:

(1) The global or regional clocks in a fast PLL's transceiver block can drive the fast PLL input. A pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

(2) EP1AGX20C, EP1AGX35C/D, EP1AGX50C and EP1AGX60C/D devices only have two fast PLLs (PLLs 1 and 2), but the connectivity from these two PLLs to the global and regional clock networks remains the same as shown in this table.

(3) PLLs 3, 4, 9, and 10 are not available in Arria GX devices.

(4) 4 or 8 PLLs are available depending on C or D device and the package option.

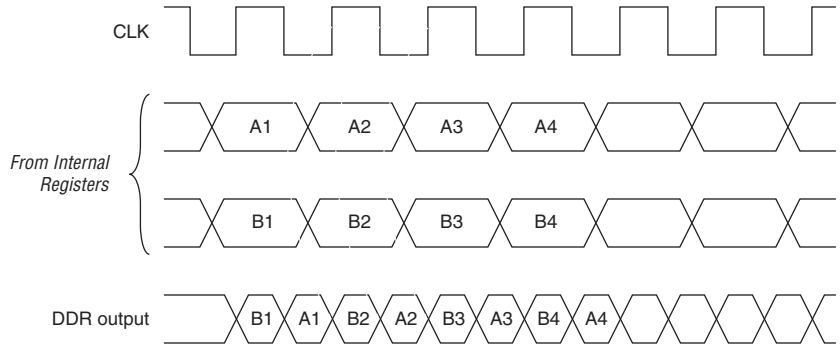
(5) 4or 8 PLLs are available depending on C, D, or E device option.

Table 2–18 lists the enhanced PLL and fast PLL features in Arria GX devices.

Table 2–18. Arria GX PLL Features (Part 1 of 2)

Feature	Enhanced PLL	Fast PLL
Clock multiplication and division	*m*/(*n* × post-scale counter) *(1)*	*m*/(*n* × post-scale counter) *(2)*
Phase shift	Down to 125-ps increments *(3)*, *(4)*	Down to 125-ps increments *(3)*, *(4)*
Clock switchover	✓	✓ *(5)*
PLL reconfiguration	✓	✓
Reconfigurable bandwidth	✓	✓
Spread spectrum clocking	✓	—
Programmable duty cycle	✓	✓
Number of internal clock outputs	6	4
Number of external clock outputs	Three differential/six single-ended	*(6)*

Figure 2–76. Output Timing Diagram in DDR Mode



The Arria GX IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations. The negative-edge-clocked OE register holds the OE signal inactive until the falling edge of the clock to meet DDR SDRAM timing requirements.

External RAM Interfacing

In addition to the six I/O registers in each IOE, Arria GX devices also have dedicated phase-shift circuitry for interfacing with external memory interfaces, including DDR, DDR2 SDRAM, and SDR SDRAM. In every Arria GX device, the I/O banks at the top (Banks 3 and 4) and bottom (Banks 7 and 8) of the device support DQ and DQS signals with DQ bus modes of ×4, ×8/×9, ×16/×18, or ×32/×36. Table 2–23 shows the number of DQ and DQS buses that are supported per device.

Table 2–23. DQS and DQ Bus Mode Support *(Note 1)*

Device	Package	Number of ×4 Groups	Number of ×8/×9 Groups	Number of ×16/×18 Groups	Number of ×32/×36 Groups
EP1AGX20	484-pin FineLine BGA	2	0	0	0
EP1AGX35	484-pin FineLine BGA	2	0	0	0
	780-pin FineLine BGA	18	8	4	0
EP1AGX50/60	484-pin FineLine BGA	2	0	0	0
	780-pin FineLine BGA	18	8	4	0
	1,152-pin FineLine BGA	36	18	8	4
EP1AGX90	1,152-pin FineLine BGA	36	18	8	4

Note to Table 2–23:

(1) Numbers are preliminary until devices are available.

A compensated delay element on each DQS pin automatically aligns input DQS synchronization signals with the data window of their corresponding DQ data signals. The DQS signals drive a local DQS bus in the top and bottom I/O banks. This DQS bus is an additional resource to the I/O clocks and is used to clock DQ input registers with the DQS signal.

Table 2–29. Supported TDO/TDI Voltage Combinations

Device	TDI Input Buffer Power	Arria GX TDO V_{CCIO} Voltage Level in I/O Bank 4				
		V_{CCIO} = 3.3 V	V_{CCIO} = 2.5 V	V_{CCIO} = 1.8 V	V_{CCIO} = 1.5 V	V_{CCIO} = 1.2 V
Arria GX	Always V_{CCPD} (3.3 V)	✓ *(1)*	✓ *(2)*	✓ *(3)*	Level shifter required	Level shifter required
Non-Arria GX	VCC = 3.3 V	✓ *(1)*	✓ *(2)*	✓ *(3)*	Level shifter required	Level shifter required
	VCC = 2.5 V	✓ *(1)*, *(4)*	✓ *(2)*	✓ *(3)*	Level shifter required	Level shifter required
	VCC = 1.8 V	✓ *(1)*, *(4)*	✓ *(2)*, *(5)*	✓	Level shifter required	Level shifter required
	VCC = 1.5 V	✓ *(1)*, *(4)*	✓ *(2)*, *(5)*	✓ *(6)*	✓	✓

Notes to Table 2–29:

(1) The TDO output buffer meets V_{OH} (MIN) = 2.4 V.
(2) The TDO output buffer meets V_{OH} (MIN) = 2.0 V.
(3) An external 250-Ω pull-up resistor is not required, but recommended if signal levels on the board are not optimal.
(4) Input buffer must be 3.3-V tolerant.
(5) Input buffer must be 2.5-V tolerant.
(6) Input buffer must be 1.8-V tolerant.

High-Speed Differential I/O with DPA Support

Arria GX devices contain dedicated circuitry for supporting differential standards at speeds up to 840 Mbps. LVDS differential I/O standards are supported in the Arria GX device. In addition, the LVPECL I/O standard is supported on input and output clock pins on the top and bottom I/O banks.

The high-speed differential I/O circuitry supports the following high-speed I/O interconnect standards and applications:

- SPI-4 Phase 2 (POS-PHY Level 4)
- SFI-4
- Parallel RapidIO standard

There are two dedicated high-speed PLLs (PLL1 and PLL2) in the EP1AGX20 and EP1AGX35 devices and up to four dedicated high-speed PLLs (PLL1, PLL2, PLL7, and PLL8) in the EP1AGX50, EP1AGX60, and EP1AGX90 devices to multiply reference clocks and drive high-speed differential SERDES channels in I/O banks 1 and 2.

Table 2–30 through Table 2–34 list the number of channels that each fast PLL can clock in each of the Arria GX devices. In Table 2–30 through Table 2–34 the first row for each transmitter or receiver provides the maximum number of channels that each fast PLL can drive in its adjacent I/O bank (I/O Bank 1 **or** I/O Bank 2). The second row shows the maximum number of channels that each fast PLL can drive in both I/O banks (I/O Bank 1 **and** I/O Bank 2). For example, in the 780-pin FineLine BGA EP1AGX20

Table 4–6. Arria GX Transceiver Block AC Specification (Part 2 of 3)

Symbol / Description	Conditions	–6 Speed Grade Commercial and Industrial			Units
		Min	Typ	Max	
Bandwidth at 2.5 Gbps	BW = Low	—	35	—	MHz
	BW = Med	—	50	—	
	BW = High	—	60	—	
Return loss differential mode	50 MHz to 1.25 GHz (PCI Express)	–10			dB
	100 MHz to 2.5 GHz (XAUI)				
Return loss common mode	50 MHz to 1.25 GHz (PCI Express)	–6			dB
	100 MHz to 2.5 GHz (XAUI)				
Programmable PPM detector *(5)*	—	± 62.5, 100, 125, 200, 250, 300, 500, 1000			PPM
Run length *(6)*	—	80			UI
Programmable equalization	—	—	—	5	dB
Signal detect/loss threshold *(7)*	—	65	—	175	mV
CDR LTR TIme *(8)*, *(9)*	—	—	—	75	us
CDR Minimum T1b *(9)*, *(10)*	—	15	—	—	us
LTD lock time *(9)*, *(11)*	—	0	100	4000	ns
Data lock time from `rx_freqlocked` *(9)*, *(12)*	—	—	—	4	us
Programmable DC gain	—	0, 3, 6			dB
Transmitter Buffer					
Output Common Mode voltage (V_{ocm})	—	580 ± 10%			mV
On-chip termination resistors	—	108±10%			Ω
Return loss differential mode	50 MHz to 1.25 GHz (PCI Express)	–10			dB
	312 MHz to 625 MHz (XAUI)				
	625 MHz to 3.125GHz (XAUI)	–10			$\frac{dB}{decade\ slope}$
Return loss common mode	50 MHz to 1.25 GHz (PCI Express)	–6			dB
Rise time	—	35	—	65	ps
Fall time	—	35	—	65	ps
Intra differential pair skew	V_{OD} = 800 mV	—	—	15	ps
Intra-transceiver block skew (×4) *(13)*	—	—	—	100	ps

Table 4–27. SSTL-18 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	High-level output voltage	I_{OH} = –13.4 mA *(1)*	V_{CCIO} – 0.28	—	—	V
V_{OL}	Low-level output voltage	I_{OL} = 13.4 mA *(1)*	—	—	0.28	V

Note to Table 4–27:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Arria GX Architecture* chapter.

Table 4–28. SSTL-18 Class I & II Differential Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	1.71	1.8	1.89	V
V_{SWING} (DC)	DC differential input voltage	0.25	—	—	V
V_X (AC)	AC differential input cross point voltage	(V_{CCIO}/2) – 0.175	—	(V_{CCIO}/2) + 0.175	V
V_{SWING} (AC)	AC differential input voltage	0.5	—	—	V
V_{ISO}	Input clock signal offset voltage	—	0.5 V_{CCIO}	—	V
ΔV_{ISO}	Input clock signal offset voltage variation	—	200	—	mV
V_{OX} (AC)	AC differential cross point voltage	(V_{CCIO}/2) – 0.125	—	(V_{CCIO}/2) + 0.125	V

Table 4–29. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	2.375	2.5	2.625	V
V_{TT}	Termination voltage	—	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage	—	1.188	1.25	1.313	V
V_{IH} (DC)	High-level DC input voltage	—	V_{REF} + 0.18	—	3.0	V
V_{IL} (DC)	Low-level DC input voltage	—	–0.3	—	V_{REF} – 0.18	V
V_{IH} (AC)	High-level AC input voltage	—	V_{REF} + 0.35	—	—	V
V_{IL} (AC)	Low-level AC input voltage	—	—	—	V_{REF} – 0.35	V
V_{OH}	High-level output voltage	I_{OH} = –8.1 mA *(1)*	V_{TT} + 0.57	—		V
V_{OL}	Low-level output voltage	I_{OL} = 8.1 mA *(1)*	—	—	V_{TT} – 0.57	V

Note to Table 4–29:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Arria GX Architecture* chapter.

Table 4–30. SSTL-2 Class II Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	2.375	2.5	2.625	V
V_{TT}	Termination voltage	—	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage	—	1.188	1.25	1.313	V
V_{IH} (DC)	High-level DC input voltage	—	V_{REF} + 0.18	—	V_{CCIO} + 0.3	V

Table 4–30. SSTL-2 Class II Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IL} (DC)	Low-level DC input voltage	—	–0.3	—	V_{REF} – 0.18	V
V_{IH} (AC)	High-level AC input voltage	—	V_{REF} + 0.35	—	—	V
V_{IL} (AC)	Low-level AC input voltage	—	—	—	V_{REF} – 0.35	V
V_{OH}	High-level output voltage	I_{OH} = –16.4 mA *(1)*	V_{TT} + 0.76	—	—	V
V_{OL}	Low-level output voltage	I_{OL} = 16.4 mA *(1)*	—	—	V_{TT} – 0.76	V

Note to Table 4–30:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Arria GX Architecture* chapter.

Table 4–31. SSTL-2 Class I & II Differential Specifications *(Note 1)*

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	2.375	2.5	2.625	V
V_{SWING} (DC)	DC differential input voltage	0.36	—	—	V
V_X (AC)	AC differential input cross point voltage	(V_{CCIO}/2) – 0.2	—	(V_{CCIO}/2) + 0.2	V
V_{SWING} (AC)	AC differential input voltage	0.7	—	—	V
V_{ISO}	Input clock signal offset voltage	—	0.5 V_{CCIO}	—	V
ΔV_{ISO}	Input clock signal offset voltage variation	—	200	—	mV
V_{OX} (AC)	AC differential output cross point voltage	(V_{CCIO}/2) – 0.2	—	(V_{CCIO}/2) + 0.2	V

Note to Table 4–31:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Arria GX Architecture* chapter.

Table 4–32. 1.2-V HSTL Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	1.14	1.2	1.26	V
V_{REF}	Reference voltage	0.48 V_{CCIO}	0.5 V_{CCIO}	0.52 V_{CCIO}	V
V_{IH} (DC)	High-level DC input voltage	V_{REF} + 0.08	—	V_{CCIO} + 0.15	V
V_{IL} (DC)	Low-level DC input voltage	–0.15	—	V_{REF} – 0.08	V
V_{IH} (AC)	High-level AC input voltage	V_{REF} + 0.15	—	V_{CCIO} + 0.24	V
V_{IL} (AC)	Low-level AC input voltage	–0.24	—	V_{REF} – 0.15	V
V_{OH}	High-level output voltage	V_{REF} + 0.15	—	V_{CCIO} + 0.15	V
V_{OL}	Low-level output voltage	–0.15	—	V_{REF} – 0.15	V

EP1AGX35 I/O Timing Parameters

Table 4–54 through Table 4–57 list the maximum I/O timing parameters for EP1AGX35 devices for I/O standards which support general purpose I/O pins.

Table 4–54 lists I/O timing specifications.

Table 4–54. EP1AGX35 Row Pins Input Timing Parameters (Part 1 of 2)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.561	1.561	3.556	ns
		t_H	–1.456	–1.456	–3.279	ns
	GCLK PLL	t_{SU}	2.980	2.980	6.628	ns
		t_H	–2.875	–2.875	–6.351	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.561	1.561	3.556	ns
		t_H	–1.456	–1.456	–3.279	ns
	GCLK PLL	t_{SU}	2.980	2.980	6.628	ns
		t_H	–2.875	–2.875	–6.351	ns
2.5 V	GCLK	t_{SU}	1.573	1.573	3.537	ns
		t_H	–1.468	–1.468	–3.260	ns
	GCLK PLL	t_{SU}	2.992	2.992	6.609	ns
		t_H	–2.887	–2.887	–6.332	ns
1.8 V	GCLK	t_{SU}	1.639	1.639	3.744	ns
		t_H	–1.534	–1.534	–3.467	ns
	GCLK PLL	t_{SU}	3.058	3.058	6.816	ns
		t_H	–2.953	–2.953	–6.539	ns
1.5 V	GCLK	t_{SU}	1.642	1.642	3.839	ns
		t_H	–1.537	–1.537	–3.562	ns
	GCLK PLL	t_{SU}	3.061	3.061	6.911	ns
		t_H	–2.956	–2.956	–6.634	ns
SSTL-2 CLASS I	GCLK	t_{SU}	1.385	1.385	3.009	ns
		t_H	–1.280	–1.280	–2.732	ns
	GCLK PLL	t_{SU}	2.804	2.804	6.081	ns
		t_H	–2.699	–2.699	–5.804	ns
SSTL-2 CLASS II	GCLK	t_{SU}	1.385	1.385	3.009	ns
		t_H	–1.280	–1.280	–2.732	ns
	GCLK PLL	t_{SU}	2.804	2.804	6.081	ns
		t_H	–2.699	–2.699	–5.804	ns
SSTL-18 CLASS I	GCLK	t_{SU}	1.417	1.417	3.118	ns
		t_H	–1.312	–1.312	–2.841	ns
	GCLK PLL	t_{SU}	2.836	2.836	6.190	ns
		t_H	–2.731	–2.731	–5.913	ns

Table 4–63. EP1AGX50 Column Pins Output Timing Parameters (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.695	2.695	5.893	ns
		GCLK PLL	t_{CO}	1.239	1.239	2.780	ns
3.3-V LVCMOS	12 mA	GCLK	t_{CO}	2.663	2.663	5.809	ns
		GCLK PLL	t_{CO}	1.211	1.211	2.702	ns
3.3-V LVCMOS	16 mA	GCLK	t_{CO}	2.666	2.666	5.776	ns
		GCLK PLL	t_{CO}	1.218	1.218	2.670	ns
3.3-V LVCMOS	20 mA	GCLK	t_{CO}	2.651	2.651	5.758	ns
		GCLK PLL	t_{CO}	1.205	1.205	2.652	ns
3.3-V LVCMOS	24 mA	GCLK	t_{CO}	2.638	2.638	5.736	ns
		GCLK PLL	t_{CO}	1.194	1.194	2.630	ns
2.5 V	4 mA	GCLK	t_{CO}	2.754	2.754	6.240	ns
		GCLK PLL	t_{CO}	1.293	1.293	3.107	ns
2.5 V	8 mA	GCLK	t_{CO}	2.697	2.697	5.963	ns
		GCLK PLL	t_{CO}	1.241	1.241	2.845	ns
2.5 V	12 mA	GCLK	t_{CO}	2.672	2.672	5.837	ns
		GCLK PLL	t_{CO}	1.220	1.220	2.728	ns
2.5 V	16 mA	GCLK	t_{CO}	2.654	2.654	5.760	ns
		GCLK PLL	t_{CO}	1.202	1.202	2.654	ns
1.8 V	2 mA	GCLK	t_{CO}	2.804	2.804	7.295	ns
		GCLK PLL	t_{CO}	1.333	1.333	4.099	ns
1.8 V	4 mA	GCLK	t_{CO}	2.808	2.808	6.479	ns
		GCLK PLL	t_{CO}	1.338	1.338	3.325	ns
1.8 V	6 mA	GCLK	t_{CO}	2.717	2.717	6.195	ns
		GCLK PLL	t_{CO}	1.262	1.262	3.061	ns
1.8 V	8 mA	GCLK	t_{CO}	2.719	2.719	6.098	ns
		GCLK PLL	t_{CO}	1.264	1.264	2.970	ns
1.8 V	10 mA	GCLK	t_{CO}	2.671	2.671	6.012	ns
		GCLK PLL	t_{CO}	1.218	1.218	2.893	ns
1.8 V	12 mA	GCLK	t_{CO}	2.671	2.671	5.953	ns
		GCLK PLL	t_{CO}	1.219	1.219	2.836	ns
1.5 V	2 mA	GCLK	t_{CO}	2.779	2.779	6.815	ns
		GCLK PLL	t_{CO}	1.313	1.313	3.629	ns
1.5 V	4 mA	GCLK	t_{CO}	2.703	2.703	6.210	ns
		GCLK PLL	t_{CO}	1.249	1.249	3.060	ns
1.5 V	6 mA	GCLK	t_{CO}	2.705	2.705	6.118	ns
		GCLK PLL	t_{CO}	1.252	1.252	2.942	ns
1.5 V	8 mA	GCLK	t_{CO}	2.660	2.660	6.014	ns
		GCLK PLL	t_{CO}	1.211	1.211	2.889	ns

Table 4–66. EP1AGX60 Row Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.281	1.281	2.777	ns
		t_H	–1.176	–1.176	–2.500	ns
	GCLK PLL	t_{SU}	2.853	2.853	6.220	ns
		t_H	–2.748	–2.748	–5.943	ns
LVDS	GCLK	t_{SU}	1.208	1.208	2.664	ns
		t_H	–1.103	–1.103	–2.387	ns
	GCLK PLL	t_{SU}	2.767	2.767	6.083	ns
		t_H	–2.662	–2.662	–5.806	ns

Table 4–67 lists I/O timing specifications.

Table 4–67. EP1AGX60 Column Pins Input Timing Parameters (Part 1 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.124	1.124	2.493	ns
		t_H	–1.019	–1.019	-2.216	ns
	GCLK PLL	t_{SU}	2.694	2.694	5.928	ns
		t_H	–2.589	–2.589	-5.651	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.124	1.124	2.493	ns
		t_H	–1.019	–1.019	-2.216	ns
	GCLK PLL	t_{SU}	2.694	2.694	5.928	ns
		t_H	–2.589	–2.589	-5.651	ns
2.5 V	GCLK	t_{SU}	1.134	1.134	2.475	ns
		t_H	–1.029	–1.029	-2.198	ns
	GCLK PLL	t_{SU}	2.704	2.704	5.910	ns
		t_H	–2.599	–2.599	-5.633	ns
1.8 V	GCLK	t_{SU}	1.200	1.200	2.685	ns
		t_H	–1.095	–1.095	-2.408	ns
	GCLK PLL	t_{SU}	2.770	2.770	6.120	ns
		t_H	–2.665	–2.665	-5.843	ns
1.5 V	GCLK	t_{SU}	1.203	1.203	2.778	ns
		t_H	–1.098	–1.098	-2.501	ns
	GCLK PLL	t_{SU}	2.773	2.773	6.213	ns
		t_H	–2.668	–2.668	-5.936	ns
SSTL-2 CLASS I	GCLK	t_{SU}	0.948	0.948	1.951	ns
		t_H	–0.843	–0.843	-1.674	ns
	GCLK PLL	t_{SU}	2.519	2.519	5.388	ns
		t_H	–2.414	–2.414	-5.111	ns

Table 4–72 lists I/O timing specifications.

Table 4–72. EP1AGX90 Row Pins Input Timing Parameters (Part 1 of 2)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.295	1.295	2.873	ns
		t_H	–1.190	–1.190	–2.596	ns
	GCLK PLL	t_{SU}	3.366	3.366	7.017	ns
		t_H	–3.261	–3.261	–6.740	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.295	1.295	2.873	ns
		t_H	–1.190	–1.190	–2.596	ns
	GCLK PLL	t_{SU}	3.366	3.366	7.017	ns
		t_H	–3.261	–3.261	–6.740	ns
2.5 V	GCLK	t_{SU}	1.307	1.307	2.854	ns
		t_H	–1.202	–1.202	–2.577	ns
	GCLK PLL	t_{SU}	3.378	3.378	6.998	ns
		t_H	–3.273	–3.273	–6.721	ns
1.8 V	GCLK	t_{SU}	1.381	1.381	3.073	ns
		t_H	–1.276	–1.276	–2.796	ns
	GCLK PLL	t_{SU}	3.434	3.434	7.191	ns
		t_H	–3.329	–3.329	–6.914	ns
1.5 V	GCLK	t_{SU}	1.384	1.384	3.168	ns
		t_H	–1.279	–1.279	–2.891	ns
	GCLK PLL	t_{SU}	3.437	3.437	7.286	ns
		t_H	–3.332	–3.332	–7.009	ns
SSTL-2 CLASS I	GCLK	t_{SU}	1.121	1.121	2.329	ns
		t_H	–1.016	–1.016	–2.052	ns
	GCLK PLL	t_{SU}	3.187	3.187	6.466	ns
		t_H	–3.082	–3.082	–6.189	ns
SSTL-2 CLASS II	GCLK	t_{SU}	1.121	1.121	2.329	ns
		t_H	–1.016	–1.016	–2.052	ns
	GCLK PLL	t_{SU}	3.187	3.187	6.466	ns
		t_H	–3.082	–3.082	–6.189	ns
SSTL-18 CLASS I	GCLK	t_{SU}	1.159	1.159	2.447	ns
		t_H	–1.054	–1.054	–2.170	ns
	GCLK PLL	t_{SU}	3.212	3.212	6.565	ns
		t_H	–3.107	–3.107	–6.288	ns
SSTL-18 CLASS II	GCLK	t_{SU}	1.157	1.157	2.441	ns
		t_H	–1.052	–1.052	–2.164	ns
	GCLK PLL	t_{SU}	3.235	3.235	6.597	ns
		t_H	–3.130	–3.130	–6.320	ns

Table 4–77 lists column pin delay adders when using the regional clock in Arria GX devices.

Table 4–77. EP1AGX90 Column Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.138	0.138	0.354	ns
RCLK PLL input adder	–1.697	–1.697	–3.607	ns
RCLK output adder	–0.138	–0.138	–0.353	ns
RCLK PLL output adder	1.966	1.966	5.188	ns

Dedicated Clock Pin Timing

Table 4–79 through Table 4–98 list clock pin timing for Arria GX devices when the clock is driven by the global clock, regional clock, periphery clock, and a PLL.

Table 4–78 lists Arria GX clock timing parameters.

Table 4–78. Arria GX Clock Timing Parameters

Symbol	Parameter
t_{CIN}	Delay from clock pad to I/O input register
t_{COUT}	Delay from clock pad to I/O output register
t_{PLLCIN}	Delay from PLL inclk pad to I/O input register
$t_{PLLCOUT}$	Delay from PLL inclk pad to I/O output register

EP1AGX20 Clock Timing Parameters

Table 4–79 through Table 4–80 list the GCLK clock timing parameters for EP1AGX20 devices.

Table 4–79 lists clock timing specifications.

Table 4–79. EP1AGX20 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
tcin	1.394	1.394	3.161	ns
tcout	1.399	1.399	3.155	ns
tpllcin	–0.027	–0.027	0.091	ns
tpllcout	–0.022	–0.022	0.085	ns

Table 4–99 lists performance notes.

Table 4–99. Arria GX Performance Notes

Applications		Resources Used			Performance
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	–6 Speed Grade
LE	16-to-1 multiplexer	5	0	0	168.41
	32-to-1 multiplexer	11	0	0	334.11
	16-bit counter	16	0	0	374.0
	64-bit counter	64	0	0	168.41
TriMatrix Memory M512 block	Simple dual-port RAM 32 x 18 bit	0	1	0	348.0
	FIFO 32 x 18 bit	0	1	0	333.22
TriMatrix Memory M4K block	Simple dual-port RAM 128 x 36 bit	0	1	0	344.71
	True dual-port RAM 128 x 18 bit	0	1	0	348.0
TriMatrix Memory MegaRAM block	Single port RAM 4K x 144 bit	0	2	0	244.0
	Simple dual-port RAM 4K x 144 bit	0	1	0	292.0
	True dual-port RAM 4K x 144 bit	0	2	0	244.0
	Single port RAM 8K x 72 bit	0	1	0	247.0
	Simple dual-port RAM 8K x 72 bit	0	1	0	292.0
	Single port RAM 16K x 36 bit	0	1	0	254.0
	Simple dual-port RAM 16K x 36 bit	0	1	0	292.0
	True dual-port RAM 16K x 36 bit	0	1	0	251.0
	Single port RAM 32K x 18 bit	0	1	0	317.36
	Simple dual-port RAM 32K x 18 bit	0	1	0	292.0
	True dual-port RAM 32K x 18 bit	0	1	0	251.0
	Single port RAM 64K x 9 bit	0	1	0	254.0
	Simple dual-port RAM 64K x 9 bit	0	1	0	292.0
	True dual-port RAM 64K x 9 bit	0	1	0	251.0

To calculate the DCD as a percentage:

(T/2 – DCD) / T = (3,745 ps/2 – 125 ps) / 3,745 ps = 46.66% (for low boundary)

(T/2 + DCD) / T = (3,745 ps/2 + 125 ps) / 3,745 ps = 53.33% (for high boundary)

Therefore, the DCD percentage for the output clock at 267 MHz is from 46.66% to 53.33%.

Table 4–109. Maximum DCD for Non-DDIO Output on Column I/O Pins

Column I/O Output Standard I/O Standard	Maximum DCD (ps) for Non-DDIO Output	Units
	–6 Speed Grade	
3.3-V LVTTL	220	ps
3.3-V LVCMOS	175	ps
2.5 V	155	ps
1.8 V	110	ps
1.5-V LVCMOS	215	ps
SSTL-2 Class I	135	ps
SSTL-2 Class II	130	ps
SSTL-18 Class I	115	ps
SSTL-18 Class II	100	ps
1.8-V HSTL Class I	110	ps
1.8-V HSTL Class II	110	ps
1.5-V HSTL Class I	115	ps
1.5-V HSTL Class II	80	ps
1.2-V HSTL-12	200	ps
LVPECL	80	ps

Table 4–110. Maximum DCD for DDIO Output on Row I/O Pins Without PLL in the Clock Path *Note (1)*

Maximum DCD (ps) for Row DDIO Output I/O Standard	Input I/O Standard (No PLL in the Clock Path)					Units
	TTL/CMOS		SSTL-2	SSTL/HSTL	LVDS	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	3.3V	
3.3-V LVTTL	440	495	170	160	105	ps
3.3-V LVCMOS	390	450	120	110	75	ps
2.5 V	375	430	105	95	90	ps
1.8 V	325	385	90	100	135	ps
1.5-V LVCMOS	430	490	160	155	100	ps
SSTL-2 Class I	355	410	85	75	85	ps
SSTL-2 Class II	350	405	80	70	90	ps
SSTL-18 Class I	335	390	65	65	105	ps
1.8-V HSTL Class I	330	385	60	70	110	ps
1.5-V HSTL Class I	330	390	60	70	105	ps