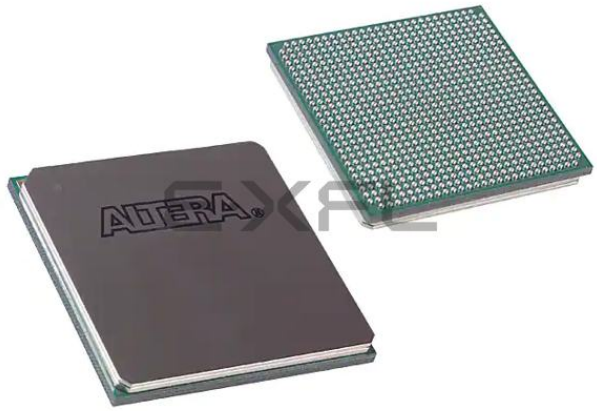

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1676
Number of Logic Elements/Cells	33520
Total RAM Bits	1348416
Number of I/O	341
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	780-BBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1agx35df780i6

Table 1–2. Arria GX Package Options (Pin Counts and Transceiver Channels) (Part 2 of 2)

Device	Transceiver Channels	Source-Synchronous Channels		Maximum User I/O Pin Count		
		Receive	Transmit	484-Pin FBGA (23 mm)	780-Pin FBGA (29 mm)	1152-Pin FBGA (35 mm)
EP1AGX60D	8	31	29	—	350	—
EP1AGX60E	12	42	42	—	—	514
EP1AGX90E	12	47	45	—	—	538

Table 1–3 lists the Arria GX device package sizes.

Table 1–3. Arria GX FBGA Package Sizes

Dimension	484 Pins	780 Pins	1152 Pins
Pitch (mm)	1.00	1.00	1.00
Area (mm^2)	529	841	1225
Length × width (mm × mm)	23 × 23	29 × 29	35 × 35

Document Revision History

Table 1–4 lists the revision history for this chapter.

Table 1–4. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
December 2009, v2.0	■ Document template update. ■ Minor text edits.	—
May 2008, v1.2	Included support for SDI, SerialLite II, and XAUI.	—
June 2007, v1.1	Included GIGE information.	—
May 2007, v1.0	Initial Release	—

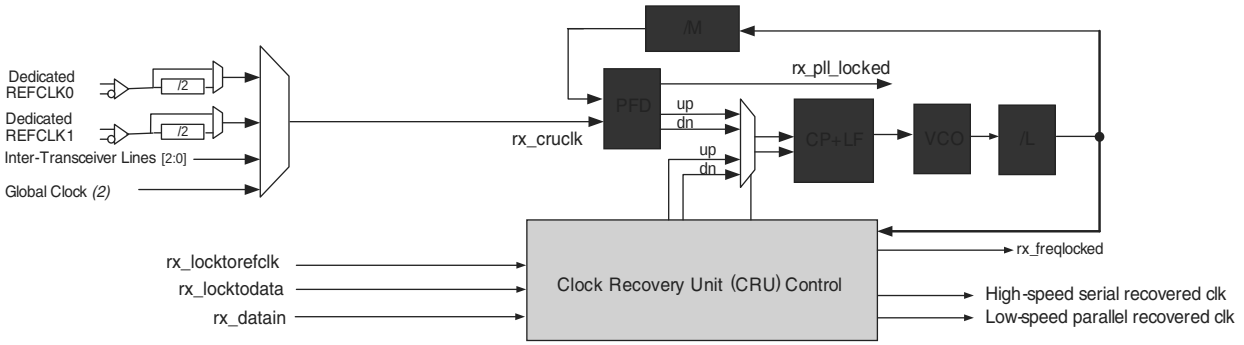
The receiver equalization circuit is comprised of a programmable amplifier. Each stage is a peaking equalizer with a different center frequency and programmable gain. This allows varying amounts of gain to be applied, depending on the overall frequency response of the channel loss. Channel loss is defined as the summation of all losses through the PCB traces, vias, connectors, and cables present in the physical link. The Quartus II software allows five equalization settings for Arria GX devices.

Receiver PLL and Clock Recovery Unit (CRU)

Each transceiver block has four receiver PLLs and CRU units, each of which is dedicated to a receiver channel. The receiver PLL is fed by an input reference clock. The receiver PLL, in conjunction with the CRU, generates two clocks: a high-speed serial recovered clock that clocks the deserializer and a low-speed parallel recovered clock that clocks the receiver's digital logic.

Figure 2–13 shows a block diagram of the receiver PLL and CRU circuits.

Figure 2–13. Receiver PLL and Clock Recovery Unit



Notes to Figure 2–13:

(1) You only need to select the protocol and the available input reference clock frequency in the ALTGXB MegaWizard Plug-In Manager. Based on your selections, the ALTGXB MegaWizard Plug-In Manager automatically selects the necessary /M and /L dividers.

(2) The global clock line must be driven from an input pin only.

The reference clock input to the receiver PLL can be derived from:

- One of the two available dedicated reference clock input pins (`REFCLK0` or `REFCLK1`) of the associated transceiver block
- PLD global clock network (must be driven directly from an input clock pin and cannot be driven by user logic or enhanced PLL)
- Inter-transceiver block lines driven by reference clock input pins of other transceiver blocks

All the parameters listed are programmable in the Quartus II software. The receiver PLL has the following features:

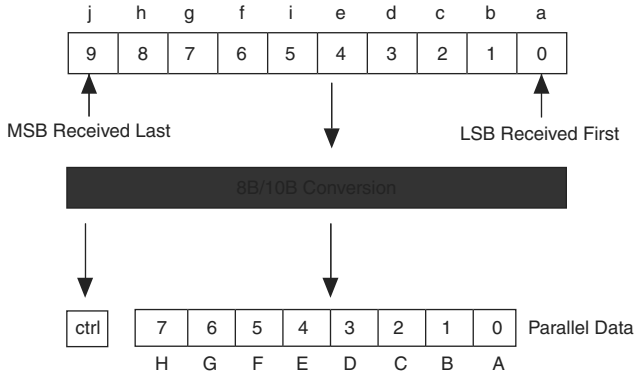
- Operates from 600 Mbps to 3.125 Gbps.
- Uses a reference clock between 50 MHz and 622.08 MHz.
- Programmable bandwidth settings: low, medium, and high.
- Programmable `rx_locktorefclk` (forces the receiver PLL to lock to reference clock) and `rx_locktodata` (forces the receiver PLL to lock to data).

8B/10B Decoder

The 8B/10B decoder is used in all supported functional modes. The 8B/10B decoder takes in 10-bit data from the rate matcher and decodes it into 8-bit data + 1-bit control identifier, thereby restoring the original transmitted data at the receiver. The 8B/10B decoder indicates whether the received 10-bit character is a data or control code through the `rx_ctrldetect` port. If the received 10-bit code group is a control character (`Kx.y`), the `rx_ctrldetect` signal is driven high and if it is a data character (`Dx.y`), the `rx_ctrldetect` signal is driven low.

Figure 2–17 shows a 10-bit code group decoded to an 8-bit data and a 1-bit control indicator.

Figure 2–17. 10-Bit to 8-Bit Conversion



If the received 10-bit code is not a part of valid Dx.y or Kx.y code groups, the 8B/10B decoder block asserts an error flag on the `rx_errdetect` port. If the received 10-bit code is detected with incorrect running disparity, the 8B/10B decoder block asserts an error flag on the `rx_disperr` and `rx_errdetect` ports. The error flag signals (`rx_errdetect` and `rx_disperr`) have the same data path delay from the 8B/10B decoder to the PLD-transceiver interface as the bad code group.

Receiver State Machine

The receiver state machine operates in Basic, GIGE, PCI Express (PIPE), and XAUI modes. In GIGE mode, the receiver state machine replaces invalid code groups with K30.7. In XAUI mode, the receiver state machine translates the XAUI PCS code group to the XAUI XGMII code group.

Table 2–10 lists the routing scheme for Arria GX device.

Table 2–10. Arria GX Device Routing Scheme

Source	Destination															
	Shared Arithmetic Chain	Carry Chain	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	R24 Interconnect	C4 Interconnect	C16 Interconnect	ALM	M512 RAM Block	M4K RAM Block	M-RAM Block	DSP Blocks	Column IOE	Row IOE
Shared arithmetic chain	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—
Carry chain	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—
Register chain	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—
Local interconnect	—	—	—	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓
Direct link interconnect	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—
R4 interconnect	—	—	—	✓	—	✓	✓	✓	✓	—	—	—	—	—	—	—
R24 interconnect	—	—	—	—	—	✓	✓	✓	✓	—	—	—	—	—	—	—
C4 interconnect	—	—	—	✓	—	✓	—	✓	—	—	—	—	—	—	—	—
C16 interconnect	—	—	—	—	—	✓	✓	✓	✓	—	—	—	—	—	—	—
ALM	✓	✓	✓	✓	✓	✓	—	✓	—	—	—	—	—	—	—	—
M512 RAM block	—	—	—	✓	✓	✓	—	✓	—	—	—	—	—	—	—	—
M4K RAM block	—	—	—	✓	✓	✓	—	✓	—	—	—	—	—	—	—	—
M-RAM block	—	—	—	—	✓	✓	✓	✓	—	—	—	—	—	—	—	—
DSP blocks	—	—	—	—	✓	✓	—	✓	—	—	—	—	—	—	—	—
Column IOE	—	—	—	—	✓	—	—	✓	✓	—	—	—	—	—	—	—
Row IOE	—	—	—	—	✓	✓	✓	✓	—	—	—	—	—	—	—	—

TriMatrix Memory

TriMatrix memory consists of three types of RAM blocks: M512, M4K, and M-RAM. Although these memory blocks are different, they can all implement various types of memory with or without parity, including true dual-port, simple dual-port, and single-port RAM, ROM, and FIFO buffers. Table 2–11 lists the size and features of the different RAM blocks.

Table 2–11. TriMatrix Memory Features (Part 1 of 2)

Memory Feature	M512 RAM Block (32 × 18 Bits)	M4K RAM Block (128 × 36 Bits)	M-RAM Block (4K × 144 Bits)
Maximum performance	345 MHz	380 MHz	290 MHz
True dual-port memory	—	✓	✓
Simple dual-port memory	✓	✓	✓
Single-port memory	✓	✓	✓
Shift register	✓	✓	—

Table 2–11. TriMatrix Memory Features (Part 2 of 2)

Memory Feature	M512 RAM Block (32 × 18 Bits)	M4K RAM Block (128 × 36 Bits)	M-RAM Block (4K × 144 Bits)
ROM	✓	✓	—
FIFO buffer	✓	✓	✓
Pack mode	—	✓	✓
Byte enable	✓	✓	✓
Address clock enable	—	✓	✓
Parity bits	✓	✓	✓
Mixed clock mode	✓	✓	✓
Memory initialization file (**.mif**)	✓	✓	—
Simple dual-port memory mixed width support	✓	✓	✓
True dual-port memory mixed width support	—	✓	✓
Power-up conditions	Outputs cleared	Outputs cleared	Outputs unknown
Register clears	Output registers	Output registers	Output registers
Mixed-port read-during-write	Unknown output/old data	Unknown output/old data	Unknown output
Configurations	512 × 1 256 × 2 128 × 4 64 × 8 64 × 9 32 × 16 32 × 18	4K × 1 2K × 2 1K × 4 512 × 8 512 × 9 256 × 16 256 × 18 128 × 32 128 × 36	64K × 8 64K × 9 32K × 16 32K × 18 16K × 32 16K × 36 8K × 64 8K × 72 4K × 128 4K × 144

TriMatrix memory provides three different memory sizes for efficient application support. The Quartus II software automatically partitions the user-defined memory into the embedded memory blocks using the most efficient size combinations. You can also manually assign the memory to a specific block size or a mixture of block sizes.

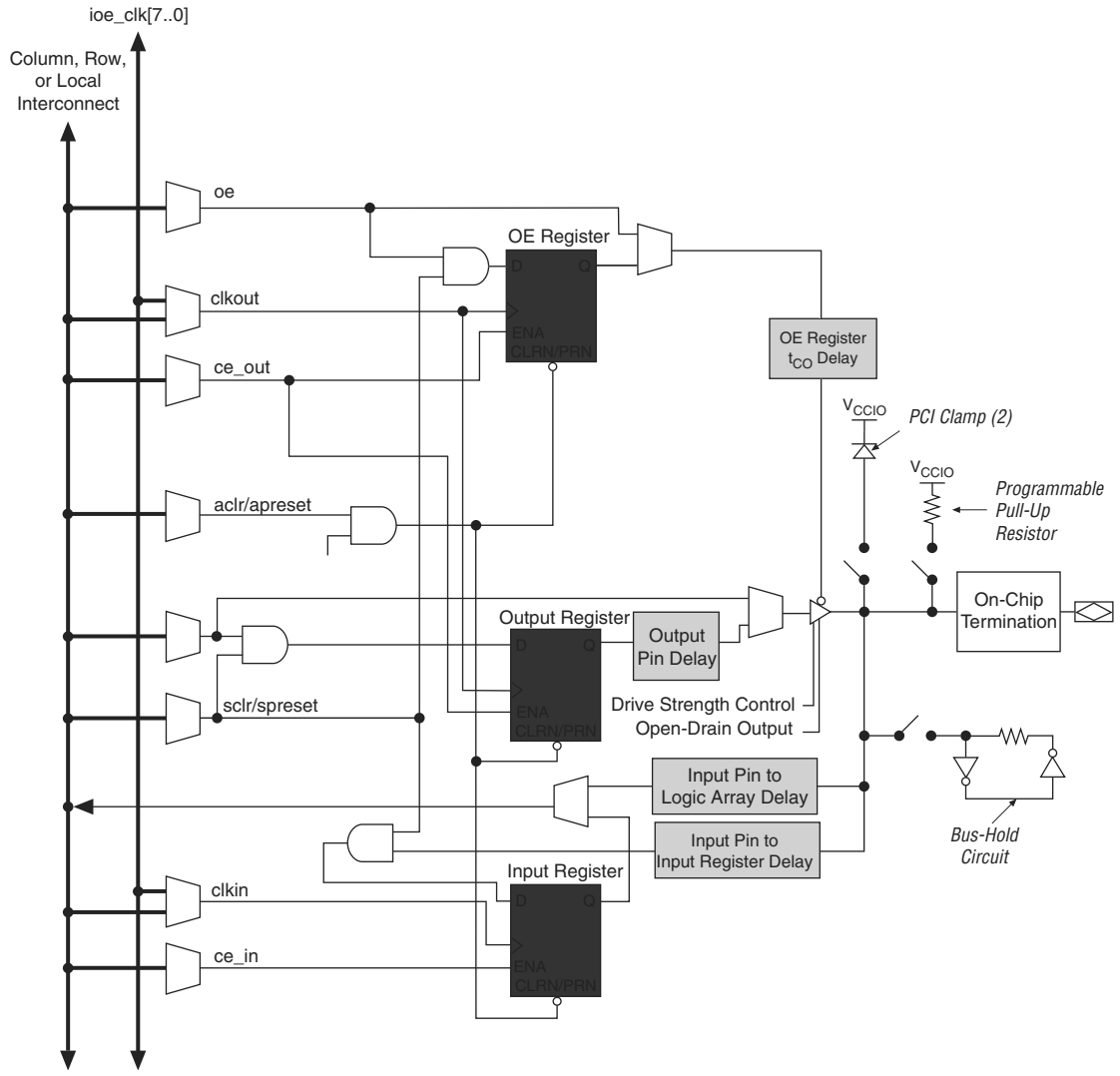
M512 RAM Block

The M512 RAM block is a simple dual-port memory block and is useful for implementing small FIFO buffers, DSP, and clock domain transfer applications. Each block contains 576 RAM bits (including parity bits). M512 RAM blocks can be configured in the following modes:

- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

In normal bidirectional operation, you can use the input register for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. The output register can be used for data requiring fast clock-to-output performance. You can use the OE register for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock enable source from the local interconnect in the associated LAB, dedicated I/O clocks, and the column and row interconnects. Figure 2–72 shows the IOE in bidirectional configuration.

Figure 2–72. Arria GX IOE in Bidirectional I/O Configuration *(Note 1)*



Notes to Figure 2–72:

(1) All input signals to the IOE can be inverted at the IOE.

(2) The optional PCI clamp is only available on column I/O pins.

The Arria GX device IOE includes programmable delays that can be activated to ensure input IOE register-to-logic array register transfers, input pin-to-logic array register transfers, or output IOE register-to-pin transfers.

Table 2–32. EP1AGX50 Device Differential Channels *(Note 1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs		Corner Fast PLLs	
			PLL1	PLL2	PLL7	PLL8
484-pin FineLine BGA	Transmitter	29	16	13	—	—
			13	16	—	—
	Receiver	31	17	14	—	—
			14	17	—	—
780-pin FineLine BGA	Transmitter	29	16	13	—	—
			13	16	—	—
	Receiver	31	17	14	—	—
			14	17	—	—
1,152-pin FineLine BGA	Transmitter	42	21	21	21	21
			21	21	—	—
	Receiver	42	21	21	21	21
			21	21	—	—

Note to Table 2–32:

(1) The total number of receiver channels includes the four non-dedicated clock channels that can be optionally used as data channels.

Table 2–33. EP1AGX60 Device Differential Channels *(Note 1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs		Corner Fast PLLs	
			PLL1	PLL2	PLL7	PLL8
484-pin FineLine BGA	Transmitter	29	16	13	—	—
			13	16	—	—
	Receiver	31	17	14	—	—
			14	17	—	—
780-pin FineLine BGA	Transmitter	29	16	13	—	—
			13	16	—	—
	Receiver	31	17	14	—	—
			14	17	—	—
1,152-pin FineLine BGA	Transmitter	42	21	21	21	21
			21	21	—	—
	Receiver	42	21	21	21	21
			21	21	—	—

Note to Table 2–33:

(1) The total number of receiver channels includes the four non-dedicated clock channels that can be optionally used as data channels.

Configuring Arria GX FPGAs with JRunner

The JRunner software driver configures Altera FPGAs, including Arria GX FPGAs, through the ByteBlaster™ II or ByteBlasterMV cables in JTAG mode. The programming input file supported is in Raw Binary File (**.rbf**) format. JRunner also requires a Chain Description File (**.cdf**) generated by the Quartus II software. JRunner is targeted for embedded JTAG configuration. The source code is developed for the Windows NT operating system (OS), but can be customized to run on other platforms.

For more information about the JRunner software driver, refer to the *AN414: JRunner Software Driver: An Embedded Solution for PLD JTAG Configuration* and the source files on the Altera website.

Programming Serial Configuration Devices with SRunner

You can program a serial configuration device in-system by an external microprocessor using SRunner™. SRunner is a software driver developed for embedded serial configuration device programming that can be easily customized to fit into different embedded systems. SRunner software driver reads a raw programming data file (**.rpd**) and writes to serial configuration devices. The serial configuration device programming time using SRunner software driver is comparable to the programming time when using the Quartus II software.

For more information about SRunner, refer to the *AN418: SRunner: An Embedded Solution for Serial Configuration Device Programming* and the source code on the Altera website.

For more information about programming serial configuration devices, refer to the *Serial Configuration Devices (EPCS1, EPCS4, EPCS64, and EPCS128) Data Sheet* in the *Configuration Handbook*.

Configuring Arria GX FPGAs with the MicroBlaster Driver

The MicroBlaster™ software driver supports a raw binary file (RBF) programming input file and is ideal for embedded FPP or PS configuration. The source code is developed for the Windows NT operating system, although it can be customized to run on other operating systems.

For more information about the MicroBlaster software driver, refer to the *Configuring the MicroBlaster Fast Passive Parallel Software Driver White Paper* or the *AN423: Configuring the MicroBlaster Passive Serial Software Driver*.

PLL Reconfiguration

The phase-locked loops (PLLs) in the Arria GX device family support reconfiguration of their multiply, divide, VCO-phase selection, and bandwidth selection settings without reconfiguring the entire device. You can use either serial data from the logic array or regular I/O pins to program the PLL's counter settings in a serial chain. This option provides considerable flexibility for frequency synthesis, allowing real-time variation of the PLL frequency and delay. The rest of the device is functional while reconfiguring the PLL.

Table 4–8 and Table 4–9 list the transmitter and receiver PCS latency for each mode, respectively.

Table 4–8. PCS Latency *(Note 1)*

Functional Mode	Configuration	Transmitter PCS Latency					
		TX PIPE	TX Phase Comp FIFO	Byte Serializer	TX State Machine	8B/10B Encoder	Sum *(2)*
XAUI	—	—	2–3	1	0.5	0.5	4–5
PIPE	×1, ×4, ×8 8-bit channel width	1	3–4	1	—	1	6–7
	×1, ×4, ×8 16-bit channel width	1	3–4	1	—	0.5	6–7
GIGE	—	—	2–3	1	—	1	4–5
Serial RapidIO	1.25 Gbps, 2.5 Gbps, 3.125 Gbps	—	2–3	1	—	0.5	4–5
SDI	HD10-bit channel width	—	2–3	1	—	1	4–5
	HD, 3G 20-bit channel width	—	2–3	1	—	0.5	4–5
BASIC Single Width	8-bit/10-bit channel width	—	2–3	1	—	1	4–5
	16-bit/20-bit channel width	—	2–3	1	—	0.5	4–5

Notes to Table 4–8:

(1) The latency numbers are with respect to the PLD-transceiver interface clock cycles.

(2) The total latency number is rounded off in the Sum column.

Table 4–9. PCS Latency (Part 1 of 2) (Part 1 of 2)

Functional Mode	Configuration	Receiver PCS Latency									
		Word Aligner	Deskew FIFO	Rate Matcher *(3)*	8B/10B Decoder	Receiver State Machine	Byte Deserializer	Byte Order	Receiver Phase Comp FIFO	Receiver PIPE	Sum *(2)*
XAUI	—	2–2.5	2–2.5	5.5–6.5	0.5	1	1	1	1–2	—	14–17
PIPE	×1, ×4 8-bit channel width	4–5	—	11–13	1	—	1	1	2–3	1	21–25
	×1, ×4 16-bit channel width	2–2.5	—	5.5–6.5	0.5	—	1	1	2–3	1	13–16
GIGE	—	4–5	—	11–13	1	—	1	1	1–2	—	19–23
Serial RapidIO	1.25 Gbps, 2.5 Gbps, 3.125 Gbps	2–2.5	—	—	0.5	—	1	1	1–2	—	6–7
SDI	HD 10-bit channel width	5	—	—	1	—	1	1	1–2	—	9–10
	HD, 3G 20-bit channel width	2.5	—	—	0.5	—	1	1	1–2	—	6–7

Table 4–54. EP1AGX35 Row Pins Input Timing Parameters (Part 2 of 2)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
SSTL-18 CLASS II	GCLK	t_{SU}	1.417	1.417	3.118	ns
		t_H	–1.312	–1.312	–2.841	ns
	GCLK PLL	t_{SU}	2.836	2.836	6.190	ns
		t_H	–2.731	–2.731	–5.913	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	1.417	1.417	3.118	ns
		t_H	–1.312	–1.312	–2.841	ns
	GCLK PLL	t_{SU}	2.836	2.836	6.190	ns
		t_H	–2.731	–2.731	–5.913	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	1.417	1.417	3.118	ns
		t_H	–1.312	–1.312	–2.841	ns
	GCLK PLL	t_{SU}	2.836	2.836	6.190	ns
		t_H	–2.731	–2.731	–5.913	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.443	1.443	3.246	ns
		t_H	–1.338	–1.338	–2.969	ns
	GCLK PLL	t_{SU}	2.862	2.862	6.318	ns
		t_H	–2.757	–2.757	–6.041	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.443	1.443	3.246	ns
		t_H	–1.338	–1.338	–2.969	ns
	GCLK PLL	t_{SU}	2.862	2.862	6.318	ns
		t_H	–2.757	–2.757	–6.041	ns
LVDS	GCLK	t_{SU}	1.341	1.341	3.088	ns
		t_H	–1.236	–1.236	–2.811	ns
	GCLK PLL	t_{SU}	2.769	2.769	6.171	ns
		t_H	–2.664	–2.664	–5.894	ns

Table 4–55 lists I/O timing specifications.

Table 4–55. EP1AGX35 Column Pins Input Timing Parameters (Part 1 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.251	1.251	2.915	ns
		t_H	–1.146	–1.146	–2.638	ns
	GCLK PLL	t_{SU}	2.693	2.693	6.021	ns
		t_H	–2.588	–2.588	–5.744	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.251	1.251	2.915	ns
		t_H	–1.146	–1.146	–2.638	ns
	GCLK PLL	t_{SU}	2.693	2.693	6.021	ns
		t_H	–2.588	–2.588	–5.744	ns

Table 4–56. EP1AGX35 Row Pins Output Timing Parameters (Part 2 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
2.5 V	8 mA	GCLK	t_{CO}	2.656	2.656	5.775	ns
		GCLK PLL	t_{CO}	1.237	1.237	2.703	ns
2.5 V	12 mA	GCLK	t_{CO}	2.637	2.637	5.661	ns
		GCLK PLL	t_{CO}	1.218	1.218	2.589	ns
1.8 V	2 mA	GCLK	t_{CO}	2.829	2.829	7.052	ns
		GCLK PLL	t_{CO}	1.410	1.410	3.980	ns
1.8 V	4 mA	GCLK	t_{CO}	2.818	2.818	6.273	ns
		GCLK PLL	t_{CO}	1.399	1.399	3.201	ns
1.8 V	6 mA	GCLK	t_{CO}	2.707	2.707	5.972	ns
		GCLK PLL	t_{CO}	1.288	1.288	2.900	ns
1.8 V	8 mA	GCLK	t_{CO}	2.676	2.676	5.858	ns
		GCLK PLL	t_{CO}	1.257	1.257	2.786	ns
1.5 V	2 mA	GCLK	t_{CO}	2.789	2.789	6.551	ns
		GCLK PLL	t_{CO}	1.370	1.370	3.479	ns
1.5 V	4 mA	GCLK	t_{CO}	2.682	2.682	5.950	ns
		GCLK PLL	t_{CO}	1.263	1.263	2.878	ns
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.626	2.626	5.614	ns
		GCLK PLL	t_{CO}	1.207	1.207	2.542	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.602	2.602	5.538	ns
		GCLK PLL	t_{CO}	1.183	1.183	2.466	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.568	2.568	5.407	ns
		GCLK PLL	t_{CO}	1.149	1.149	2.335	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.614	2.614	5.556	ns
		GCLK PLL	t_{CO}	1.195	1.195	2.484	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.618	2.618	5.485	ns
		GCLK PLL	t_{CO}	1.199	1.199	2.413	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.594	2.594	5.468	ns
		GCLK PLL	t_{CO}	1.175	1.175	2.396	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.597	2.597	5.447	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.375	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.595	2.595	5.466	ns
		GCLK PLL	t_{CO}	1.176	1.176	2.394	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.598	2.598	5.430	ns
		GCLK PLL	t_{CO}	1.179	1.179	2.358	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.580	2.580	5.426	ns
		GCLK PLL	t_{CO}	1.161	1.161	2.354	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.584	2.584	5.415	ns
		GCLK PLL	t_{CO}	1.165	1.165	2.343	ns

Table 4–59 lists column pin delay adders when using the regional clock in Arria GX devices.

Table 4–59. EP1AGX35 Column Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.099	0.099	0.254	ns
RCLK PLL input adder	–0.012	–0.012	–0.01	ns
RCLK output adder	–0.086	–0.086	–0.244	ns
RCLK PLL output adder	1.253	1.253	3.133	ns

EP1AGX50 I/O Timing Parameters

Table 4–60 through Table 4–63 list the maximum I/O timing parameters for EP1AGX50 devices for I/O standards which support general purpose I/O pins.

Table 4–60 lists I/O timing specifications.

Table 4–60. EP1AGX50 Row Pins Input Timing Parameters (Part 1 of 2)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.550	1.550	3.542	ns
		t_H	–1.445	–1.445	–3.265	ns
	GCLK PLL	t_{SU}	2.978	2.978	6.626	ns
		t_H	–2.873	–2.873	–6.349	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.550	1.550	3.542	ns
		t_H	–1.445	–1.445	–3.265	ns
	GCLK PLL	t_{SU}	2.978	2.978	6.626	ns
		t_H	–2.873	–2.873	–6.349	ns
2.5 V	GCLK	t_{SU}	1.562	1.562	3.523	ns
		t_H	–1.457	–1.457	–3.246	ns
	GCLK PLL	t_{SU}	2.990	2.990	6.607	ns
		t_H	–2.885	–2.885	–6.330	ns
1.8 V	GCLK	t_{SU}	1.628	1.628	3.730	ns
		t_H	–1.523	–1.523	–3.453	ns
	GCLK PLL	t_{SU}	3.056	3.056	6.814	ns
		t_H	–2.951	–2.951	–6.537	ns
1.5 V	GCLK	t_{SU}	1.631	1.631	3.825	ns
		t_H	–1.526	–1.526	–3.548	ns
	GCLK PLL	t_{SU}	3.059	3.059	6.909	ns
		t_H	–2.954	–2.954	–6.632	ns

Table 4–62. EP1AGX50 Row Pins Output Timing Parameters (Part 2 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.731	2.731	6.036	ns
		GCLK PLL	t_{CO}	1.303	1.303	2.952	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.787	2.787	6.073	ns
		GCLK PLL	t_{CO}	1.359	1.359	2.989	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.681	2.681	5.767	ns
		GCLK PLL	t_{CO}	1.253	1.253	2.683	ns
2.5 V	4 mA	GCLK	t_{CO}	2.770	2.770	6.047	ns
		GCLK PLL	t_{CO}	1.342	1.342	2.963	ns
2.5 V	8 mA	GCLK	t_{CO}	2.667	2.667	5.789	ns
		GCLK PLL	t_{CO}	1.239	1.239	2.705	ns
2.5 V	12 mA	GCLK	t_{CO}	2.648	2.648	5.675	ns
		GCLK PLL	t_{CO}	1.220	1.220	2.591	ns
1.8 V	2 mA	GCLK	t_{CO}	2.840	2.840	7.066	ns
		GCLK PLL	t_{CO}	1.412	1.412	3.982	ns
1.8 V	4 mA	GCLK	t_{CO}	2.829	2.829	6.287	ns
		GCLK PLL	t_{CO}	1.401	1.401	3.203	ns
1.8 V	6 mA	GCLK	t_{CO}	2.718	2.718	5.986	ns
		GCLK PLL	t_{CO}	1.290	1.290	2.902	ns
1.8 V	8 mA	GCLK	t_{CO}	2.687	2.687	5.872	ns
		GCLK PLL	t_{CO}	1.259	1.259	2.788	ns
1.5 V	2 mA	GCLK	t_{CO}	2.800	2.800	6.565	ns
		GCLK PLL	t_{CO}	1.372	1.372	3.481	ns
1.5 V	4 mA	GCLK	t_{CO}	2.693	2.693	5.964	ns
		GCLK PLL	t_{CO}	1.265	1.265	2.880	ns
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.636	2.636	5.626	ns
		GCLK PLL	t_{CO}	1.209	1.209	2.544	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.612	2.612	5.550	ns
		GCLK PLL	t_{CO}	1.185	1.185	2.468	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.578	2.578	5.419	ns
		GCLK PLL	t_{CO}	1.151	1.151	2.337	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.625	2.625	5.570	ns
		GCLK PLL	t_{CO}	1.197	1.197	2.486	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.628	2.628	5.497	ns
		GCLK PLL	t_{CO}	1.201	1.201	2.415	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.604	2.604	5.480	ns
		GCLK PLL	t_{CO}	1.177	1.177	2.398	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.607	2.607	5.459	ns
		GCLK PLL	t_{CO}	1.180	1.180	2.377	ns

Table 4–63. EP1AGX50 Column Pins Output Timing Parameters (Part 4 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
1.8-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.602	2.602	5.574	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.314	ns
1.8-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.604	2.604	5.578	ns
		GCLK PLL	t_{CO}	1.166	1.166	2.325	ns
1.8-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.604	2.604	5.577	ns
		GCLK PLL	t_{CO}	1.166	1.166	2.334	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.637	2.637	5.675	ns
		GCLK PLL	t_{CO}	1.196	1.196	2.569	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.644	2.644	5.651	ns
		GCLK PLL	t_{CO}	1.206	1.206	2.554	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.626	2.626	5.653	ns
		GCLK PLL	t_{CO}	1.188	1.188	2.556	ns
1.5-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.626	2.626	5.655	ns
		GCLK PLL	t_{CO}	1.188	1.188	2.558	ns
1.5-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.620	2.620	5.653	ns
		GCLK PLL	t_{CO}	1.182	1.182	2.556	ns
1.5-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.607	2.607	5.573	ns
		GCLK PLL	t_{CO}	1.169	1.169	2.368	ns
1.5-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.610	2.610	5.571	ns
		GCLK PLL	t_{CO}	1.172	1.172	2.378	ns
1.5-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.612	2.612	5.581	ns
		GCLK PLL	t_{CO}	1.174	1.174	2.391	ns
3.3-V PCI	—	GCLK	t_{CO}	2.786	2.786	5.803	ns
		GCLK PLL	t_{CO}	1.322	1.322	2.697	ns
3.3-V PCI-X	—	GCLK	t_{CO}	2.786	2.786	5.803	ns
		GCLK PLL	t_{CO}	1.322	1.322	2.697	ns
LVDS	—	GCLK	t_{CO}	3.621	3.621	6.969	ns
		GCLK PLL	t_{CO}	2.190	2.190	3.880	ns

Table 4–64 through Table 4–65 list EP1AGX50 regional clock (RCLK) adder values that should be added to the GCLK values. These adder values are used to determine I/O timing when the I/O pin is driven using the regional clock. This applies for all I/O standards supported by Arria GX with general purpose I/O pins.

Table 4–64 lists row pin delay adders when using the regional clock in Arria GX devices.

Table 4–64. EP1AGX50 Row Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.151	0.151	0.329	ns
RCLK PLL input adder	0.011	0.011	0.016	ns
RCLK output adder	–0.151	–0.151	–0.329	ns
RCLK PLL output adder	–0.011	–0.011	–0.016	ns

Table 4–65 lists column pin delay adders when using the regional clock in Arria GX devices.

Table 4–65. EP1AGX50 Column Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.146	0.146	0.334	ns
RCLK PLL input adder	–1.713	–1.713	–3.645	ns
RCLK output adder	–0.146	–0.146	–0.336	ns
RCLK PLL output adder	1.716	1.716	4.488	ns

EP1AGX60 I/O Timing Parameters

Table 4–66 through Table 4–69 list the maximum I/O timing parameters for EP1AGX60 devices for I/O standards which support general purpose I/O pins.

Table 4–66 lists I/O timing specifications.

Table 4–66. EP1AGX60 Row Pins Input Timing Parameters (Part 1 of 3)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.413	1.413	3.113	ns
		t_H	–1.308	–1.308	–2.836	ns
	GCLK PLL	t_{SU}	2.975	2.975	6.536	ns
		t_H	–2.870	–2.870	–6.259	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.413	1.413	3.113	ns
		t_H	–1.308	–1.308	–2.836	ns
	GCLK PLL	t_{SU}	2.975	2.975	6.536	ns
		t_H	–2.870	–2.870	–6.259	ns
2.5 V	GCLK	t_{SU}	1.425	1.425	3.094	ns
		t_H	–1.320	–1.320	–2.817	ns
	GCLK PLL	t_{SU}	2.987	2.987	6.517	ns
		t_H	–2.882	–2.882	–6.240	ns

Table 4–90 lists clock timing specifications.

Table 4–90. EP1AGX50 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.653	1.653	3.841	ns
t_{COUT}	1.651	1.651	3.839	ns
t_{PLLCIN}	0.245	0.245	0.755	ns
$t_{PLLCOUT}$	0.245	0.245	0.755	ns

EP1AGX60 Clock Timing Parameters

Table 4–91 to Table 4–92 on page 4–82 list the GCLK clock timing parameters for EP1AGX60 devices.

Table 4–91 lists clock timing specifications.

Table 4–91. EP1AGX60 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.531	1.531	3.593	ns
t_{COUT}	1.536	1.536	3.587	ns
t_{PLLCIN}	–0.023	–0.023	0.188	ns
$t_{PLLCOUT}$	–0.018	–0.018	0.182	ns

Table 4–92 lists clock timing specifications.

Table 4–92. EP1AGX60 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.792	1.792	4.165	ns
t_{COUT}	1.792	1.792	4.165	ns
t_{PLLCIN}	0.238	0.238	0.758	ns
$t_{PLLCOUT}$	0.238	0.238	0.758	ns

Table 4–99 lists performance notes.

Table 4–99. Arria GX Performance Notes

Applications		Resources Used			Performance
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	–6 Speed Grade
LE	16-to-1 multiplexer	5	0	0	168.41
	32-to-1 multiplexer	11	0	0	334.11
	16-bit counter	16	0	0	374.0
	64-bit counter	64	0	0	168.41
TriMatrix Memory M512 block	Simple dual-port RAM 32 x 18 bit	0	1	0	348.0
	FIFO 32 x 18 bit	0	1	0	333.22
TriMatrix Memory M4K block	Simple dual-port RAM 128 x 36 bit	0	1	0	344.71
	True dual-port RAM 128 x 18 bit	0	1	0	348.0
TriMatrix Memory MegaRAM block	Single port RAM 4K x 144 bit	0	2	0	244.0
	Simple dual-port RAM 4K x 144 bit	0	1	0	292.0
	True dual-port RAM 4K x 144 bit	0	2	0	244.0
	Single port RAM 8K x 72 bit	0	1	0	247.0
	Simple dual-port RAM 8K x 72 bit	0	1	0	292.0
	Single port RAM 16K x 36 bit	0	1	0	254.0
	Simple dual-port RAM 16K x 36 bit	0	1	0	292.0
	True dual-port RAM 16K x 36 bit	0	1	0	251.0
	Single port RAM 32K x 18 bit	0	1	0	317.36
	Simple dual-port RAM 32K x 18 bit	0	1	0	292.0
	True dual-port RAM 32K x 18 bit	0	1	0	251.0
	Single port RAM 64K x 9 bit	0	1	0	254.0
	Simple dual-port RAM 64K x 9 bit	0	1	0	292.0
	True dual-port RAM 64K x 9 bit	0	1	0	251.0

Table 4–101 lists IOE programmable delays.

Table 4–101. Arria GX IOE Programmable Delay on Column Pins

Parameter	Paths Affected	Available Settings	Fast Model				–6 Speed Grade		Units
			Industrial		Commercial				
			Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	
Input delay from pin to internal cells	Pad to I/O dataout to core	8	0	1.781	0	1.781	0	4.132	ns
Input delay from pin to input register	Pad to I/O input register	64	0	2.053	0	2.053	0	4.697	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.332	0	0.332	0	0.717	ns
Output enable pin delay	txz/tzx	2	0	0.32	0	0.32	0	0.693	ns

Maximum Input and Output Clock Toggle Rate

Maximum clock toggle rate is defined as the maximum frequency achievable for a clock type signal at an I/O pin. The I/O pin can be a regular I/O pin or a dedicated clock I/O pin.

The maximum clock toggle rate is different from the maximum data bit rate. If the maximum clock toggle rate on a regular I/O pin is 300 MHz, the maximum data bit rate for dual data rate (DDR) could be potentially as high as 600 Mbps on the same I/O pin.

Table 4–105, Table 4–106, and Table 4–107 provide output toggle rates at the default capacitive loading. Use the Quartus II software to obtain output toggle rates at loads different from the default capacitive loading.

Table 4–102 shows the maximum input clock toggle rates for Arria GX device column I/O pins.

Table 4–102. Arria GX Maximum Input Toggle Rate for Column I/O Pins

I/O Standards	–6 Speed Grade	Units
3.3-V LVTTL	420	MHz
3.3-V LVCMOS	420	MHz
2.5 V	420	MHz
1.8 V	420	MHz
1.5 V	420	MHz
SSTL-2 CLASS I	467	MHz
SSTL-2 CLASS II	467	MHz
SSTL-18 CLASS I	467	MHz

Table 4–105. Arria GX Maximum Output Toggle Rate for Column I/O Pins (Part 2 of 3)

I/O Standards	Drive Strength	–6 Speed Grade	Units
3.3-V LVCMOS	4 mA	215	MHz
	8 mA	411	MHz
	12 mA	626	MHz
	16 mA	819	MHz
	20 mA	874	MHz
	24 mA	934	MHz
2.5 V	4 mA	168	MHz
	8 mA	355	MHz
	12 mA	514	MHz
	16 mA	766	MHz
1.8 V	2 mA	97	MHz
	4 mA	215	MHz
	6 mA	336	MHz
	8 mA	486	MHz
	10 mA	706	MHz
	12 mA	925	MHz
1.5 V	2 mA	168	MHz
	4 mA	303	MHz
	6 mA	350	MHz
	8 mA	392	MHz
SSTL-2 CLASS I	8 mA	280	MHz
	12 mA	327	MHz
SSTL-2 CLASS II	16 mA	280	MHz
	20 mA	327	MHz
	24 mA	327	MHz
SSTL-18 CLASS I	4 mA	140	MHz
	6 mA	186	MHz
	8 mA	280	MHz
	10 mA	373	MHz
	12 mA	373	MHz
SSTL-18 CLASS II	8 mA	140	MHz
	16 mA	327	MHz
	18 mA	373	MHz
	20 mA	420	MHz
1.8-V HSTL CLASS I	4 mA	280	MHz
	6 mA	420	MHz
	8 mA	561	MHz
	10 mA	561	MHz
	12 mA	607	MHz

Table 4–116. Enhanced PLL Specifications (Part 2 of 2)

Name	Description	Min	Typ	Max	Units
$t_{RECONFIGWAIT}$	The time required for the wait after the reconfiguration is done and the areset is applied.	—	—	2	us

Notes to Table 4–116:

(1) This is limited by the I/O f_{MAX}.

(2) If the counter cascading feature of the PLL is used, there is no minimum output clock frequency.

Table 4–117. Fast PLL Specifications (Part 1 of 2)

Name	Description	Min	Typ	Max	Units
f_{IN}	Input clock frequency	16.08	—	640	MHz
f_{INPFD}	Input frequency to the PFD	16.08	—	500	MHz
f_{INDUTY}	Input clock duty cycle	40	—	60	%
$t_{INJITTER}$	Input clock jitter tolerance in terms of period jitter. Bandwidth ≤ 2 MHz	—	0.5	—	ns (p-p)
	Input clock jitter tolerance in terms of period jitter. Bandwidth > 0.2 MHz	—	1.0	—	ns (p-p)
f_{VCO}	Upper VCO frequency range	300	—	840	MHz
	Lower VCO frequency range	150	—	420	MHz
f_{OUT}	PLL output frequency to GCLK or RCLK	4.6875	—	550	MHz
	PLL output frequency to LVDS or DPA clock	150	—	840	MHz
f_{OUT_EXT}	PLL clock output frequency to regular I/O	4.6875	—	*(1)*	MHz
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for fast PLLs	—	$75/f_{SCANCLK}$	—	ns
f_{CLBW}	PLL closed-loop bandwidth	1.16	5	28	MHz
t_{LOCK}	Time required for the PLL to lock from the time it is enabled or the end of the device configuration	—	0.03	1	ms
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±30	ps
t_{ARESET}	Minimum pulse width on areset signal.	10	—	—	ns