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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1676
Number of Logic Elements/Cells	33520
Total RAM Bits	1348416
Number of I/O	341
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep1agx35df780i6n

Once a pattern is detected and the data bus is aligned, the word boundary is locked. The two detection status signals (`rx_syncstatus` and `rx_patterndetect`) indicate that an alignment is complete.

Figure 2–15 is a block diagram of the word aligner.

Figure 2–15. Word Aligner

Control and Status Signals

The `rx_enapatternalign` signal is the FPGA control signal that enables word alignment in non-automatic modes. The `rx_enapatternalign` signal is not used in automatic modes (PCI Express [PIPE], XAUI, GIGE, and Serial RapidIO).

In manual alignment mode, after the `rx_enapatternalign` signal is activated, the `rx_syncstatus` signal goes high for one parallel clock cycle to indicate that the alignment pattern has been detected and the word boundary has been locked. If `rx_enapatternalign` is deactivated, the `rx_syncstatus` signal acts as a re-synchronization signal to signify that the alignment pattern has been detected but not locked on a different word boundary.

When using the synchronization state machine, the `rx_syncstatus` signal indicates the link status. If the `rx_syncstatus` signal is high, link synchronization is achieved. If the `rx_syncstatus` signal is low, link synchronization has not yet been achieved, or there were enough code group errors to lose synchronization.

For more information about manual alignment modes, refer to the *Arria GX Device Handbook*.

The `rx_patterndetect` signal pulses high during a new alignment and whenever the alignment pattern occurs on the current word boundary.

Programmable Run Length Violation

The word aligner supports a programmable run length violation counter. Whenever the number of the continuous '0' (or '1') exceeds a user programmable value, the `rx_rlv` signal goes high for a minimum pulse width of two recovered clock cycles. The maximum run values supported are 128 UI for 8-bit serialization or 160 UI for 10-bit serialization.

Running Disparity Check

The running disparity error `rx_disperr` and running disparity value `rx_runningdisp` are sent along with aligned data from the 8B/10B decoder to the FPGA. You can ignore or act on the reported running disparity value and running disparity error signals.

For more information about transceiver clocking in all supported functional modes, refer to the *Arria GX Transceiver Architecture* chapter.

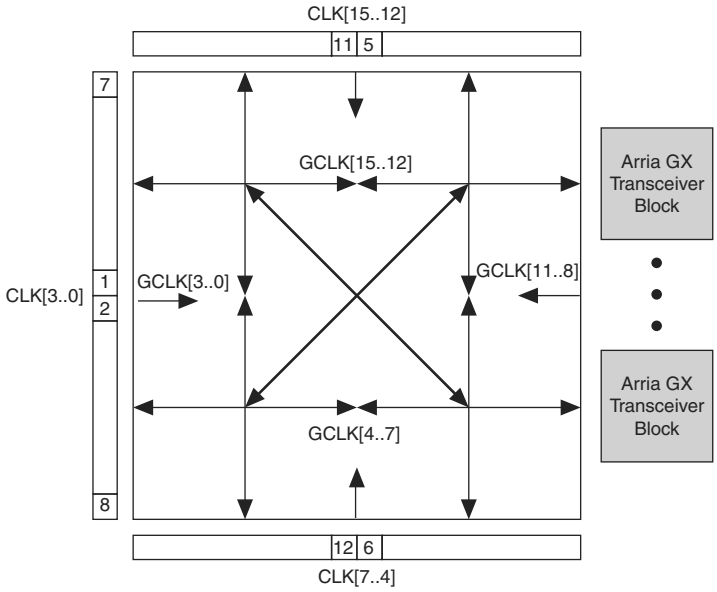
PLD Clock Utilization by Transceiver Blocks

Arria GX devices have up to 16 global clock (GCLK) lines and 16 regional clock (RCLK) lines that are used to route the transceiver clocks. The following transceiver clocks use the available global and regional clock resources:

- `pll_inclk` (if driven from an FPGA input pin)
- `rx_cruclk` (if driven from an FPGA input pin)
- `tx_clkout/coreclkout` (CMU low-speed parallel clock forwarded to the PLD)
- Recovered clock from each channel (`rx_clkout`) in non-rate matcher mode
- Calibration clock (`cal_blk_clk`)
- Fixed clock (`fixedclk` used for receiver detect circuitry in PCI Express [PIPE] mode only)

Figure 2–23 and Figure 2–24 show the available GCLK and RCLK resources in Arria GX devices.

Figure 2–23. Global Clock Resources in Arria GX Devices



Logic Array Blocks

Each logic array block (LAB) consists of eight adaptive logic modules (ALMs), carry chains, shared arithmetic chains, LAB control signals, local interconnects, and register chain connection lines. The local interconnect transfers signals between ALMs in the same LAB. Register chain connections transfer the output of an ALM register to the adjacent ALM register in a LAB. The Quartus II Compiler places associated logic in a LAB or adjacent LABs, allowing the use of local, shared arithmetic chain, and register chain connections for performance and area efficiency. Table 2–9 lists Arria GX device resources. Figure 2–25 shows the Arria GX LAB structure.

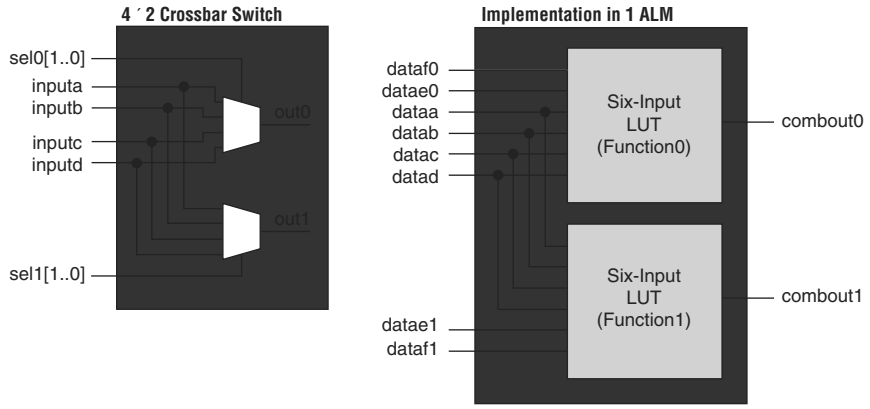
Table 2–9. Arria GX Device Resources

Device	M512 RAM Columns/Blocks	M4K RAM Columns/Blocks	M-RAM Blocks	DSP Block Columns/Blocks
EP1AGX20	166	118	1	10
EP1AGX35	197	140	1	14
EP1AGX50	313	242	2	26
EP1AGX60	326	252	2	32
EP1AGX90	478	400	4	44

To pack two five-input functions into one ALM, the functions must have at least two common inputs. The common inputs are dataa and datab. The combination of a four-input function with a five-input function requires one common input (either dataa or datab).

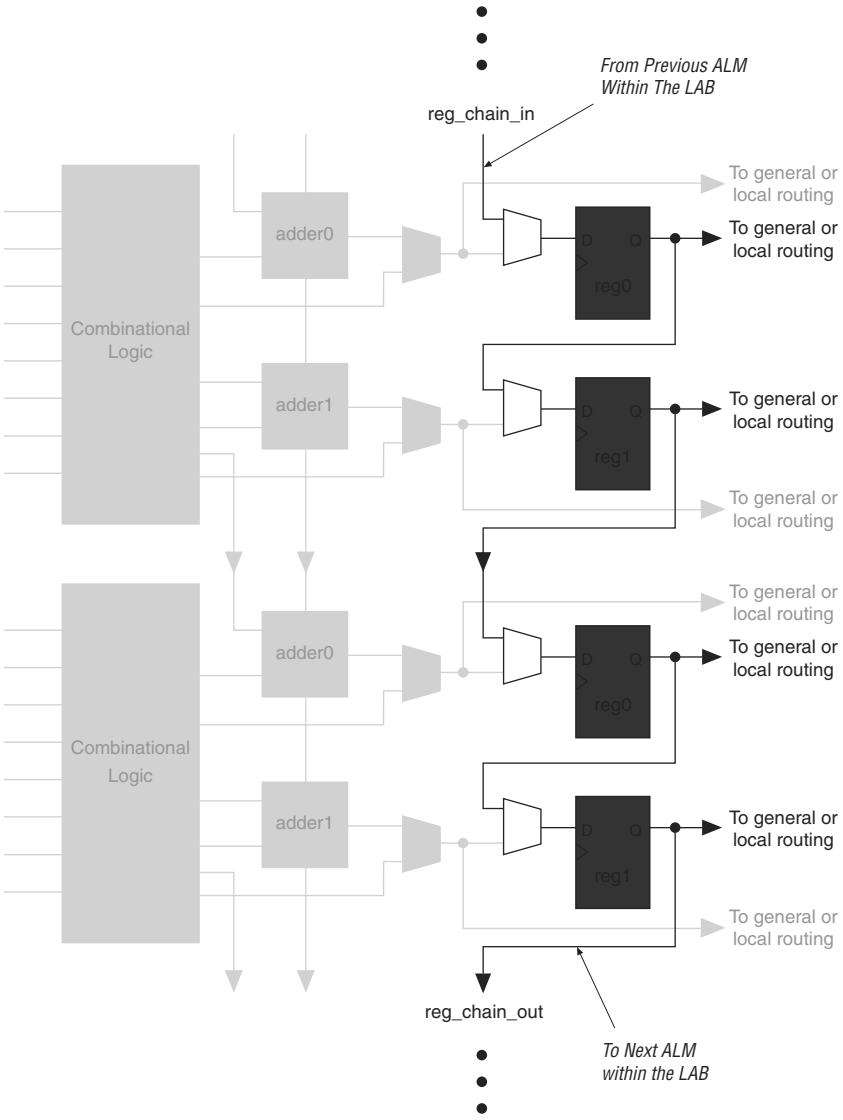
To implement two six-input functions in one ALM, four inputs must be shared and the combinational function must be the same. For example, a 4 × 2 crossbar switch (two 4-to-1 multiplexers with common inputs and unique select lines) can be implemented in one ALM, as shown in Figure 2–31. The shared inputs are dataa, datab, datac, and datad, while the unique select lines are datae0 and dataf0 for function0, and datae1 and dataf1 for function1. This crossbar switch consumes four LUTs in a four-input LUT-based architecture.

Figure 2–31. 4 × 2 Crossbar Switch Example



In a sparsely used device, functions that can be placed into one ALM can be implemented in separate ALMs. The Quartus II Compiler spreads a design out to achieve the best possible performance. As a device begins to fill up, the Quartus II software automatically uses the full potential of the Arria GX ALM. The Quartus II Compiler automatically searches for functions of common inputs or completely independent functions to be placed into one ALM and to make efficient use of the device resources. In addition, you can manually control resource usage by setting location assignments. Any six-input function can be implemented utilizing inputs dataa, datab, datac, datad, and either datae0 and dataf0 or datae1 and dataf1. If datae0 and dataf0 are used, the output is driven to register0, and/or register0 is bypassed and the data drives out to the interconnect using the top set of output drivers (refer to Figure 2–32). If datae1 and dataf1 are used, the output drives to register1 and/or bypasses register1 and drives to the interconnect using the bottom set of output drivers. The Quartus II Compiler automatically selects the inputs to the LUT. Asynchronous load data for the register comes from the datae or dataf input of the ALM. ALMs in normal mode support register packing.

Figure 2–38. Register Chain within a LAB *(Note 1)*



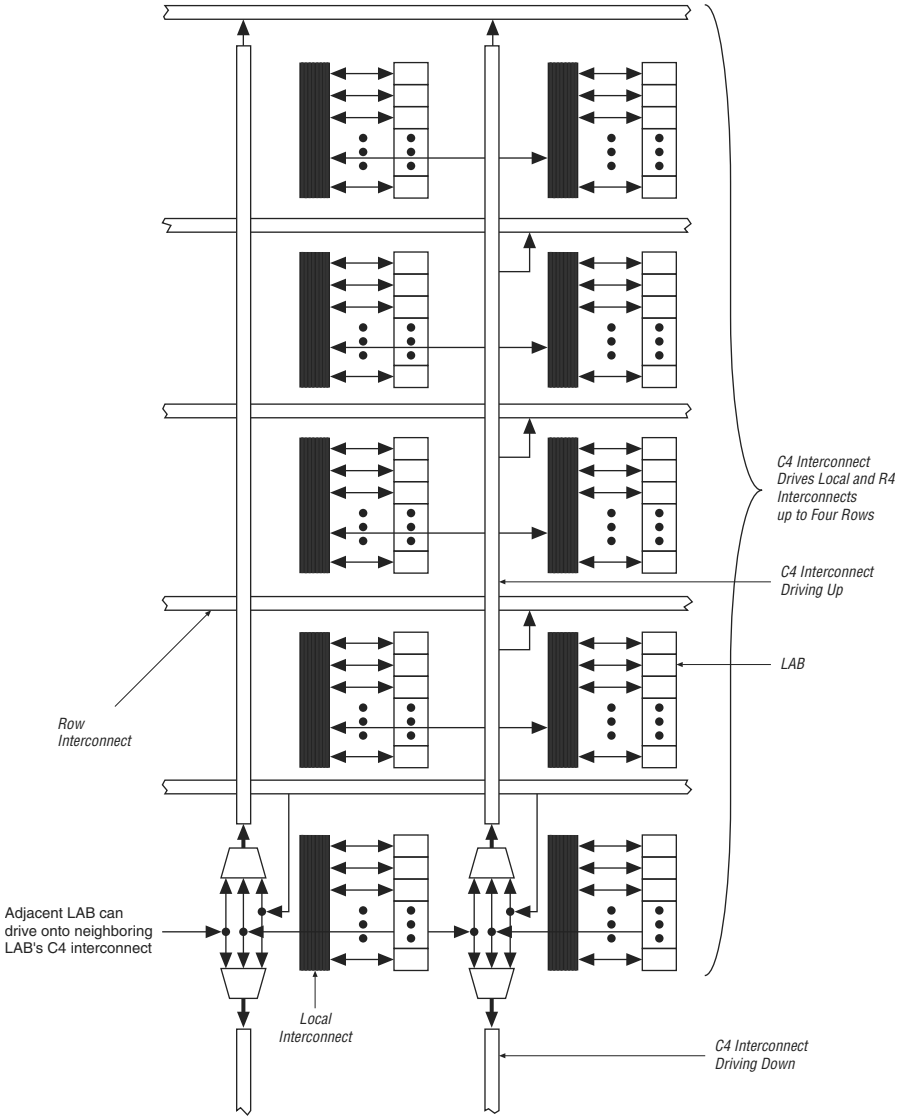
Note to Figure 2–38:

(1) The combinational or adder logic can be used to implement an unrelated, unregistered function.

Clear and Preset Logic Control

LAB-wide signals control the logic for the register's clear and load/preset signals. The ALM directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. The direct asynchronous preset does not require a NOT gate push-back technique. Arria GX devices support simultaneous asynchronous load/preset and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one load/preset signal.

Figure 2–41. C4 Interconnect Connections *(Note 1)*

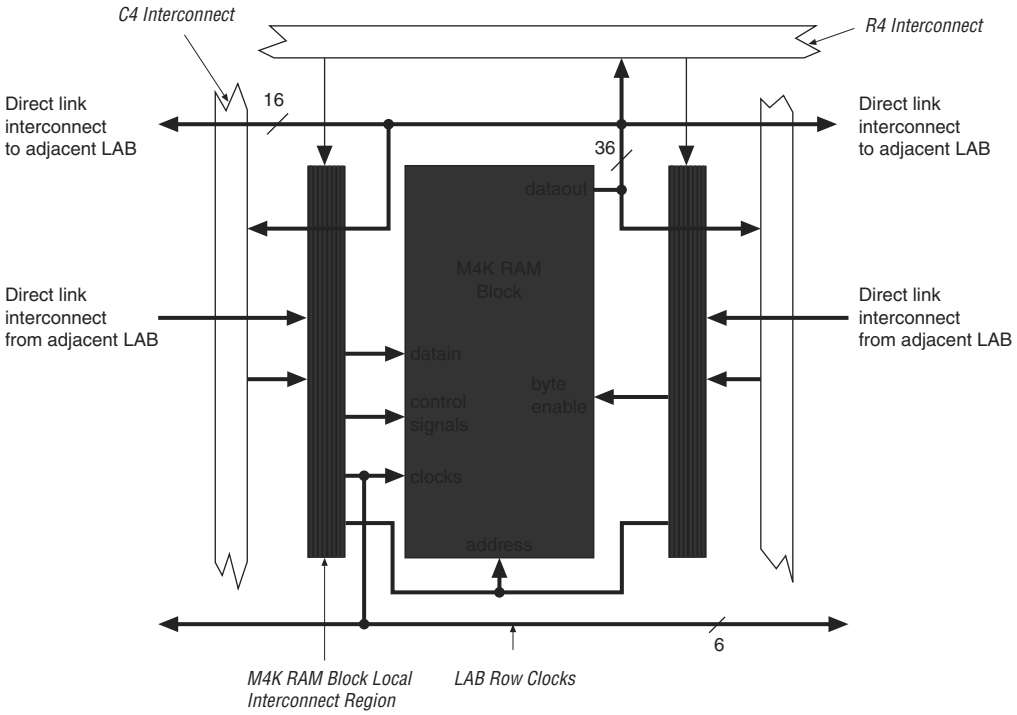


Note to Figure 2–41:

(1) Each C4 interconnect can drive either up or down four rows.

C16 column interconnects span a length of 16 LABs and provide the fastest resource for long column connections between LABs, TriMatrix memory blocks, DSP blocks, and IOEs. C16 interconnects can cross M-RAM blocks and also drive to row and column interconnects at every fourth LAB. C16 interconnects drive LAB local interconnects via C4 and R4 interconnects and do not drive LAB local interconnects directly. All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (that is, TriMatrix memory and DSP blocks) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB. All blocks are fed by the row LAB clocks, `labclk[5..0]`.

Figure 2–45. M4K RAM Block LAB Row Interface



M-RAM Block

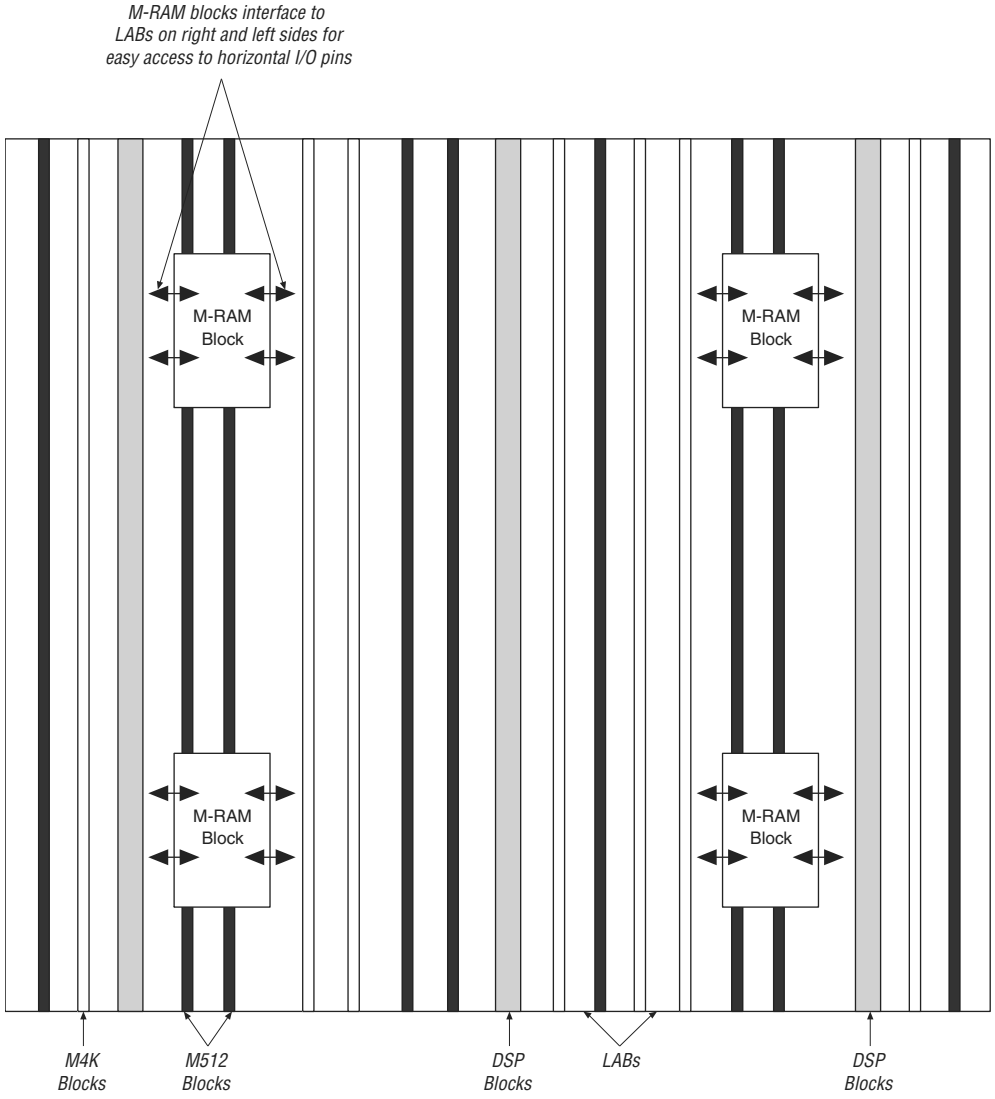
The largest TriMatrix memory block, the M-RAM block, is useful for applications where a large volume of data must be stored on-chip. Each block contains 589,824 RAM bits (including parity bits). The M-RAM block can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO

You cannot use an initialization file to initialize the contents of a M-RAM block. All M-RAM block contents power up to an undefined value. Only synchronous operation is supported in the M-RAM block, so all inputs are registered. Output registers can be bypassed.

Similar to all RAM blocks, M-RAM blocks can have different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M-RAM block registers (`renwe`, `address`, byte enable, `datain`, and output registers). You can bypass the output register. The six `labclk` signals or local interconnect can drive the control signals for the A and B ports of the M-RAM block. ALMs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, `clr_b`, `clocken_a`, and `clocken_b` signals, as shown in Figure 2–46.

Figure 2–47. EP1AGX90 Device with M-RAM Interface Locations *(Note 1)*



Note to Figure 2–47:

(1) The device shown is an EP1AGX90 device. The number and position of M-RAM blocks vary in other devices.

Figure 2–51. DSP Block Diagram for 18 × 18-Bit Configuration

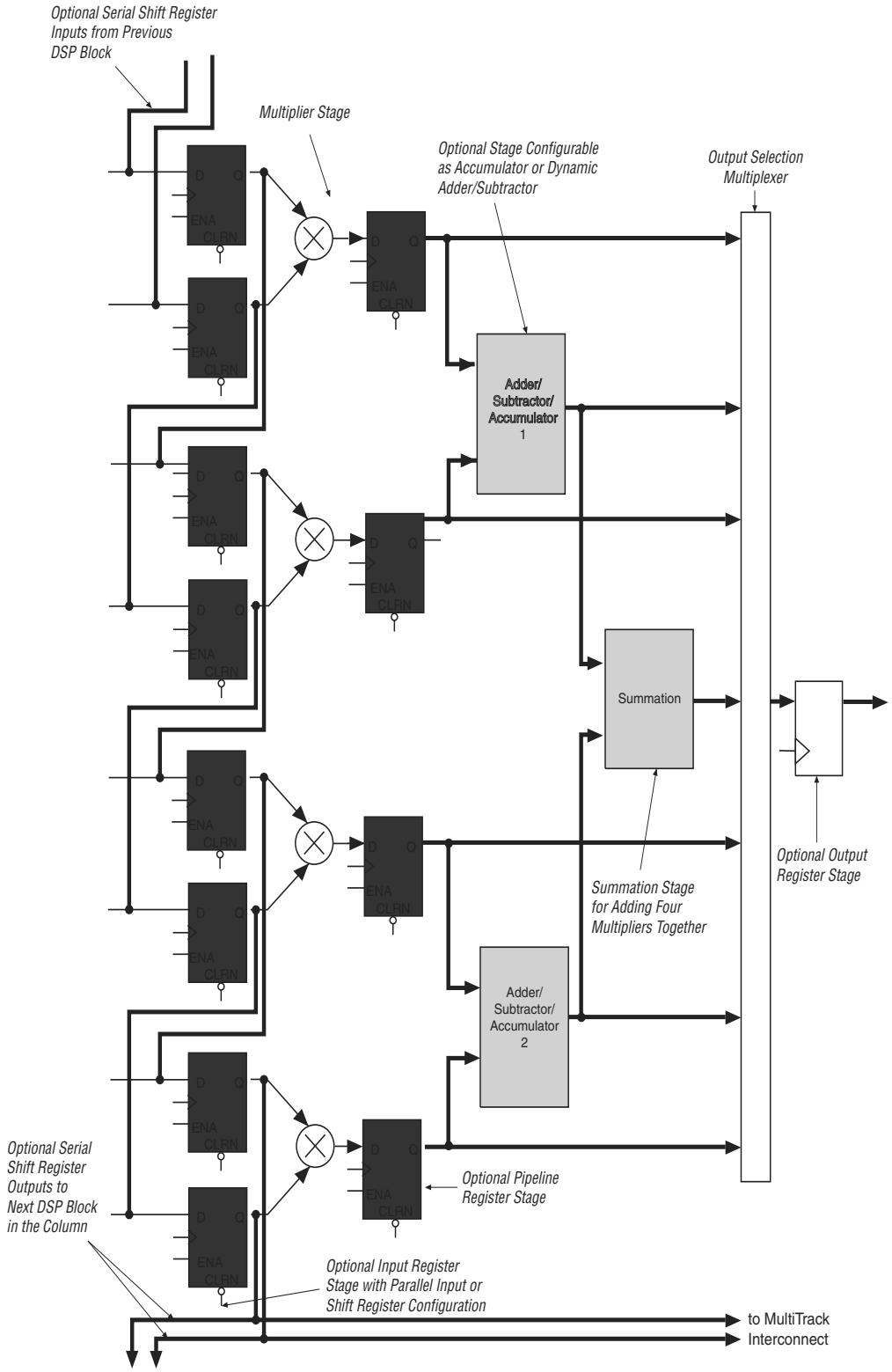
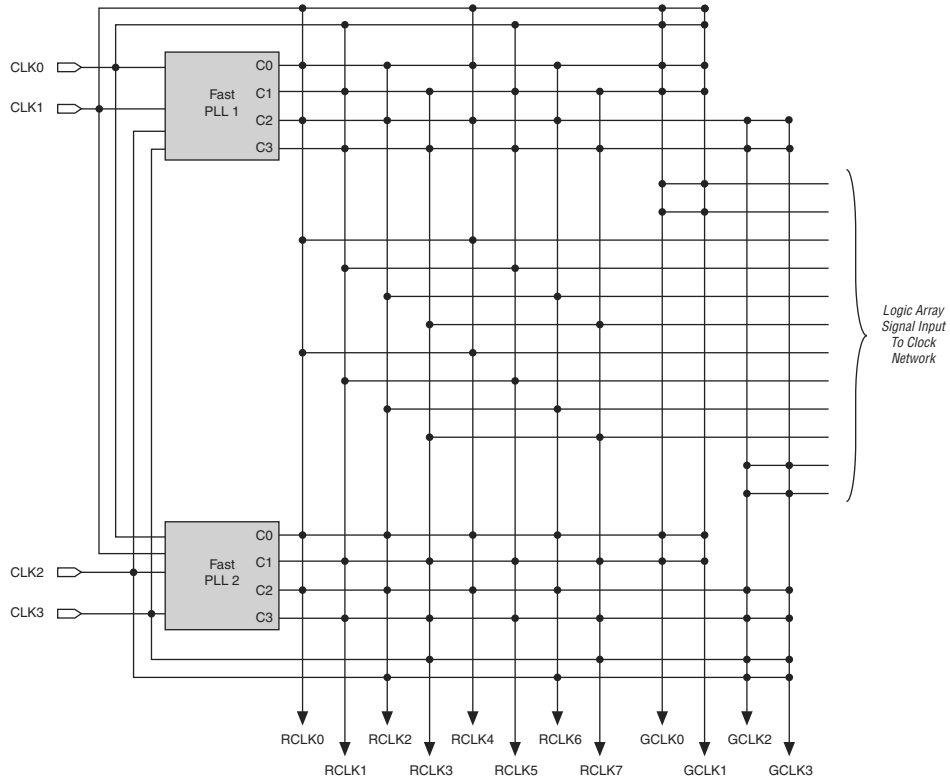


Figure 2–62. Global and Regional Clock Connections from Center Clock Pins and Fast PLL Outputs *(Note 1)*



Note to Figure 2–62:

(1) The global or regional clocks in a fast PLL's quadrant can drive the fast PLL input. A dedicated clock input pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

Table 2–19. Global and Regional Clock Connections from Left Side Clock Pins and Fast PLL Outputs (Part 2 of 2)

Left Side Global & Regional Clock Network Connectivity	CLK0	CLK1	CLK2	CLK3	RCLK0	RCLK1	RCLK2	RCLK3	RCLK4	RCLK5	RCLK6	RCLK7
RCLKDRV7	—	—	—	—	—	—	—	✓	—	—	—	✓
PLL 1 Outputs												
c0	✓	✓	—	—	✓	—	✓	—	✓	—	✓	—
c1	✓	✓	—	—	—	✓	—	✓		✓	—	✓
c2	—	—	✓	✓	✓	—	✓	—	✓	—	✓	—
c3	—	—	✓	✓	—	✓	—	✓	—	✓	—	✓
PLL 2 Outputs												
c0	✓	✓	—	—	—	✓	—	✓	—	✓	—	✓
c1	✓	✓	—	—	✓	—	✓	—	✓	—	✓	—
c2	—	—	✓	✓	—	✓	—	✓	—	✓	—	✓
c3	—	—	✓	✓	✓	—	✓	—	✓	—	✓	—
PLL 7 Outputs												
c0	—	—	✓	✓	—	✓	—	✓	—	—	—	—
c1	—	—	✓	✓	✓	—	✓	—	—	—	—	—
c2	✓	✓	—	—	—	✓	—	✓	—	—	—	—
c3	✓	✓	—	—	✓	—	✓	—	—	—	—	—
PLL 8 Outputs												
c0	—	—	✓	✓	—	—	—	—	✓	—	✓	—
c1	—	—	✓	✓	—	—	—	—	—	✓	—	✓
c2	✓	✓	—	—	—	—	—	—	✓	—	✓	—
c3	✓	✓	—	—	—	—	—	—	—	✓	—	✓

Table 2–21. Global and Regional Clock Connections from Bottom Clock Pins and Enhanced PLL Outputs

Bottom Side Global and Regional Clock Network Connectivity	DLLCLK	CLK4	CLK5	CLK6	CLK7	RCLK8	RCLK9	RCLK10	RCLK11	RCLK12	RCLK13	RCLK14	RCLK15
Clock pins													
CLK4p	✓	✓	✓	—	—	✓	—	—	—	✓	—	—	—
CLK5p	✓	✓	✓	—	—	—	✓	—	—	—	✓	—	—
CLK6p	✓	—	—	✓	✓	—	—	✓	—	—	—	✓	—
CLK7p	✓	—	—	✓	✓	—	—	—	✓	—	—	—	✓
CLK4n	—	✓	—	—	—	✓	—	—	—	✓	—	—	—
CLK5n	—	—	✓	—	—	—	✓	—	—	—	✓	—	—
CLK6n	—	—	—	✓	—	—	—	✓	—	—	—	✓	—
CLK7n	—	—	—	—	✓	—	—	—	✓	—	—	—	✓
Drivers from internal logic													
GCLKDRV0	—	✓	—	—	—	—	—	—	—	—	—	—	—
GCLKDRV1	—	—	✓	—	—	—	—	—	—	—	—	—	—
GCLKDRV2	—	—	—	✓	—	—	—	—	—	—	—	—	—
GCLKDRV3	—	—	—	—	✓	—	—	—	—	—	—	—	—
RCLKDRV0	—	—	—	—	—	✓	—	—	—	✓	—	—	—
RCLKDRV1	—	—	—	—	—	—	✓	—	—	—	✓	—	—
RCLKDRV2	—	—	—	—	—	—	—	✓	—	—	—	✓	—
RCLKDRV3	—	—	—	—	—	—	—	—	✓	—	—	—	✓
RCLKDRV4	—	—	—	—	—	✓	—	—	—	✓	—	—	—
RCLKDRV5	—	—	—	—	—	—	✓	—	—	—	✓	—	—
RCLKDRV6	—	—	—	—	—	—	—	✓	—	—	—	✓	—
RCLKDRV7	—	—	—	—	—	—	—	—	✓	—	—	—	✓
Enhanced PLL 6 outputs													
c0	✓	✓	✓	—	—	✓	—	—	—	✓	—	—	—
c1	✓	✓	✓	—	—	—	✓	—	—	—	✓	—	—
c2	✓	—	—	✓	✓	—	—	✓	—	—		✓	
c3	✓	—	—	✓	✓	—	—	—	✓	—	—	—	✓
c4	✓	—	—	—	—	✓	—	✓	—	✓	—	✓	—
c5	✓	—	—	—	—	—	✓	—	✓	—	✓	—	✓
Enhanced PLL 12 outputs													
c0	—	✓	✓	—	—	✓	—	—	—	✓	—	—	—
c1	—	✓	✓	—	—	—	✓	—	—	—	✓	—	—
c2	—	—	—	✓	✓	—	—	✓	—	—	—	✓	—
c3	—	—	—	✓	✓	—	—	—	✓	—	—	—	✓
c4	—	—	—	—	—	✓	—	✓	—	✓	—	✓	—
c5	—	—	—	—	—	—	✓	—	✓	—	✓	—	✓

Arria GX devices provide two types of termination:

- On-chip differential termination (R_D OCT)
- On-chip series termination (R_S OCT)

Table 2–26 lists the Arria GX OCT support per I/O bank.

Table 2–26. On-Chip Termination Support by I/O Banks

On-Chip Termination Support	I/O Standard Support	Top and Bottom Banks (3, 4, 7, 8)	Left Bank (1, 2)
Series termination	3.3-V LVTTL	✓	✓
	3.3-V LVCMOS	✓	✓
	2.5-V LVTTL	✓	✓
	2.5-V LVCMOS	✓	✓
	1.8-V LVTTL	✓	✓
	1.8-V LVCMOS	✓	✓
	1.5-V LVTTL	✓	✓
	1.5-V LVCMOS	✓	✓
	SSTL-2 class I and II	✓	✓
	SSTL-18 class I	✓	✓
	SSTL-18 class II	✓	—
	1.8-V HSTL class I	✓	✓
	1.8-V HSTL class II	✓	—
	1.5-V HSTL class I	✓	✓
	1.2-V HSTL	✓	—
Differential termination *(1)*	LVDS	—	✓
	HyperTransport technology	—	✓

Note to Table 2–26:

(1) Clock pins `CLK1` and `CLK3`, and pins `FPLL[7..8]CLK` do not support differential on-chip termination. Clock pins `CLK0` and `CLK2`, do support differential on-chip termination. Clock pins in the top and bottom banks (`CLK[4..7, 12..15]`) do not support differential on-chip termination.

On-Chip Differential Termination (R_D OCT)

Arria GX devices support internal differential termination with a nominal resistance value of 100 Ω for LVDS input receiver buffers. LVPECL input signals (supported on clock pins only) require an external termination resistor. R_D OCT is supported across the full range of supported differential data rates as shown in the *High-Speed I/O Specifications* section of the *DC & Switching Characteristics* chapter.

For more information about R_D OCT, refer to the *High-Speed Differential I/O Interfaces with DPA in Arria GX Devices* chapter.

For more information about tolerance specifications for R_D OCT, refer to the *DC & Switching Characteristics* chapter.

On-Chip Series Termination (R_S OCT)

Arria GX devices support driver impedance matching to provide the I/O driver with controlled output impedance that closely matches the impedance of the transmission line. As a result, reflections can be significantly reduced. Arria GX devices support R_S OCT for single-ended I/O standards with typical R_S values of 25 and 50 Ω. Once matching impedance is selected, current drive strength is no longer selectable. Table 2–26 shows the list of output standards that support R_S OCT.

For more information about R_S OCT supported by Arria GX devices, refer to the *Selectable I/O Standards in Arria GX Devices* chapter.

For more information about tolerance specifications for OCT without calibration, refer to the *DC & Switching Characteristics* chapter.

MultiVolt I/O Interface

The Arria GX architecture supports the MultiVolt I/O interface feature that allows Arria GX devices in all packages to interface with systems of different supply voltages. Arria GX VCCINT pins must always be connected to a 1.2-V power supply. With a 1.2-V V_{CCINT} level, input pins are 1.2-, 1.5-, 1.8-, 2.5-, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.2-, 1.5-, 1.8-, 2.5-, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (for example, when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). Arria GX VCCPD power pins must be connected to a 3.3-V power supply. These power pins are used to supply the pre-driver power to the output buffers, which increases the performance of the output pins. The VCCPD pins also power configuration input pins and JTAG input pins.

Table 2–27 lists Arria GX MultiVolt I/O support.

Table 2–27. Arria GX MultiVolt I/O Support *(Note 1)*

V_{CCIO} (V)	Input Signal (V)					Output Signal (V)					
	1.2	1.5	1.8	2.5	3.3	1.2	1.5	1.8	2.5	3.3	5.0
1.2	*(4)*	✓ *(2)*	✓ *(2)*	✓ *(2)*	✓ *(2)*	✓ *(4)*	—	—	—	—	—
1.5	*(4)*	✓	✓	✓ *(2)*	✓ *(2)*	✓ *(3)*	✓	—	—	—	—
1.8	*(4)*	✓	✓	✓ *(2)*	✓ *(2)*	✓ *(3)*	✓ *(3)*	✓	—	—	—
2.5	*(4)*	—	—	✓	✓	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓	—	—
3.3	*(4)*	—	—	✓	✓	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓	✓

Notes to Table 2–27:

(1) To drive inputs higher than V_{CCIO} but less than 4.0 V, disable the PCI clamping diode and select the **Allow LVTTL and LVCMOS input levels to overdrive input buffer** option in the Quartus II software.

(2) The pin current may be slightly higher than the default value. You must verify that the driving device's V_{OL} maximum and V_{OH} minimum voltages do not violate the applicable Arria GX V_{IL} maximum and V_{IH} minimum voltage specifications.

(3) Although V_{CCIO} specifies the voltage necessary for the Arria GX device to drive out, a receiving device powered at a different level can still interface with the Arria GX device if it has inputs that tolerate the V_{CCIO} value.

(4) Arria GX devices support 1.2-V HSTL. They do not support 1.2-V LVTTL and 1.2-V LVCMOS.

Table 4–54. EP1AGX35 Row Pins Input Timing Parameters (Part 2 of 2)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
SSTL-18 CLASS II	GCLK	t_{SU}	1.417	1.417	3.118	ns
		t_H	–1.312	–1.312	–2.841	ns
	GCLK PLL	t_{SU}	2.836	2.836	6.190	ns
		t_H	–2.731	–2.731	–5.913	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	1.417	1.417	3.118	ns
		t_H	–1.312	–1.312	–2.841	ns
	GCLK PLL	t_{SU}	2.836	2.836	6.190	ns
		t_H	–2.731	–2.731	–5.913	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	1.417	1.417	3.118	ns
		t_H	–1.312	–1.312	–2.841	ns
	GCLK PLL	t_{SU}	2.836	2.836	6.190	ns
		t_H	–2.731	–2.731	–5.913	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.443	1.443	3.246	ns
		t_H	–1.338	–1.338	–2.969	ns
	GCLK PLL	t_{SU}	2.862	2.862	6.318	ns
		t_H	–2.757	–2.757	–6.041	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.443	1.443	3.246	ns
		t_H	–1.338	–1.338	–2.969	ns
	GCLK PLL	t_{SU}	2.862	2.862	6.318	ns
		t_H	–2.757	–2.757	–6.041	ns
LVDS	GCLK	t_{SU}	1.341	1.341	3.088	ns
		t_H	–1.236	–1.236	–2.811	ns
	GCLK PLL	t_{SU}	2.769	2.769	6.171	ns
		t_H	–2.664	–2.664	–5.894	ns

Table 4–55 lists I/O timing specifications.

Table 4–55. EP1AGX35 Column Pins Input Timing Parameters (Part 1 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.251	1.251	2.915	ns
		t_H	–1.146	–1.146	–2.638	ns
	GCLK PLL	t_{SU}	2.693	2.693	6.021	ns
		t_H	–2.588	–2.588	–5.744	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.251	1.251	2.915	ns
		t_H	–1.146	–1.146	–2.638	ns
	GCLK PLL	t_{SU}	2.693	2.693	6.021	ns
		t_H	–2.588	–2.588	–5.744	ns

Table 4–68. EP1AGX60 Row Pins Output Timing Parameters (Part 2 of 2)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.774	2.774	6.057	ns
		GCLK PLL	t_{CO}	1.211	1.211	2.633	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.750	2.750	5.981	ns
		GCLK PLL	t_{CO}	1.187	1.187	2.557	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.716	2.716	5.850	ns
		GCLK PLL	t_{CO}	1.153	1.153	2.426	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.776	2.776	6.025	ns
		GCLK PLL	t_{CO}	1.204	1.204	2.582	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.780	2.780	5.954	ns
		GCLK PLL	t_{CO}	1.208	1.208	2.511	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.756	2.756	5.937	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.494	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.759	2.759	5.916	ns
		GCLK PLL	t_{CO}	1.187	1.187	2.473	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.757	2.757	5.935	ns
		GCLK PLL	t_{CO}	1.185	1.185	2.492	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.760	2.760	5.899	ns
		GCLK PLL	t_{CO}	1.188	1.188	2.456	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.742	2.742	5.895	ns
		GCLK PLL	t_{CO}	1.170	1.170	2.452	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.746	2.746	5.884	ns
		GCLK PLL	t_{CO}	1.174	1.174	2.441	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.737	2.737	5.883	ns
		GCLK PLL	t_{CO}	1.165	1.165	2.440	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.756	2.756	5.912	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.469	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.759	2.759	5.898	ns
		GCLK PLL	t_{CO}	1.187	1.187	2.455	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.744	2.744	5.890	ns
		GCLK PLL	t_{CO}	1.172	1.172	2.447	ns
LVDS	—	GCLK	t_{CO}	2.787	2.787	6.037	ns
		GCLK PLL	t_{CO}	1.228	1.228	2.618	ns

Table 4–74. EP1AGX90 Row Pins Output Timing Parameters (Part 2 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
1.8 V	2 mA	GCLK	t_{CO}	3.087	3.087	7.723	ns
		GCLK PLL	t_{CO}	1.034	1.034	3.605	ns
1.8 V	4 mA	GCLK	t_{CO}	3.076	3.076	6.944	ns
		GCLK PLL	t_{CO}	1.023	1.023	2.826	ns
1.8 V	6 mA	GCLK	t_{CO}	2.965	2.965	6.643	ns
		GCLK PLL	t_{CO}	0.912	0.912	2.525	ns
1.8 V	8 mA	GCLK	t_{CO}	2.934	2.934	6.529	ns
		GCLK PLL	t_{CO}	0.881	0.881	2.411	ns
1.5 V	2 mA	GCLK	t_{CO}	3.047	3.047	7.222	ns
		GCLK PLL	t_{CO}	0.994	0.994	3.104	ns
1.5 V	4 mA	GCLK	t_{CO}	2.940	2.940	6.621	ns
		GCLK PLL	t_{CO}	0.887	0.887	2.503	ns
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.890	2.890	6.294	ns
		GCLK PLL	t_{CO}	0.824	0.824	2.157	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.866	2.866	6.218	ns
		GCLK PLL	t_{CO}	0.800	0.800	2.081	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.832	2.832	6.087	ns
		GCLK PLL	t_{CO}	0.766	0.766	1.950	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.872	2.872	6.227	ns
		GCLK PLL	t_{CO}	0.819	0.819	2.109	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.878	2.878	6.162	ns
		GCLK PLL	t_{CO}	0.800	0.800	2.006	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.854	2.854	6.145	ns
		GCLK PLL	t_{CO}	0.776	0.776	1.989	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.857	2.857	6.124	ns
		GCLK PLL	t_{CO}	0.779	0.779	1.968	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.853	2.853	6.137	ns
		GCLK PLL	t_{CO}	0.800	0.800	2.019	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.858	2.858	6.107	ns
		GCLK PLL	t_{CO}	0.780	0.780	1.951	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.840	2.840	6.103	ns
		GCLK PLL	t_{CO}	0.762	0.762	1.947	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.844	2.844	6.092	ns
		GCLK PLL	t_{CO}	0.766	0.766	1.936	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.835	2.835	6.091	ns
		GCLK PLL	t_{CO}	0.757	0.757	1.935	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.852	2.852	6.114	ns
		GCLK PLL	t_{CO}	0.799	0.799	1.996	ns

Table 4–90 lists clock timing specifications.

Table 4–90. EP1AGX50 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.653	1.653	3.841	ns
t_{COUT}	1.651	1.651	3.839	ns
t_{PLLCIN}	0.245	0.245	0.755	ns
$t_{PLLCOUT}$	0.245	0.245	0.755	ns

EP1AGX60 Clock Timing Parameters

Table 4–91 to Table 4–92 on page 4–82 list the GCLK clock timing parameters for EP1AGX60 devices.

Table 4–91 lists clock timing specifications.

Table 4–91. EP1AGX60 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.531	1.531	3.593	ns
t_{COUT}	1.536	1.536	3.587	ns
t_{PLLCIN}	–0.023	–0.023	0.188	ns
$t_{PLLCOUT}$	–0.018	–0.018	0.182	ns

Table 4–92 lists clock timing specifications.

Table 4–92. EP1AGX60 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.792	1.792	4.165	ns
t_{COUT}	1.792	1.792	4.165	ns
t_{PLLCIN}	0.238	0.238	0.758	ns
$t_{PLLCOUT}$	0.238	0.238	0.758	ns

Table 4–93 through Table 4–94 list the RCLK clock timing parameters for EP1AGX60 devices.

Table 4–93 lists clock timing specifications.

Table 4–93. EP1AGX60 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.382	1.382	3.268	ns
t_{COUT}	1.387	1.387	3.262	ns
t_{PLLCIN}	–0.031	–0.031	0.174	ns
$t_{PLLCOUT}$	–0.026	–0.026	0.168	ns

Table 4–94 lists clock timing specifications.

Table 4–94. EP1AGX60 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.649	1.649	3.835	ns
t_{COUT}	1.651	1.651	3.839	ns
t_{PLLCIN}	0.245	0.245	0.755	ns
$t_{PLLCOUT}$	0.245	0.245	0.755	ns

EP1AGX90 Clock Timing Parameters

Table 4–95 through Table 4–96 list the GCLK clock timing parameters for EP1AGX90 devices.

Table 4–95 lists clock timing specifications.

Table 4–95. EP1AGX90 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.630	1.630	3.799	ns
t_{COUT}	1.635	1.635	3.793	ns
t_{PLLCIN}	–0.422	–0.422	–0.310	ns
$t_{PLLCOUT}$	–0.417	–0.417	–0.316	ns

Table 4–96 lists clock timing specifications.

Table 4–96. EP1AGX90 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.904	1.904	4.376	ns
t_{COUT}	1.904	1.904	4.376	ns
t_{PLLCIN}	–0.153	–0.153	0.254	ns
$t_{PLLCOUT}$	–0.153	–0.153	0.254	ns

Table 4–97 through Table 4–98 list the RCLK clock timing parameters for EP1AGX90 devices.

Table 4–97 lists clock timing specifications.

Table 4–97. EP1AGX90 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.462	1.462	3.407	ns
t_{COUT}	1.467	1.467	3.401	ns
t_{PLLCIN}	–0.430	–0.430	–0.322	ns
$t_{PLLCOUT}$	–0.425	–0.425	–0.328	ns

Table 4–98 lists clock timing specifications.

Table 4–98. EP1AGX90 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.760	1.760	4.011	ns
t_{COUT}	1.760	1.760	4.011	ns
t_{PLLCIN}	–0.118	–0.118	0.303	ns
$t_{PLLCOUT}$	–0.118	–0.118	0.303	ns

Block Performance

Table 4–99 shows the Arria GX performance for some common designs. All performance values were obtained with the Quartus II software compilation of library of parameterized modules (LPM) or MegaCore functions for finite impulse response (FIR) and fast Fourier transform (FFT) designs.