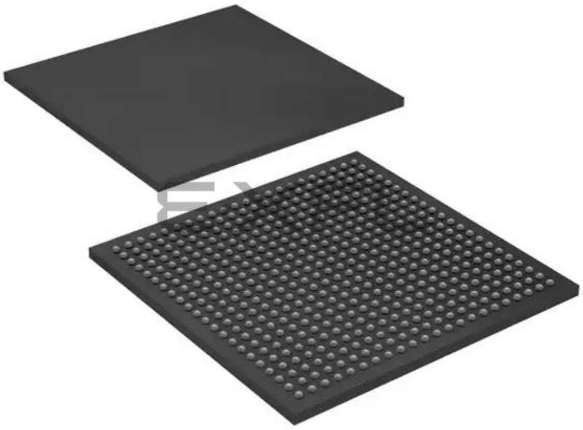

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	2508
Number of Logic Elements/Cells	50160
Total RAM Bits	2475072
Number of I/O	229
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1agx50cf484c6

Transmit State Machine

The transmit state machine operates in either PCI Express (PIPE) mode, XAUI mode, or GIGE mode, depending on the protocol used.

GIGE Mode

In GIGE mode, the transmit state machine converts all idle ordered sets (/K28.5/, /Dx.y/) to either /I1/ or /I2/ ordered sets. The /I1/ set consists of a negative-ending disparity /K28.5/ (denoted by /K28.5/-), followed by a neutral /D5.6/. The /I2/ set consists of a positive-ending disparity /K28.5/ (denoted by /K28.5/+) and a negative-ending disparity /D16.2/ (denoted by /D16.2/-). The transmit state machines do not convert any of the ordered sets to match /C1/ or /C2/, which are the configuration ordered sets. (/C1/ and /C2/ are defined by [/K28.5/, /D21.5/] and [/K28.5/, /D2.2/], respectively). Both the /I1/ and /I2/ ordered sets guarantee a negative-ending disparity after each ordered set.

XAUI Mode

The transmit state machine translates the XAUI XGMII code group to the XAUI PCS code group. Table 2–3 lists the code conversion.

Table 2–3. On-Chip Termination Support by I/O Banks

XGMII TXC	XGMII TXD	PCS Code-Group	Description
0	00 through FF	Dxx.y	Normal data
1	07	K28.0 or K28.3 or K28.5	Idle in ||I||
1	07	K28.5	Idle in ||T||
1	9C	K28.4	Sequence
1	FB	K27.7	Start
1	FD	K29.7	Terminate
1	FE	K30.7	Error
1	Refer to IEEE 802.3 reserved code groups	Refer to IEEE 802.3 reserved code groups	Reserved code groups
1	Other value	K30.7	Invalid XGMII character

The XAUI PCS idle code groups, /K28.0/ (/R/) and /K28.5/ (/K/), are automatically randomized based on a PRBS7 pattern with an $\times 7 + \times 6 + 1$ polynomial. The /K28.3/ (/A/) code group is automatically generated between 16 and 31 idle code groups. The idle randomization on the /A/, /K/, and /R/ code groups is automatically done by the transmit state machine.

Serializer (Parallel-to-Serial Converter)

The serializer block clocks in 8- or 10-bit encoded data from the 8B/10B encoder using the low-speed parallel clock and clocks out serial data using the high-speed serial clock from the central or local clock divider blocks. The serializer feeds the data LSB to MSB to the transmitter output buffer.

The transmitter PLL multiplies the input reference clock to generate a high-speed serial clock at a frequency that is half the data rate of the configured functional mode. This high-speed serial clock (or its divide-by-two version if the functional mode uses byte serializer) is fed to the CMU clock divider block. Depending on the configured functional mode, the CMU clock divider block divides the high-speed serial clock to generate the low-speed parallel clock that clocks the transceiver PCS logic in the associated channel. The low-speed parallel clock is also forwarded to the PLD logic array on the `tx_clkout` or `coreclkout` ports.

The receiver PLL in each channel is also fed by an input reference clock. The receiver PLL along with the clock recovery unit generates a high-speed serial recovered clock and a low-speed parallel recovered clock. The low-speed parallel recovered clock feeds the receiver PCS logic until the rate matcher. The CMU low-speed parallel clock clocks the rest of the logic from the rate matcher until the receiver phase compensation FIFO. In modes that do not use a rate matcher, the receiver PCS logic is clocked by the recovered clock until the receiver phase compensation FIFO.

The input reference clock to the transmitter and receiver PLLs can be derived from:

- One of two available dedicated reference clock input pins (`REFCLK0` or `REFCLK1`) of the associated transceiver block
- PLD clock network (must be driven directly from an input clock pin and cannot be driven by user logic or enhanced PLL)
- Inter-transceiver block lines driven by reference clock input pins of other transceiver blocks

Figure 2–22 shows the input reference clock sources for the transmitter and receiver PLL.

Figure 2–22. Input Reference Clock Sources

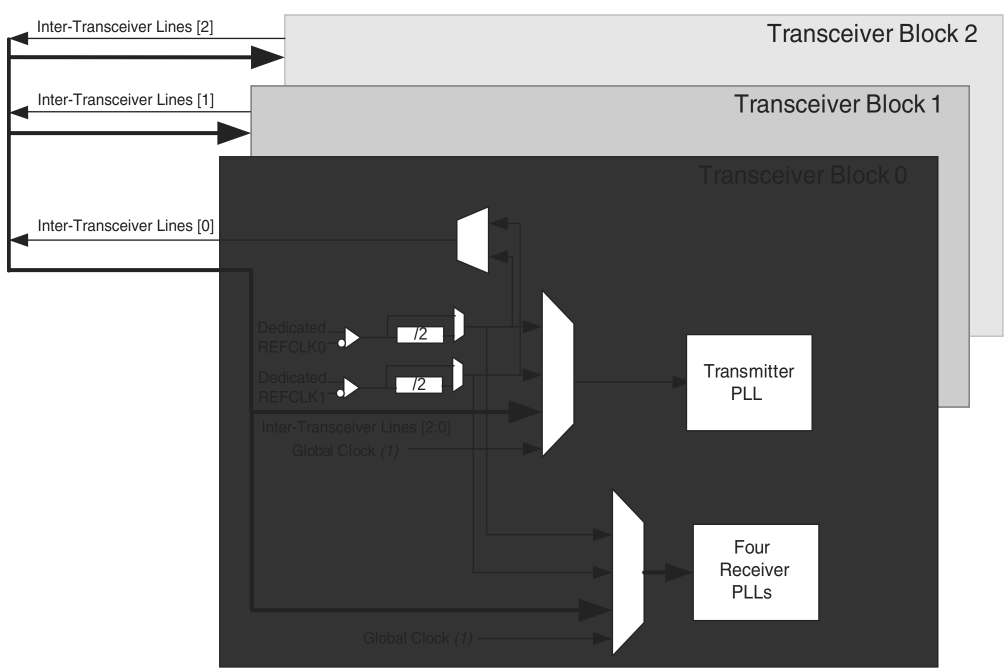
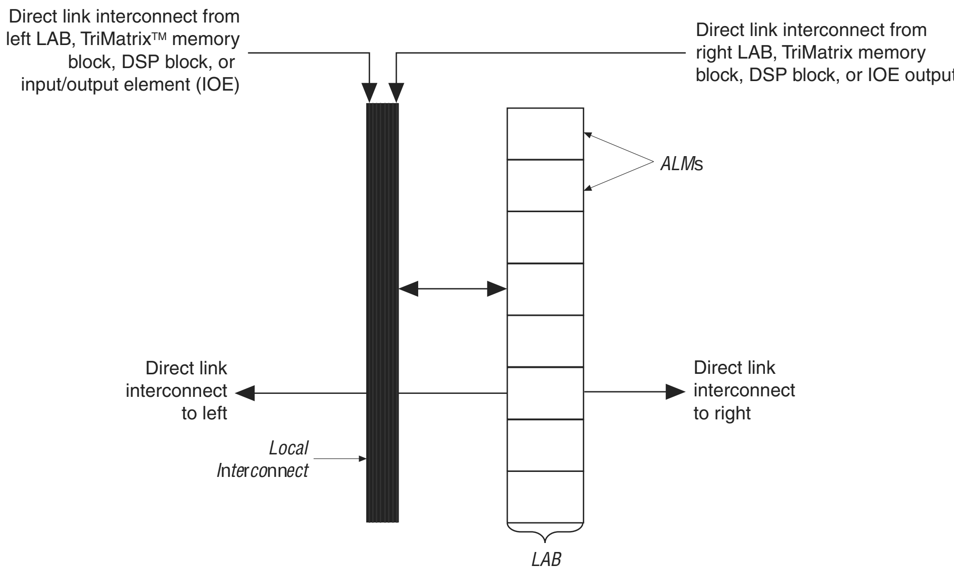


Figure 2–26 shows the direct link connection.

Figure 2–26. Direct Link Connection



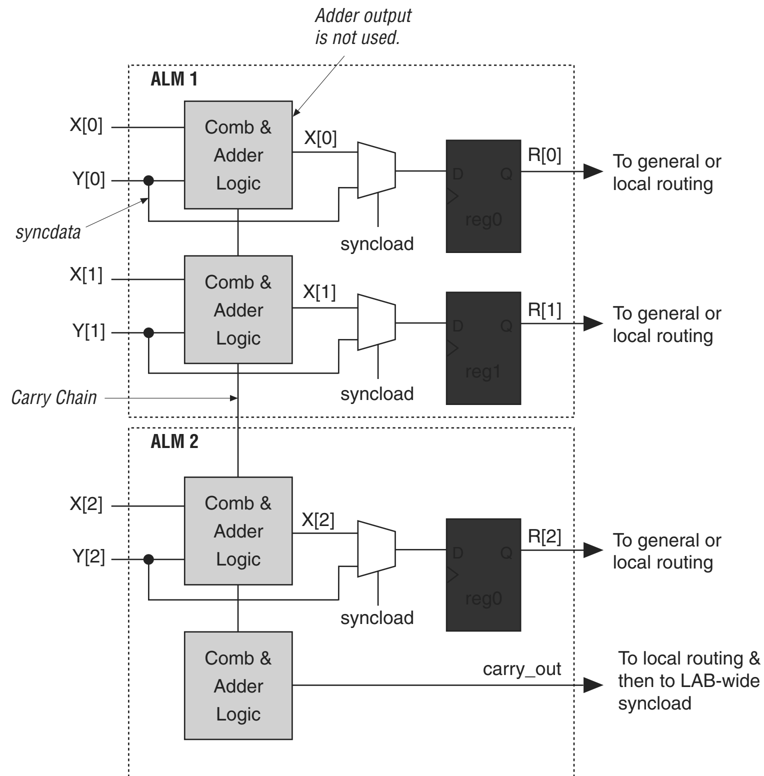
LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its ALMs. The control signals include three clocks, three clock enables, two asynchronous clears, synchronous clear, asynchronous preset or load, and synchronous load control signals, providing a maximum of 11 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use three clocks and three clock enable signals. However, there can only be up to two unique clocks per LAB, as shown in the LAB control signal generation circuit in Figure 2–27. Each LAB's clock and clock enable signals are linked. For example, any ALM in a particular LAB using the `labclk1` signal also uses `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses two LAB-wide clock signals. De-asserting the clock enable signal turns off the corresponding LAB-wide clock. Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. The asynchronous load acts as a preset when the asynchronous load data input is tied high. When the asynchronous load/preset signal is used, the `labclkena0` signal is no longer available.

The LAB row clocks `[5..0]` and LAB local interconnect generate the LAB-wide control signals. The MultiTrack interconnects have inherently low skew. This low skew allows the MultiTrack interconnects to distribute clock and control signals in addition to data.

Figure 2–35. Conditional Operation Example



Arithmetic mode also offers clock enable, counter enable, synchronous up/down control, add/subtract control, synchronous clear, and synchronous load. The LAB local interconnect data inputs generate the clock enable, counter enable, synchronous up/down and add/subtract control signals. These control signals can be used for the inputs that are shared between the four LUTs in the ALM. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

Carry Chain

Carry chain provides a fast carry function between the dedicated adders in arithmetic or shared arithmetic mode. Carry chains can begin in either the first ALM or the fifth ALM in a LAB. The final carry-out signal is routed to an ALM, where it is fed to local, row, or column interconnects.

The Quartus II Compiler automatically creates carry chain logic during compilation, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions. The Quartus II Compiler creates carry chains longer than 16 (8 ALMs in arithmetic or shared arithmetic mode) by linking LABs together automatically. For enhanced fitting, a long carry chain runs vertically allowing fast horizontal connections to TriMatrix memory and DSP blocks. A carry chain can continue as far as a full column. To avoid routing congestion in one small area of the device when a high fan-in arithmetic function is implemented, the LAB can support carry chains that only use either the top half or bottom half of the LAB before connecting to the next LAB.

chains are also top- or bottom-half bypassable. This capability allows the shared arithmetic chain to cascade through half of the ALMs in a LAB while leaving the other half available for narrower fan-in functionality. Every other LAB column is top-half bypassable, while the other LAB columns are bottom-half bypassable. For more information about shared arithmetic chain interconnect, refer to "MultiTrack Interconnect" on page 2–44.

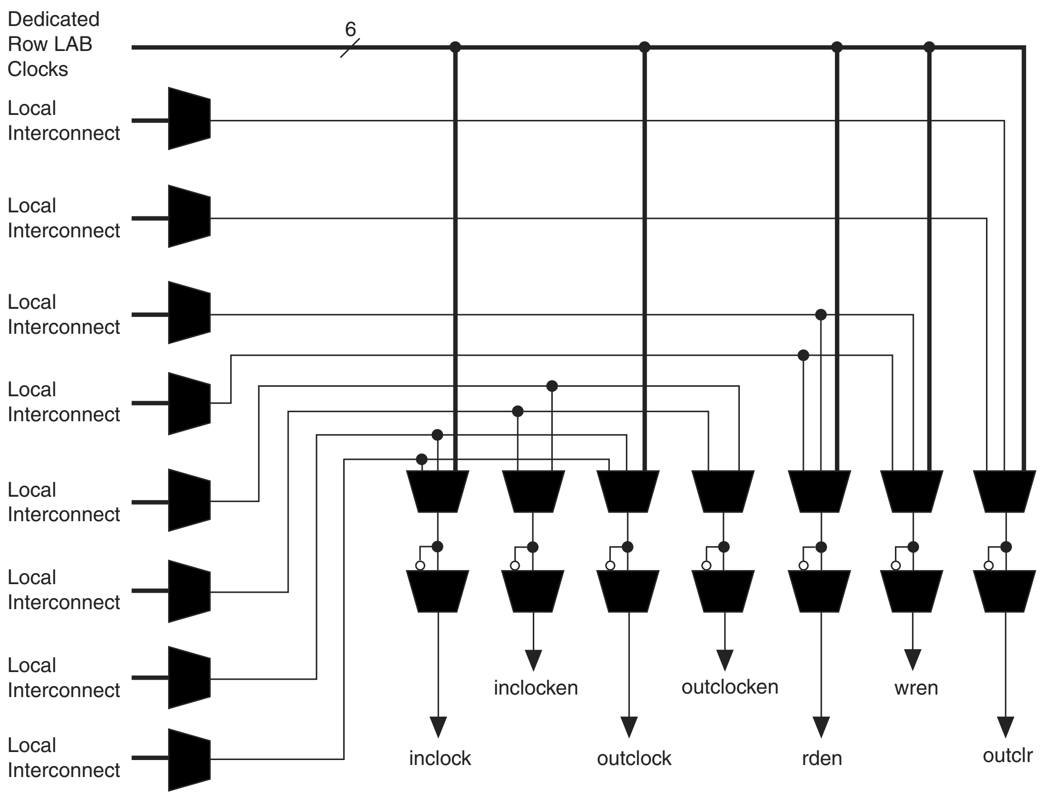
Register Chain

In addition to the general routing outputs, the ALMs in a LAB have register chain outputs. Register chain routing allows registers in the same LAB to be cascaded together. The register chain interconnect allows a LAB to use LUTs for a single combinational function and the registers to be used for an unrelated shift register implementation. These resources speed up connections between ALMs while saving local interconnect resources (refer to Figure 2–38). The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. For more information about register chain interconnect, refer to "MultiTrack Interconnect" on page 2–44.

When configured as RAM or ROM, you can use an initialization file to pre-load the memory contents.

M512 RAM blocks can have different clocks on its inputs and outputs. The `wren`, `datain`, and write address registers are all clocked together from one of the two clocks feeding the block. The read address, `rden`, and output registers can be clocked by either of the two clocks driving the block, allowing the RAM block to operate in read and write or input and output clock modes. Only the output register can be bypassed. The six `labclk` signals or local interconnect can drive the `inclock`, `outclock`, `wren`, `rden`, and `outclr` signals. Because of the advanced interconnect between the LAB and M512 RAM blocks, ALMs can also control the `wren` and `rden` signals and the RAM clock, clock enable, and asynchronous clear signals. Figure 2–42 shows the M512 RAM block control signal generation logic.

Figure 2–42. M512 RAM Block Control Signals



The RAM blocks in Arria GX devices have local interconnects to allow ALMs and interconnects to drive into RAM blocks. The M512 RAM block local interconnect is driven by the R4, C4, and direct link interconnects from adjacent LABs. The M512 RAM blocks can communicate with LABs on either the left or right side through these row interconnects or with LAB columns on the left or right side with the column interconnects. The M512 RAM block has up to 16 direct link input connections from the left adjacent LABs and another 16 from the right adjacent LAB. M512 RAM outputs can also connect to left and right LABs through direct link interconnect. The M512 RAM block has equal opportunity for access and performance to and from LABs on either its left or right side. Figure 2–43 shows the M512 RAM block to logic array interface.

Table 2–20. Global and Regional Clock Connections from Top Clock Pins and Enhanced PLL Outputs

Top Side Global and Regional Clock Network Connectivity	DLLCLK	CLK12	CLK13	CLK14	CLK15	RCLK24	RCLK25	RCLK26	RCLK27	RCLK28	RCLK29	RCLK30	RCLK31
Clock pins													
CLK12p	✓	✓	✓	—	—	✓	—	—	—	✓	—	—	—
CLK13p	✓	✓	✓	—	—	—	✓	—	—	—	✓	—	—
CLK14p	✓	—	—	✓	✓	—	—	✓	—	—	—	✓	—
CLK15p	✓	—	—	✓	✓	—	—	—	✓	—	—	—	✓
CLK12n	—	✓	—	—	—	✓	—	—	—	✓	—	—	—
CLK13n	—	—	✓	—	—	—	✓	—	—	—	✓	—	—
CLK14n	—	—	—	✓	—	—	—	✓	—	—	—	✓	—
CLK15n	—	—	—	—	✓	—	—	—	✓	—	—	—	✓
Drivers from internal logic													
GCLKDRV0	—	✓	—	—	—	—	—	—	—	—	—	—	—
GCLKDRV1	—	—	✓	—	—	—	—	—	—	—	—	—	—
GCLKDRV2	—	—	—	✓	—	—	—	—	—	—	—	—	—
GCLKDRV3	—	—	—	—	✓	—	—	—	—	—	—	—	—
RCLKDRV0	—	—	—	—	—	✓	—	—	—	✓	—	—	—
RCLKDRV1	—	—	—	—	—	—	✓	—	—	—	✓	—	—
RCLKDRV2	—	—	—	—	—	—	—	✓	—	—	—	✓	—
RCLKDRV3	—	—	—	—	—	—	—	—	✓	—	—	—	✓
RCLKDRV4	—	—	—	—	—	✓	—	—	—	✓	—	—	—
RCLKDRV5	—	—	—	—	—	—	✓	—	—	—	✓	—	—
RCLKDRV6	—	—	—	—	—	—	—	✓	—	—	—	✓	—
RCLKDRV7	—	—	—	—	—	—	—	—	✓	—	—	—	✓
Enhanced PLL5 outputs													
c0	✓	✓	✓	—	—	✓	—	—	—	✓	—	—	—
c1	✓	✓	✓	—	—	—	✓	—	—	—	✓	—	—
c2	✓	—	—	✓	✓	—	—	✓	—	—	—	✓	—
c3	✓	—	—	✓	✓	—	—	—	✓	—	—	—	✓
c4	✓	—	—	—	—	✓	—	✓	—	✓	—	✓	—
c5	✓	—	—	—	—	—	✓	—	✓	—	✓	—	✓
Enhanced PLL 11 outputs													
c0	—	✓	✓	—	—	✓	—	—	—	✓	—	—	—
c1	—	✓	✓	—	—	—	✓	—	—	—	✓	—	—
c2	—	—	—	✓	✓	—	—	✓	—	—	—	✓	—
c3	—	—	—	✓	✓	—	—	—	✓	—	—	—	✓
c4	—	—	—	—	—	✓	—	✓	—	✓	—	✓	—
c5	—	—	—	—	—	—	✓	—	✓	—	✓	—	✓

Table 4 69 lists I/O timing specifications.

Table 4–69. EP1AGX60 Column Pins Output Timing Parameters (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	3.036	3.036	6.963	ns
		GCLK PLL	t_{CO}	1.466	1.466	3.528	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.891	2.891	6.591	ns
		GCLK PLL	t_{CO}	1.321	1.321	3.156	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.824	2.824	6.591	ns
		GCLK PLL	t_{CO}	1.254	1.254	3.156	ns
3.3-V LVTTL	16 mA	GCLK	t_{CO}	2.798	2.798	6.422	ns
		GCLK PLL	t_{CO}	1.228	1.228	2.987	ns
3.3-V LVTTL	20 mA	GCLK	t_{CO}	2.776	2.776	6.297	ns
		GCLK PLL	t_{CO}	1.206	1.206	2.862	ns
3.3-V LVTTL	24 mA	GCLK	t_{CO}	2.769	2.769	6.299	ns
		GCLK PLL	t_{CO}	1.199	1.199	2.864	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.891	2.891	6.591	ns
		GCLK PLL	t_{CO}	1.321	1.321	3.156	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.799	2.799	6.296	ns
		GCLK PLL	t_{CO}	1.229	1.229	2.861	ns
3.3-V LVCMOS	12 mA	GCLK	t_{CO}	2.771	2.771	6.218	ns
		GCLK PLL	t_{CO}	1.201	1.201	2.783	ns
3.3-V LVCMOS	16 mA	GCLK	t_{CO}	2.778	2.778	6.186	ns
		GCLK PLL	t_{CO}	1.208	1.208	2.751	ns
3.3-V LVCMOS	20 mA	GCLK	t_{CO}	2.765	2.765	6.168	ns
		GCLK PLL	t_{CO}	1.195	1.195	2.733	ns
3.3-V LVCMOS	24 mA	GCLK	t_{CO}	2.754	2.754	6.146	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.711	ns
2.5 V	4 mA	GCLK	t_{CO}	2.853	2.853	6.623	ns
		GCLK PLL	t_{CO}	1.283	1.283	3.188	ns
2.5 V	8 mA	GCLK	t_{CO}	2.801	2.801	6.361	ns
		GCLK PLL	t_{CO}	1.231	1.231	2.926	ns
2.5 V	12 mA	GCLK	t_{CO}	2.780	2.780	6.244	ns
		GCLK PLL	t_{CO}	1.210	1.210	2.809	ns
2.5 V	16 mA	GCLK	t_{CO}	2.762	2.762	6.170	ns
		GCLK PLL	t_{CO}	1.192	1.192	2.735	ns
1.8 V	2 mA	GCLK	t_{CO}	2.893	2.893	7.615	ns
		GCLK PLL	t_{CO}	1.323	1.323	4.180	ns
1.8 V	4 mA	GCLK	t_{CO}	2.898	2.898	6.841	ns
		GCLK PLL	t_{CO}	1.328	1.328	3.406	ns