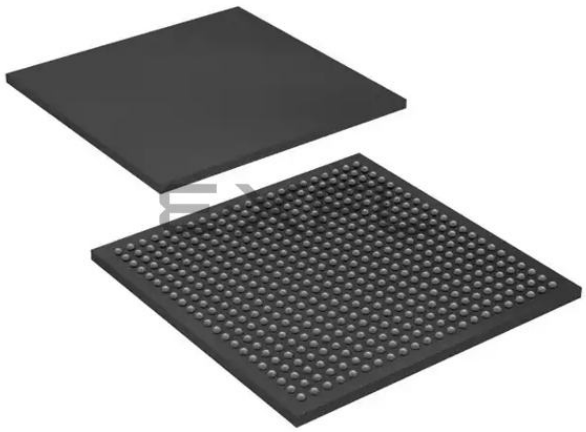

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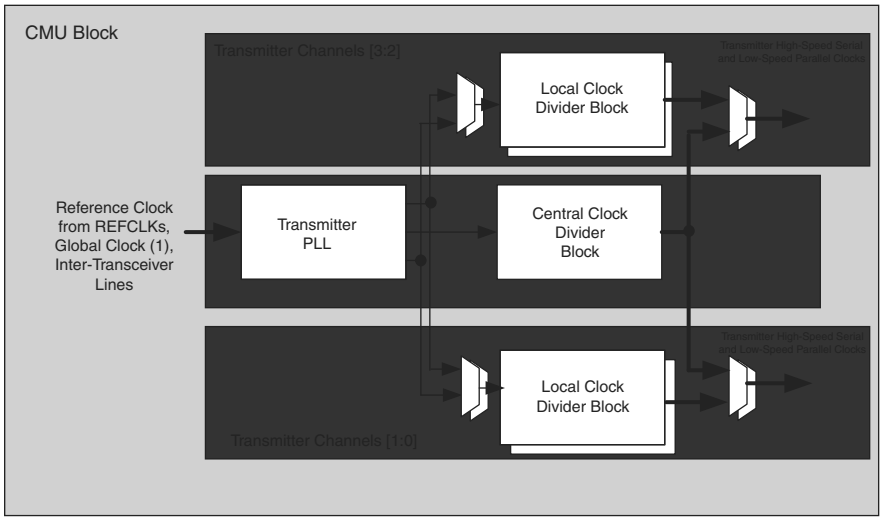
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2508
Number of Logic Elements/Cells	50160
Total RAM Bits	2475072
Number of I/O	229
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1agx50cf484c6n

Figure 2–3 shows the block diagram of the clock multiplier unit.

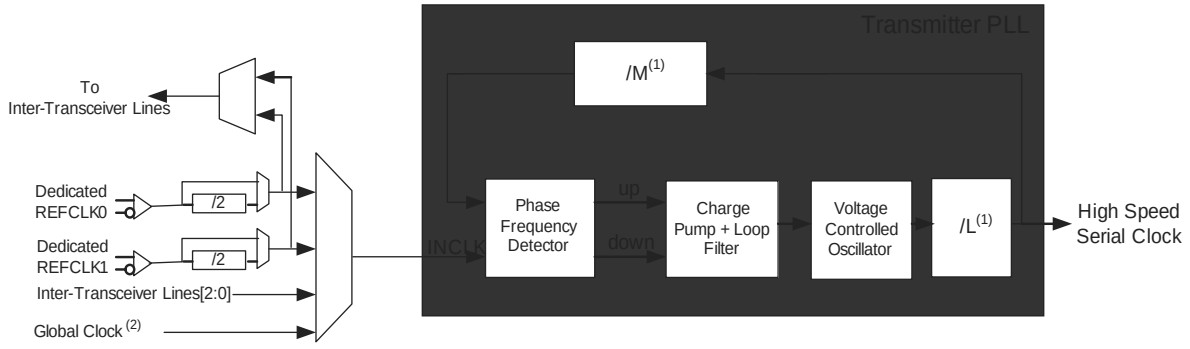
Figure 2–3. Clock Multiplier Unit



The transmitter PLL multiplies the input reference clock to generate the high-speed serial clock required to support the intended protocol. It implements a half-rate voltage controlled oscillator (VCO) that generates a clock at half the frequency of the serial data rate for which it is configured.

Figure 2–4 shows the block diagram of the transmitter PLL.

Figure 2–4. Transmitter PLL



Notes to Figure 2–4:

(1) You only need to select the protocol and the available input reference clock frequency in the ALTGXB MegaWizard Plug-In Manager. Based on your selections, the MegaWizard Plug-In Manager automatically selects the necessary /M and /L dividers (clock multiplication factors).

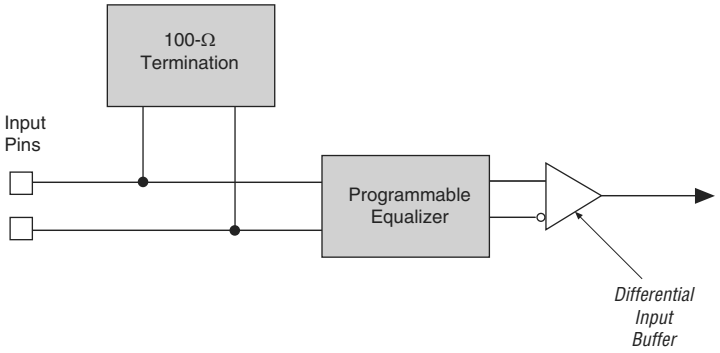
(2) The global clock line must be driven from an input pin only.

The reference clock input to the transmitter PLL can be derived from:

- One of two available dedicated reference clock input pins (`REFCLK0` or `REFCLK1`) of the associated transceiver block
- PLD global clock network (must be driven directly from an input clock pin and cannot be driven by user logic or enhanced PLL)

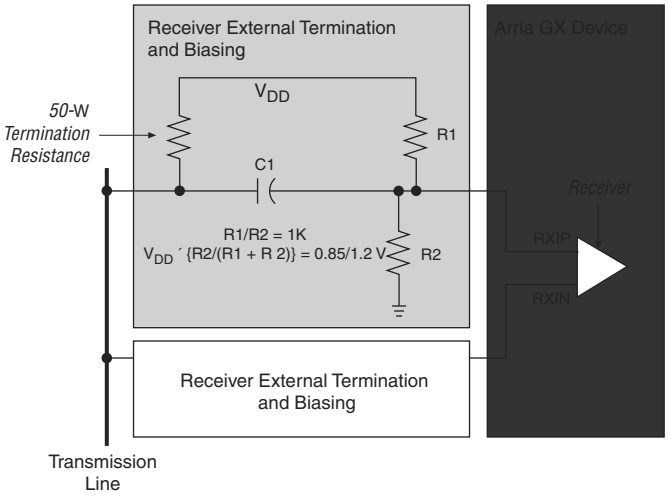
The receiver has 100-Ω on-chip differential termination (R_D OCT) for different protocols, as shown in Figure 2–11. You can disable the receiver's internal termination if external terminations and biasing are provided. The receiver and transmitter differential termination method can be set independently of each other.

Figure 2–11. Receiver Input Buffer



If a design uses external termination, the receiver must be externally terminated and biased to 0.85 V or 1.2 V. Figure 2–12 shows an example of an external termination and biasing circuit.

Figure 2–12. External Termination and Biasing Circuit



Programmable Equalizer

The Arria GX receivers provide a programmable receiver equalization feature to compensate for the effects of channel attenuation for high-speed signaling. PCB traces carrying these high-speed signals have low-pass filter characteristics. Impedance mismatch boundaries can also cause signal degradation. Equalization in the receiver diminishes the lossy attenuation effects of the PCB at high frequencies.

Byte Deserializer

Byte deserializer takes in one-byte wide data from the 8B/10B decoder and deserializes it into a two-byte wide data at half the speed. This allows clocking the PLD-receiver interface at half the speed as compared to the receiver PCS logic. The byte deserializer is bypassed in GIGE mode.

The byte ordering at the receiver output might be different than what was transmitted. This is a non-deterministic swap, because it depends on PLL lock times and link delay. If required, you must implement byte ordering logic in the PLD to correct this situation.

For more information about byte serializer, refer to the *Arria GX Transceiver Architecture* chapter.

Receiver Phase Compensation FIFO Buffer

A receiver phase compensation FIFO buffer is located at each receiver channel's logic array interface. It compensates for the phase difference between the receiver PCS clock and the local PLD receiver clock. The receiver phase compensation FIFO is used in all supported functional modes. The receiver phase compensation FIFO buffer is eight words deep in PCI Express (PIPE) mode and four words deep in all other modes.

For more information about architecture and clocking, refer to the *Arria GX Transceiver Architecture* chapter.

Loopback Modes

Arria GX transceivers support the following loopback configurations for diagnostic purposes:

- Serial loopback
- Reverse serial loopback
- Reverse serial loopback (pre-CDR)
- PCI Express (PIPE) reverse parallel loopback (available only in [PIPE] mode)

Serial Loopback

Figure 2–18 shows the transceiver data path in serial loopback.

Figure 2–18. Transceiver Data Path in Serial Loopback

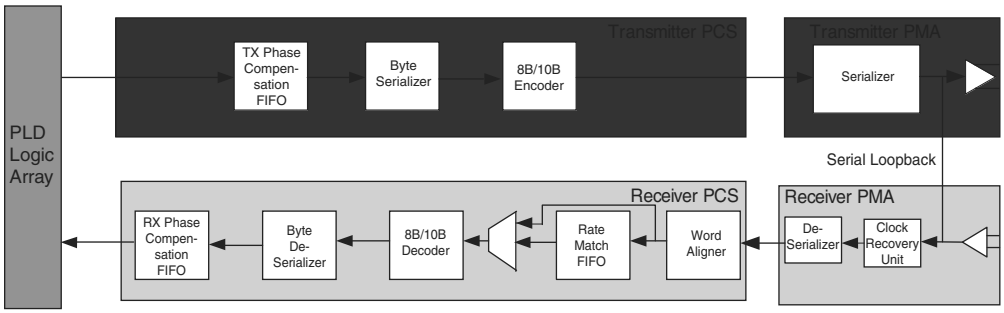
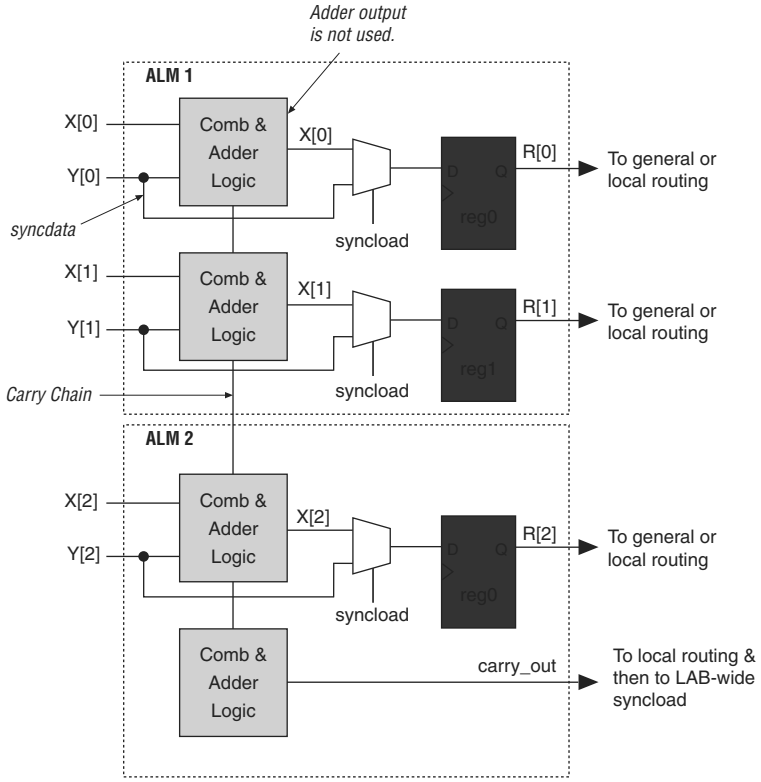


Figure 2–35. Conditional Operation Example



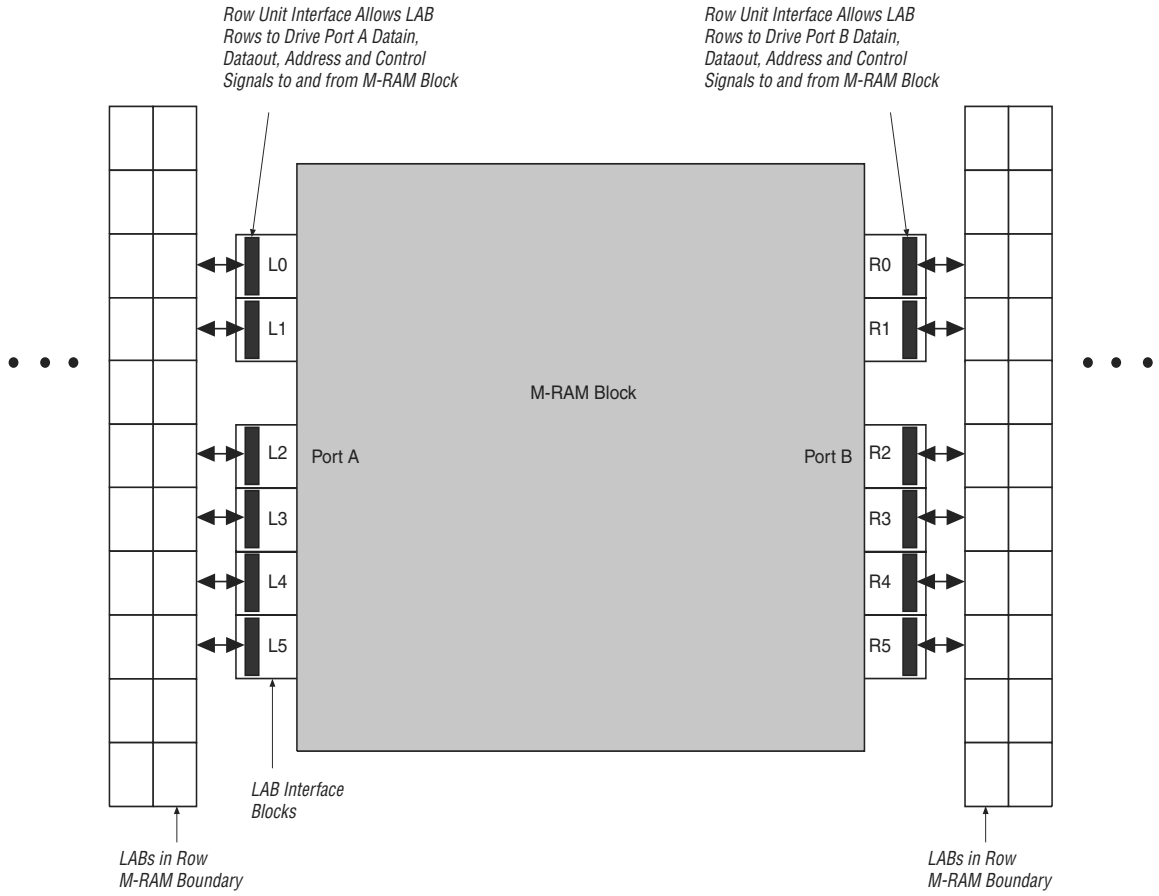
Arithmetic mode also offers clock enable, counter enable, synchronous up/down control, add/subtract control, synchronous clear, and synchronous load. The LAB local interconnect data inputs generate the clock enable, counter enable, synchronous up/down and add/subtract control signals. These control signals can be used for the inputs that are shared between the four LUTs in the ALM. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

Carry Chain

Carry chain provides a fast carry function between the dedicated adders in arithmetic or shared arithmetic mode. Carry chains can begin in either the first ALM or the fifth ALM in a LAB. The final carry-out signal is routed to an ALM, where it is fed to local, row, or column interconnects.

The Quartus II Compiler automatically creates carry chain logic during compilation, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions. The Quartus II Compiler creates carry chains longer than 16 (8 ALMs in arithmetic or shared arithmetic mode) by linking LABs together automatically. For enhanced fitting, a long carry chain runs vertically allowing fast horizontal connections to TriMatrix memory and DSP blocks. A carry chain can continue as far as a full column. To avoid routing congestion in one small area of the device when a high fan-in arithmetic function is implemented, the LAB can support carry chains that only use either the top half or bottom half of the LAB before connecting to the next LAB.

Figure 2–48. M-RAM Block LAB Row Interface *(Note 1)*



Note to Figure 2–48:

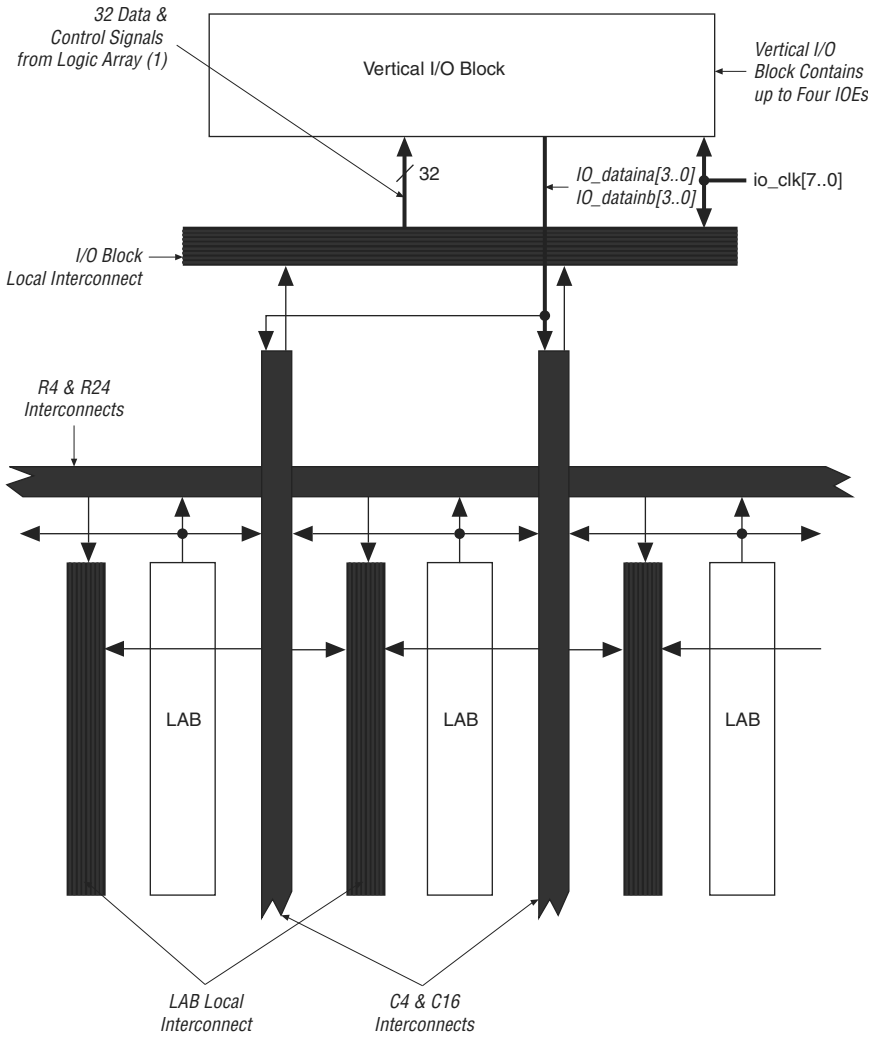
(1) Only R24 and C16 interconnects cross the M-RAM block boundaries.

Table 2–20. Global and Regional Clock Connections from Top Clock Pins and Enhanced PLL Outputs

Top Side Global and Regional Clock Network Connectivity	DLLCLK	CLK12	CLK13	CLK14	CLK15	RCLK24	RCLK25	RCLK26	RCLK27	RCLK28	RCLK29	RCLK30	RCLK31
Clock pins													
CLK12p	✓	✓	✓	—	—	✓	—	—	—	✓	—	—	—
CLK13p	✓	✓	✓	—	—	—	✓	—	—	—	✓	—	—
CLK14p	✓	—	—	✓	✓	—	—	✓	—	—	—	✓	—
CLK15p	✓	—	—	✓	✓	—	—	—	✓	—	—	—	✓
CLK12n	—	✓	—	—	—	✓	—	—	—	✓	—	—	—
CLK13n	—	—	✓	—	—	—	✓	—	—	—	✓	—	—
CLK14n	—	—	—	✓	—	—	—	✓	—	—	—	✓	—
CLK15n	—	—	—	—	✓	—	—	—	✓	—	—	—	✓
Drivers from internal logic													
GCLKDRV0	—	✓	—	—	—	—	—	—	—	—	—	—	—
GCLKDRV1	—	—	✓	—	—	—	—	—	—	—	—	—	—
GCLKDRV2	—	—	—	✓	—	—	—	—	—	—	—	—	—
GCLKDRV3	—	—	—	—	✓	—	—	—	—	—	—	—	—
RCLKDRV0	—	—	—	—	—	✓	—	—	—	✓	—	—	—
RCLKDRV1	—	—	—	—	—	—	✓	—	—	—	✓	—	—
RCLKDRV2	—	—	—	—	—	—	—	✓	—	—	—	✓	—
RCLKDRV3	—	—	—	—	—	—	—	—	✓	—	—	—	✓
RCLKDRV4	—	—	—	—	—	✓	—	—	—	✓	—	—	—
RCLKDRV5	—	—	—	—	—	—	✓	—	—	—	✓	—	—
RCLKDRV6	—	—	—	—	—	—	—	✓	—	—	—	✓	—
RCLKDRV7	—	—	—	—	—	—	—	—	✓	—	—	—	✓
Enhanced PLL5 outputs													
c0	✓	✓	✓	—	—	✓	—	—	—	✓	—	—	—
c1	✓	✓	✓	—	—	—	✓	—	—	—	✓	—	—
c2	✓	—	—	✓	✓	—	—	✓	—	—	—	✓	—
c3	✓	—	—	✓	✓	—	—	—	✓	—	—	—	✓
c4	✓	—	—	—	—	✓	—	✓	—	✓	—	✓	—
c5	✓	—	—	—	—	—	✓	—	✓	—	✓	—	✓
Enhanced PLL 11 outputs													
c0	—	✓	✓	—	—	✓	—	—	—	✓	—	—	—
c1	—	✓	✓	—	—	—	✓	—	—	—	✓	—	—
c2	—	—	—	✓	✓	—	—	✓	—	—	—	✓	—
c3	—	—	—	✓	✓	—	—	—	✓	—	—	—	✓
c4	—	—	—	—	—	✓	—	✓	—	✓	—	✓	—
c5	—	—	—	—	—	—	✓	—	✓	—	✓	—	✓

Figure 2–69 shows how a column I/O block connects to the logic array.

Figure 2–69. Column I/O Block Connection to the Interconnect



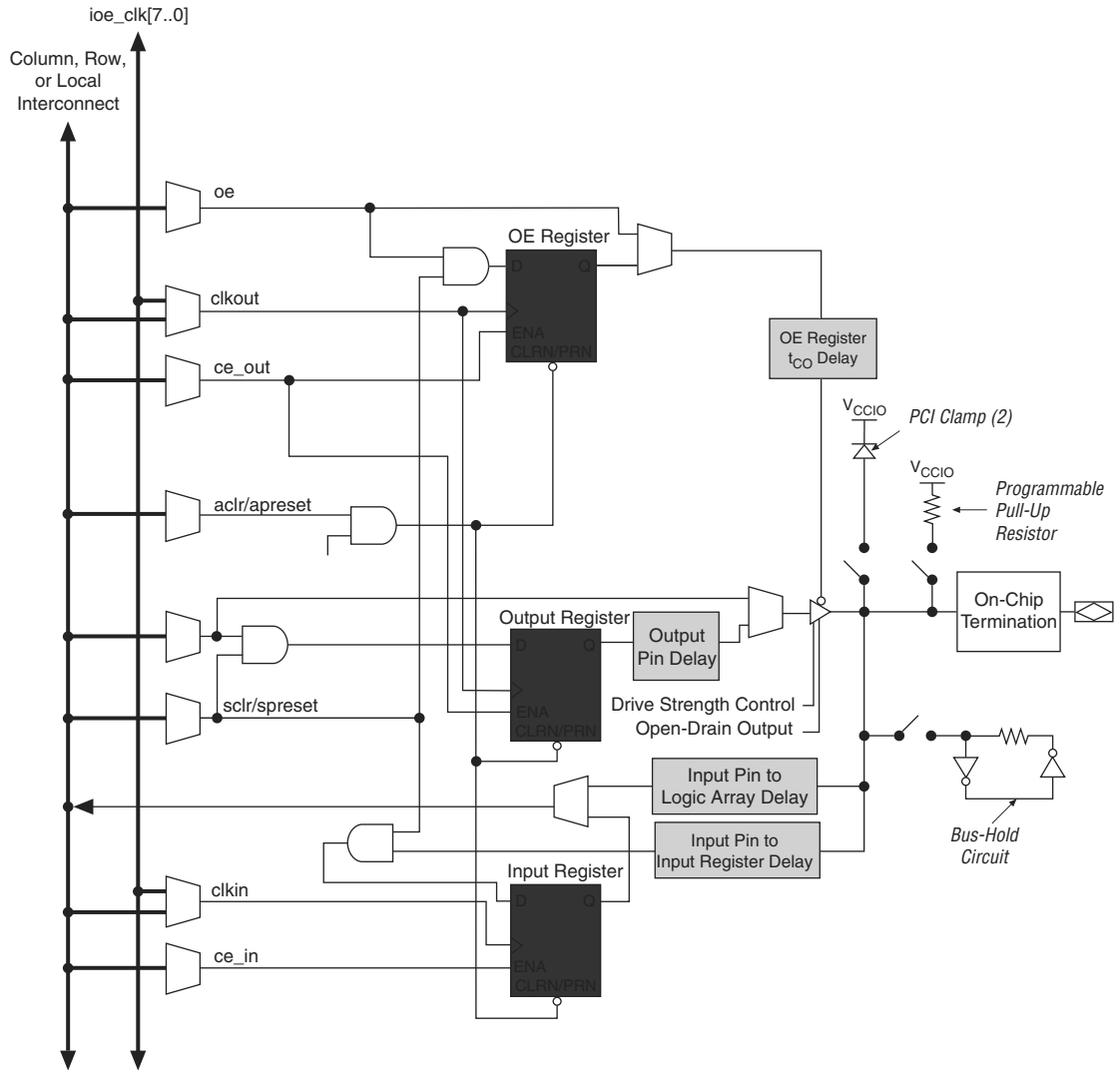
Note to Figure 2–69:

(1) The 32 data and control signals consist of eight data out lines: four lines each for DDR applications `io_dataouta[3..0]` and `io_dataoutb[3..0]`, four output enables `io_oe[3..0]`, four input clock enables `io_ce_in[3..0]`, four output clock enables `io_ce_out[3..0]`, four clocks `io_clk[3..0]`, four asynchronous clear and preset signals `io_aclr/apreset[3..0]`, and four synchronous clear and preset signals `io_sclr/spreset[3..0]`.

There are 32 control and data signals that feed each row or column I/O block. These control and data signals are driven from the logic array. The row or column IOE clocks, `io_clk[7..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. I/O clocks are generated from global or regional clocks (refer to "PLLs and Clock Networks" on page 2–66).

In normal bidirectional operation, you can use the input register for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. The output register can be used for data requiring fast clock-to-output performance. You can use the OE register for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock enable source from the local interconnect in the associated LAB, dedicated I/O clocks, and the column and row interconnects. Figure 2–72 shows the IOE in bidirectional configuration.

Figure 2–72. Arria GX IOE in Bidirectional I/O Configuration *(Note 1)*



Notes to Figure 2–72:

(1) All input signals to the IOE can be inverted at the IOE.

(2) The optional PCI clamp is only available on column I/O pins.

The Arria GX device IOE includes programmable delays that can be activated to ensure input IOE register-to-logic array register transfers, input pin-to-logic array register transfers, or output IOE register-to-pin transfers.

Table 4–7. Arria GX Transceiver Block AC Specification *(Note 1), (2), (3)* (Part 2 of 4)

Description	Condition	–6 Speed Grade Commercial & Industrial	Units
Deterministic jitter at 3.125 Gbps	REFCLK = 156.25 MHz Pattern = CJPAT V_{OD} = 1200 mV No Pre-emphasis	0.17	UI
XAUI Receiver Jitter Tolerance *(4)*			
Total jitter	Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.65	UI
Deterministic jitter	Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.37	UI
Peak-to-peak jitter	Jitter frequency = 22.1 KHz	> 8.5	UI
Peak-to-peak jitter	Jitter frequency = 1.875 MHz	> 0.1	UI
Peak-to-peak jitter	Jitter frequency = 20 MHz	> 0.1	UI
PCI Express (PIPE) Transmitter Jitter Generation *(5)*			
Total Transmitter Jitter Generation	Compliance Pattern; V_{OD} = 800 mV; Pre-emphasis = 49%	< 0.25	UI p-p
PCI Express (PIPE) Receiver Jitter Tolerance *(5)*			
Total Receiver Jitter Tolerance	Compliance Pattern; DC Gain = 3 db	> 0.6	UI p-p
Gigabit Ethernet (GIGE) Transmitter Jitter Generation *(7)*			
Total Transmitter Jitter Generation (TJ)	CRPAT: V_{OD} = 800 mV; Pre-emphasis = 0%	< 0.279	UI p-p
Deterministic Transmitter Jitter Generation (DJ)	CRPAT; V_{OD} = 800 mV; Pre-emphasis = 0%	< 0.14	UI p-p
Gigabit Ethernet (GIGE) Receiver Jitter Tolerance			
Total Jitter Tolerance	CJPAT Compliance Pattern; DC Gain = 0 dB	> 0.66	UI p-p
Deterministic Jitter Tolerance	CJPAT Compliance Pattern; DC Gain = 0 dB	> 0.4	UI p-p
Serial RapidIO (1.25 Gbps, 2.5 Gbps, and 3.125 Gbps) Transmitter Jitter Generation *(6)*			
Total Transmitter Jitter Generation (TJ)	CJPAT Compliance Pattern; V_{OD} = 800 mV; Pre-emphasis = 0%	< 0.35	UI p-p
Deterministic Transmitter Jitter Generation (DJ)	CJPAT Compliance Pattern; V_{OD} = 800 mV; Pre-emphasis = 0%	< 0.17	UI p-p

Figure 4–5. Receiver Input Waveforms for Differential I/O Standards

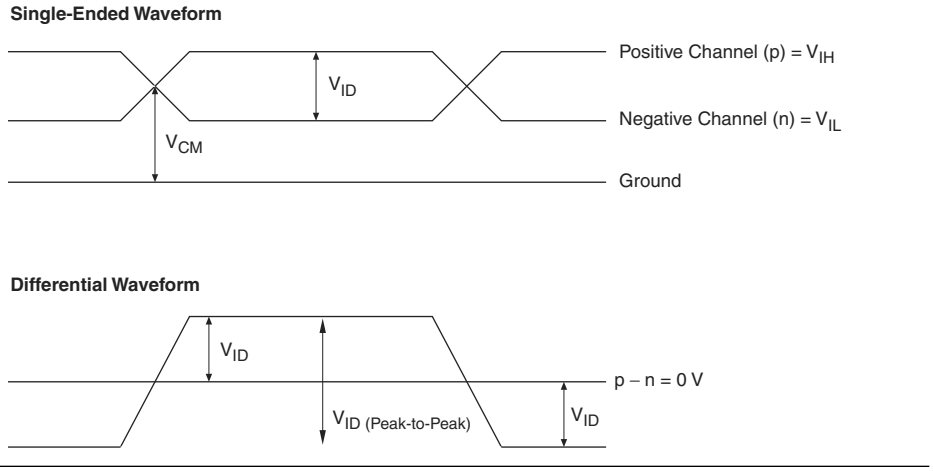


Figure 4–6. Transmitter Output Waveforms for Differential I/O Standards

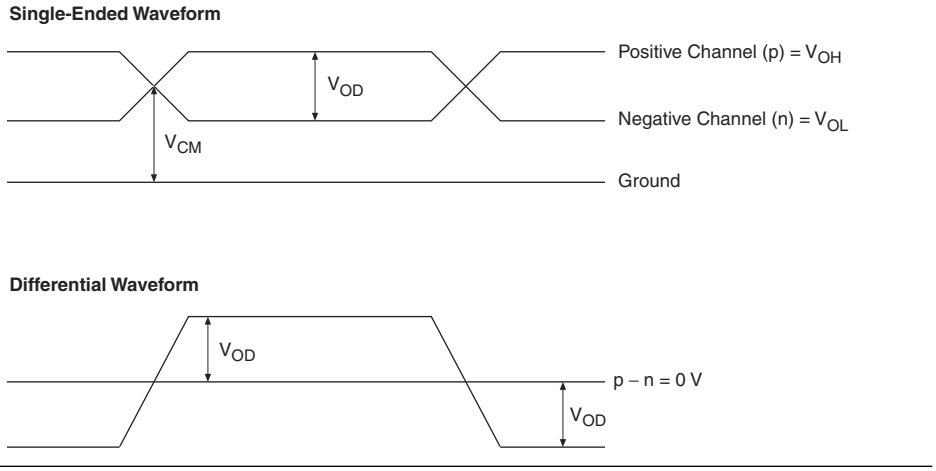


Table 4–20. 2.5-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage for left and right I/O banks (1, 2, 5, and 6)	—	2.375	2.5	2.625	V
V_{ID}	Input differential voltage swing (single-ended)	—	100	350	900	mV
V_{ICM}	Input common mode voltage	—	200	1,250	1,800	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	250	—	450	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	1.125	—	1.375	V
R_L	Receiver differential input discrete resistor (external to Arria GX devices)	—	90	100	110	Ω

Table 4–49. EP1AGX20 Column Pins Input Timing Parameters (Part 2 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
SSTL-2 CLASS II	GCLK	t_{SU}	1.075	1.075	2.372	ns
		t_H	–0.970	–0.970	–2.095	ns
	GCLK PLL	t_{SU}	2.517	2.517	5.480	ns
		t_H	–2.412	–2.412	–5.203	ns
SSTL-18 CLASS I	GCLK	t_{SU}	1.113	1.113	2.479	ns
		t_H	–1.008	–1.008	–2.202	ns
	GCLK PLL	t_{SU}	2.555	2.555	5.585	ns
		t_H	–2.450	–2.450	–5.308	ns
SSTL-18 CLASS II	GCLK	t_{SU}	1.114	1.114	2.479	ns
		t_H	–1.009	–1.009	–2.202	ns
	GCLK PLL	t_{SU}	2.556	2.556	5.587	ns
		t_H	–2.451	–2.451	–5.310	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	1.113	1.113	2.479	ns
		t_H	–1.008	–1.008	–2.202	ns
	GCLK PLL	t_{SU}	2.555	2.555	5.585	ns
		t_H	–2.450	–2.450	–5.308	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	1.114	1.114	2.479	ns
		t_H	–1.009	–1.009	–2.202	ns
	GCLK PLL	t_{SU}	2.556	2.556	5.587	ns
		t_H	–2.451	–2.451	–5.310	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.131	1.131	2.607	ns
		t_H	–1.026	–1.026	–2.330	ns
	GCLK PLL	t_{SU}	2.573	2.573	5.713	ns
		t_H	–2.468	–2.468	–5.436	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.132	1.132	2.607	ns
		t_H	–1.027	–1.027	–2.330	ns
	GCLK PLL	t_{SU}	2.574	2.574	5.715	ns
		t_H	–2.469	–2.469	–5.438	ns
3.3-V PCI	GCLK	t_{SU}	1.256	1.256	2.903	ns
		t_H	–1.151	–1.151	–2.626	ns
	GCLK PLL	t_{SU}	2.698	2.698	6.009	ns
		t_H	–2.593	–2.593	–5.732	ns
3.3-V PCI-X	GCLK	t_{SU}	1.256	1.256	2.903	ns
		t_H	–1.151	–1.151	–2.626	ns
	GCLK PLL	t_{SU}	2.698	2.698	6.009	ns
		t_H	–2.593	–2.593	–5.732	ns

Table 4–49. EP1AGX20 Column Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
LVDS	GCLK	t_{SU}	1.106	1.106	2.489	ns
		t_H	–1.001	–1.001	–2.212	ns
	GCLK PLL	t_{SU}	2.530	2.530	5.564	ns
		t_H	–2.425	–2.425	–5.287	ns

Table 4–50 describes I/O timing specifications.

Table 4–50. EP1AGX20 Row Pins output Timing Parameters (Part 1 of 2)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	2.904	2.904	6.699	ns
		GCLK PLL	t_{CO}	1.485	1.485	3.627	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.776	2.776	6.059	ns
		GCLK PLL	t_{CO}	1.357	1.357	2.987	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.720	2.720	6.022	ns
		GCLK PLL	t_{CO}	1.301	1.301	2.950	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.776	2.776	6.059	ns
		GCLK PLL	t_{CO}	1.357	1.357	2.987	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.670	2.670	5.753	ns
		GCLK PLL	t_{CO}	1.251	1.251	2.681	ns
2.5 V	4 mA	GCLK	t_{CO}	2.759	2.759	6.033	ns
		GCLK PLL	t_{CO}	1.340	1.340	2.961	ns
2.5 V	8 mA	GCLK	t_{CO}	2.656	2.656	5.775	ns
		GCLK PLL	t_{CO}	1.237	1.237	2.703	ns
2.5 V	12 mA	GCLK	t_{CO}	2.637	2.637	5.661	ns
		GCLK PLL	t_{CO}	1.218	1.218	2.589	ns
1.8 V	2 mA	GCLK	t_{CO}	2.829	2.829	7.052	ns
		GCLK PLL	t_{CO}	1.410	1.410	3.980	ns
1.8 V	4 mA	GCLK	t_{CO}	2.818	2.818	6.273	ns
		GCLK PLL	t_{CO}	1.399	1.399	3.201	ns
1.8 V	6 mA	GCLK	t_{CO}	2.707	2.707	5.972	ns
		GCLK PLL	t_{CO}	1.288	1.288	2.900	ns
1.8 V	8 mA	GCLK	t_{CO}	2.676	2.676	5.858	ns
		GCLK PLL	t_{CO}	1.257	1.257	2.786	ns
1.5 V	2 mA	GCLK	t_{CO}	2.789	2.789	6.551	ns
		GCLK PLL	t_{CO}	1.370	1.370	3.479	ns
1.5 V	4 mA	GCLK	t_{CO}	2.682	2.682	5.950	ns
		GCLK PLL	t_{CO}	1.263	1.263	2.878	ns

Table 4–54. EP1AGX35 Row Pins Input Timing Parameters (Part 2 of 2)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
SSTL-18 CLASS II	GCLK	t_{SU}	1.417	1.417	3.118	ns
		t_H	–1.312	–1.312	–2.841	ns
	GCLK PLL	t_{SU}	2.836	2.836	6.190	ns
		t_H	–2.731	–2.731	–5.913	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	1.417	1.417	3.118	ns
		t_H	–1.312	–1.312	–2.841	ns
	GCLK PLL	t_{SU}	2.836	2.836	6.190	ns
		t_H	–2.731	–2.731	–5.913	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	1.417	1.417	3.118	ns
		t_H	–1.312	–1.312	–2.841	ns
	GCLK PLL	t_{SU}	2.836	2.836	6.190	ns
		t_H	–2.731	–2.731	–5.913	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.443	1.443	3.246	ns
		t_H	–1.338	–1.338	–2.969	ns
	GCLK PLL	t_{SU}	2.862	2.862	6.318	ns
		t_H	–2.757	–2.757	–6.041	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.443	1.443	3.246	ns
		t_H	–1.338	–1.338	–2.969	ns
	GCLK PLL	t_{SU}	2.862	2.862	6.318	ns
		t_H	–2.757	–2.757	–6.041	ns
LVDS	GCLK	t_{SU}	1.341	1.341	3.088	ns
		t_H	–1.236	–1.236	–2.811	ns
	GCLK PLL	t_{SU}	2.769	2.769	6.171	ns
		t_H	–2.664	–2.664	–5.894	ns

Table 4–55 lists I/O timing specifications.

Table 4–55. EP1AGX35 Column Pins Input Timing Parameters (Part 1 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.251	1.251	2.915	ns
		t_H	–1.146	–1.146	–2.638	ns
	GCLK PLL	t_{SU}	2.693	2.693	6.021	ns
		t_H	–2.588	–2.588	–5.744	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.251	1.251	2.915	ns
		t_H	–1.146	–1.146	–2.638	ns
	GCLK PLL	t_{SU}	2.693	2.693	6.021	ns
		t_H	–2.588	–2.588	–5.744	ns

Table 4–57. EP1AGX35 Column Pins Output Timing Parameters (Part 3 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
SSTL-2 CLASS II	24 mA	GCLK	t_{CO}	2.587	2.587	5.624	ns
		GCLK PLL	t_{CO}	1.142	1.142	2.512	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.626	2.626	5.733	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.627	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.630	2.630	5.694	ns
		GCLK PLL	t_{CO}	1.185	1.185	2.582	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.609	2.609	5.675	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.563	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.614	2.614	5.673	ns
		GCLK PLL	t_{CO}	1.169	1.169	2.561	ns
SSTL-18 CLASS I	12 mA	GCLK	t_{CO}	2.608	2.608	5.659	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.547	ns
SSTL-18 CLASS II	8 mA	GCLK	t_{CO}	2.597	2.597	5.625	ns
		GCLK PLL	t_{CO}	1.152	1.152	2.513	ns
SSTL-18 CLASS II	16 mA	GCLK	t_{CO}	2.609	2.609	5.603	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.491	ns
SSTL-18 CLASS II	18 mA	GCLK	t_{CO}	2.605	2.605	5.611	ns
		GCLK PLL	t_{CO}	1.160	1.160	2.499	ns
SSTL-18 CLASS II	20 mA	GCLK	t_{CO}	2.605	2.605	5.609	ns
		GCLK PLL	t_{CO}	1.160	1.160	2.497	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.629	2.629	5.664	ns
		GCLK PLL	t_{CO}	1.187	1.187	2.558	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.634	2.634	5.649	ns
		GCLK PLL	t_{CO}	1.189	1.189	2.537	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.612	2.612	5.638	ns
		GCLK PLL	t_{CO}	1.167	1.167	2.526	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.616	2.616	5.644	ns
		GCLK PLL	t_{CO}	1.171	1.171	2.532	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.608	2.608	5.637	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.525	ns
1.8-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.591	2.591	5.401	ns
		GCLK PLL	t_{CO}	1.146	1.146	2.289	ns
1.8-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.593	2.593	5.412	ns
		GCLK PLL	t_{CO}	1.148	1.148	2.300	ns
1.8-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.593	2.593	5.421	ns
		GCLK PLL	t_{CO}	1.148	1.148	2.309	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.629	2.629	5.663	ns
		GCLK PLL	t_{CO}	1.187	1.187	2.557	ns

Table 4–57. EP1AGX35 Column Pins Output Timing Parameters (Part 4 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.633	2.633	5.641	ns
		GCLK PLL	t_{CO}	1.188	1.188	2.529	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.615	2.615	5.643	ns
		GCLK PLL	t_{CO}	1.170	1.170	2.531	ns
1.5-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.615	2.615	5.645	ns
		GCLK PLL	t_{CO}	1.170	1.170	2.533	ns
1.5-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.609	2.609	5.643	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.531	ns
1.5-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.596	2.596	5.455	ns
		GCLK PLL	t_{CO}	1.151	1.151	2.343	ns
1.5-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.599	2.599	5.465	ns
		GCLK PLL	t_{CO}	1.154	1.154	2.353	ns
1.5-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.601	2.601	5.478	ns
		GCLK PLL	t_{CO}	1.156	1.156	2.366	ns
3.3-V PCI	—	GCLK	t_{CO}	2.755	2.755	5.791	ns
		GCLK PLL	t_{CO}	1.313	1.313	2.685	ns
3.3-V PCI-X	—	GCLK	t_{CO}	2.755	2.755	5.791	ns
		GCLK PLL	t_{CO}	1.313	1.313	2.685	ns
LVDS	—	GCLK	t_{CO}	3.621	3.621	6.969	ns
		GCLK PLL	t_{CO}	2.190	2.190	3.880	ns

Table 4–58 through Table 4–59 list EP1AGX35 regional clock (RCLK) adder values that should be added to GCLK values. These adder values are used to determine I/O timing when the I/O pin is driven using the regional clock. This applies for all I/O standards supported by Arria GX with general purpose I/O pins.

Table 4–58 describes row pin delay adders when using the regional clock in Arria GX devices.

Table 4–58. EP1AGX35 Row Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.126	0.126	0.281	ns
RCLK PLL input adder	0.011	0.011	0.018	ns
RCLK output adder	–0.126	–0.126	–0.281	ns
RCLK PLL output adder	–0.011	–0.011	–0.018	ns

Table 4–72. EP1AGX90 Row Pins Input Timing Parameters (Part 2 of 2)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
1.8-V HSTL CLASS I	GCLK	t_{SU}	1.159	1.159	2.447	ns
		t_H	–1.054	–1.054	–2.170	ns
	GCLK PLL	t_{SU}	3.212	3.212	6.565	ns
		t_H	–3.107	–3.107	–6.288	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	1.157	1.157	2.441	ns
		t_H	–1.052	–1.052	–2.164	ns
	GCLK PLL	t_{SU}	3.235	3.235	6.597	ns
		t_H	–3.130	–3.130	–6.320	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.185	1.185	2.575	ns
		t_H	–1.080	–1.080	–2.298	ns
	GCLK PLL	t_{SU}	3.238	3.238	6.693	ns
		t_H	–3.133	–3.133	–6.416	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.183	1.183	2.569	ns
		t_H	–1.078	–1.078	–2.292	ns
	GCLK PLL	t_{SU}	3.261	3.261	6.725	ns
		t_H	–3.156	–3.156	–6.448	ns
LVDS	GCLK	t_{SU}	1.098	1.098	2.439	ns
		t_H	–0.993	–0.993	–2.162	ns
	GCLK PLL	t_{SU}	3.160	3.160	6.566	ns
		t_H	–3.055	–3.055	–6.289	ns

Table 4–73 lists I/O timing specifications.

Table 4–73. EP1AGX90 Column Pins Input Timing Parameters (Part 1 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.018	1.018	2.290	ns
		t_H	–0.913	–0.913	–2.013	ns
	GCLK PLL	t_{SU}	3.082	3.082	6.425	ns
		t_H	–2.977	–2.977	–6.148	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.018	1.018	2.290	ns
		t_H	–0.913	–0.913	–2.013	ns
	GCLK PLL	t_{SU}	3.082	3.082	6.425	ns
		t_H	–2.977	–2.977	–6.148	ns
2.5 V	GCLK	t_{SU}	1.028	1.028	2.272	ns
		t_H	–0.923	–0.923	–1.995	ns
	GCLK PLL	t_{SU}	3.092	3.092	6.407	ns
		t_H	–2.987	–2.987	–6.130	ns

Table 4–104. Arria GX Maximum Input Clock Rate for Dedicated Clock Pins (Part 2 of 2)

I/O Standards	–6 Speed Grade	Units
3.3-V PCI-X	373	MHz
SSTL-18 CLASS I	467	MHz
SSTL-18 CLASS II	467	MHz
1.8-V HSTL CLASS I	467	MHz
1.8-V HSTL CLASS II	467	MHz
1.5-V HSTL CLASS I	467	MHz
1.5-V HSTL CLASS II	467	MHz
1.2-V HSTL	233	MHz
DIFFERENTAL SSTL-2	467	MHz
DIFFERENTIAL 2.5-V SSTL CLASS II	467	MHz
DIFFERENTIAL 1.8-V SSTL CLASS I	467	MHz
DIFFERENTIAL 1.8-V SSTL CLASS II	467	MHz
DIFFERENTIAL 1.8-V HSTL CLASS I	467	MHz
DIFFERENTIAL 1.8-V HSTL CLASS II	467	MHz
DIFFERENTIAL 1.5-V HSTL CLASS I	467	MHz
DIFFERENTIAL 1.5-V HSTL CLASS II	467	MHz
DIFFERENTIAL 1.2-V HSTL	233	MHz
LVDS	640	MHz
LVDS *(1)*	373	MHz

Note to Table 4–104:

(1) This set of numbers refers to the VIO dedicated input clock pins.

Table 4–105 shows the maximum output clock toggle rates for Arria GX device column I/O pins.

Table 4–105. Arria GX Maximum Output Toggle Rate for Column I/O Pins (Part 1 of 3)

I/O Standards	Drive Strength	–6 Speed Grade	Units
3.3-V LVTTL	4 mA	196	MHz
	8 mA	303	MHz
	12 mA	393	MHz
	16 mA	486	MHz
	20 mA	570	MHz
	24 mA	626	MHz

To calculate the DCD as a percentage:

(T/2 – DCD) / T = (3,745 ps/2 – 125 ps) / 3,745 ps = 46.66% (for low boundary)

(T/2 + DCD) / T = (3,745 ps/2 + 125 ps) / 3,745 ps = 53.33% (for high boundary)

Therefore, the DCD percentage for the output clock at 267 MHz is from 46.66% to 53.33%.

Table 4–109. Maximum DCD for Non-DDIO Output on Column I/O Pins

Column I/O Output Standard I/O Standard	Maximum DCD (ps) for Non-DDIO Output	Units
	–6 Speed Grade	
3.3-V LVTTL	220	ps
3.3-V LVCMOS	175	ps
2.5 V	155	ps
1.8 V	110	ps
1.5-V LVCMOS	215	ps
SSTL-2 Class I	135	ps
SSTL-2 Class II	130	ps
SSTL-18 Class I	115	ps
SSTL-18 Class II	100	ps
1.8-V HSTL Class I	110	ps
1.8-V HSTL Class II	110	ps
1.5-V HSTL Class I	115	ps
1.5-V HSTL Class II	80	ps
1.2-V HSTL-12	200	ps
LVPECL	80	ps

Table 4–110. Maximum DCD for DDIO Output on Row I/O Pins Without PLL in the Clock Path *Note (1)*

Maximum DCD (ps) for Row DDIO Output I/O Standard	Input I/O Standard (No PLL in the Clock Path)					Units
	TTL/CMOS		SSTL-2	SSTL/HSTL	LVDS	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	3.3V	
3.3-V LVTTL	440	495	170	160	105	ps
3.3-V LVCMOS	390	450	120	110	75	ps
2.5 V	375	430	105	95	90	ps
1.8 V	325	385	90	100	135	ps
1.5-V LVCMOS	430	490	160	155	100	ps
SSTL-2 Class I	355	410	85	75	85	ps
SSTL-2 Class II	350	405	80	70	90	ps
SSTL-18 Class I	335	390	65	65	105	ps
1.8-V HSTL Class I	330	385	60	70	110	ps
1.5-V HSTL Class I	330	390	60	70	105	ps

Table 4–121. DQS Bus Clock Skew Adder Specifications ($t_{DQS\_CLOCK\_SKEW\_ADDER}$)

Mode	DQS Clock Skew Adder (ps)
4 DQ per DQS	40
9 DQ per DQS	70
18 DQ per DQS	75
36 DQ per DQS	95

Table 4–122. DQS Phase Offset Delay Per Stage (ps) *Note (1), (2), (3)*

Speed Grade	Positive Offset		Negative Offset	
	Min	Max	Min	Max
–6	10	16	8	12

Notes to Table 4–122:

(1) The delay settings are linear.
(2) The valid settings for phase offset are –32 to +31.
(3) The typical value equals the average of the minimum and maximum values.

JTAG Timing Specifications

Figure 4–13 shows the timing requirements for the JTAG signals

Figure 4–13. Arria GX JTAG Waveforms.