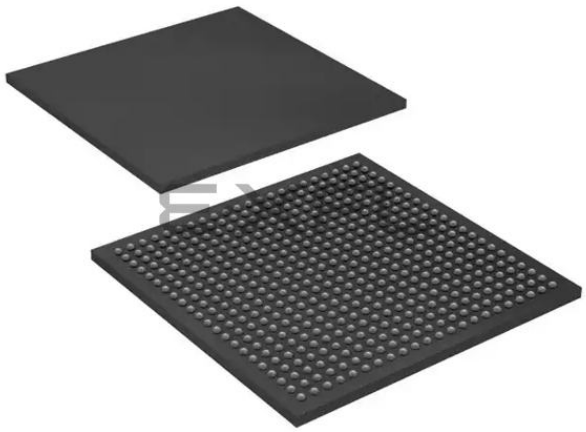

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2508
Number of Logic Elements/Cells	50160
Total RAM Bits	2475072
Number of I/O	229
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1agx50cf484i6n

AGX51002-2.0

Transceivers

Arria® GX devices incorporate up to 12 high-speed serial transceiver channels that build on the success of the Stratix® II GX device family. Arria GX transceivers are structured into full-duplex (transmitter and receiver) four-channel groups called transceiver blocks located on the right side of the device. You can configure the transceiver blocks to support the following serial connectivity protocols (functional modes):

- PCI Express (PIPE)
- Gigabit Ethernet (GIGE)
- XAUI
- Basic (600 Mbps to 3.125 Gbps)
- SDI (HD, 3G)
- Serial RapidIO (1.25 Gbps, 2.5 Gbps, 3.125 Gbps)

Transceivers within each block are independent and have their own set of dividers. Therefore, each transceiver can operate at different frequencies. Each block can select from two reference clocks to provide two clock domains that each transceiver can select from.

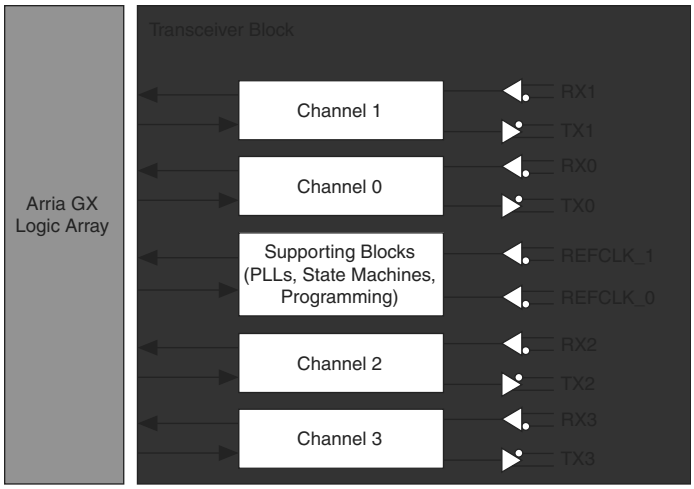
Table 2–1 lists the number of transceiver channels for each member of the Arria GX family.

Table 2–1. Arria GX Transceiver Channels

Device	Number of Transceiver Channels
EP1AGX20C	4
EP1AGX35C	4
EP1AGX35D	8
EP1AGX50C	4
EP1AGX50D	8
EP1AGX60C	4
EP1AGX60D	8
EP1AGX60E	12
EP1AGX90E	12

Figure 2–1 shows a high-level diagram of the transceiver block architecture divided into four channels.

Figure 2–1. Transceiver Block

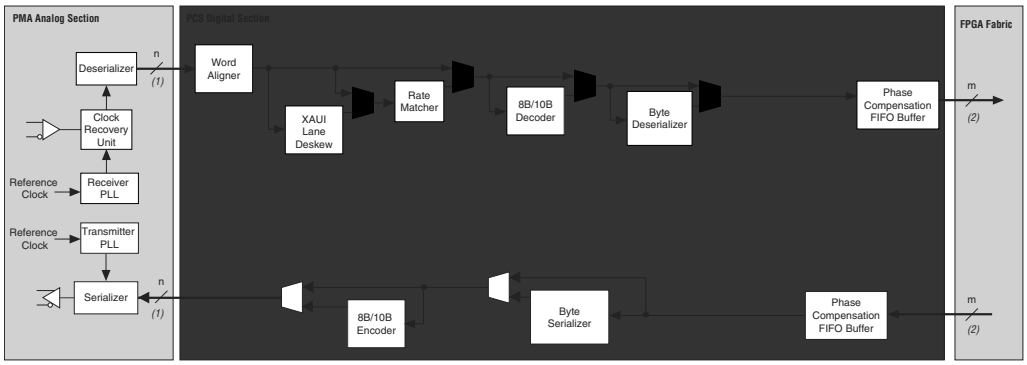


Each transceiver block has:

- Four transceiver channels with dedicated physical coding sublayer (PCS) and physical media attachment (PMA) circuitry
- One transmitter PLL that takes in a reference clock and generates high-speed serial clock depending on the functional mode
- Four receiver PLLs and clock recovery unit (CRU) to recover clock and data from the received serial data stream
- State machines and other logic to implement special features required to support each protocol

Figure 2–2 shows functional blocks that make up a transceiver channel.

Figure 2–2. Arria GX Transceiver Channel Block Diagram



Notes to Figure 2–2:

(1) "n" represents the number of bits in each word that must be serialized by the transmitter portion of the PMA. n = 8 or 10.

(2) "m" represents the number of bits in the word that passes between the FPGA logic and the PCS portion of the transceiver. m = 8, 10, 16, or 20.

Each transceiver channel is full-duplex and consists of a transmitter channel and a receiver channel.

The transmitter channel contains the following sub-blocks:

- Transmitter phase compensation first-in first-out (FIFO) buffer
- Byte serializer (optional)
- 8B/10B encoder (optional)
- Serializer (parallel-to-serial converter)
- Transmitter differential output buffer

The receiver channel contains the following:

- Receiver differential input buffer
- Receiver lock detector and run length checker
- CRU
- Deserializer
- Pattern detector
- Word aligner
- Lane deskew
- Rate matcher (optional)
- 8B/10B decoder (optional)
- Byte deserializer (optional)
- Receiver phase compensation FIFO buffer

You can configure the transceiver channels to the desired functional modes using the ALT2GXB MegaCore instance in the Quartus® II MegaWizard™ Plug-in Manager for the Arria GX device family. Depending on the selected functional mode, the Quartus II software automatically configures the transceiver channels to employ a subset of the sub-blocks listed above.

Transmitter Path

This section describes the data path through the Arria GX transmitter. The sub-blocks are described in order from the PLD-transmitter parallel interface to the serial transmitter buffer.

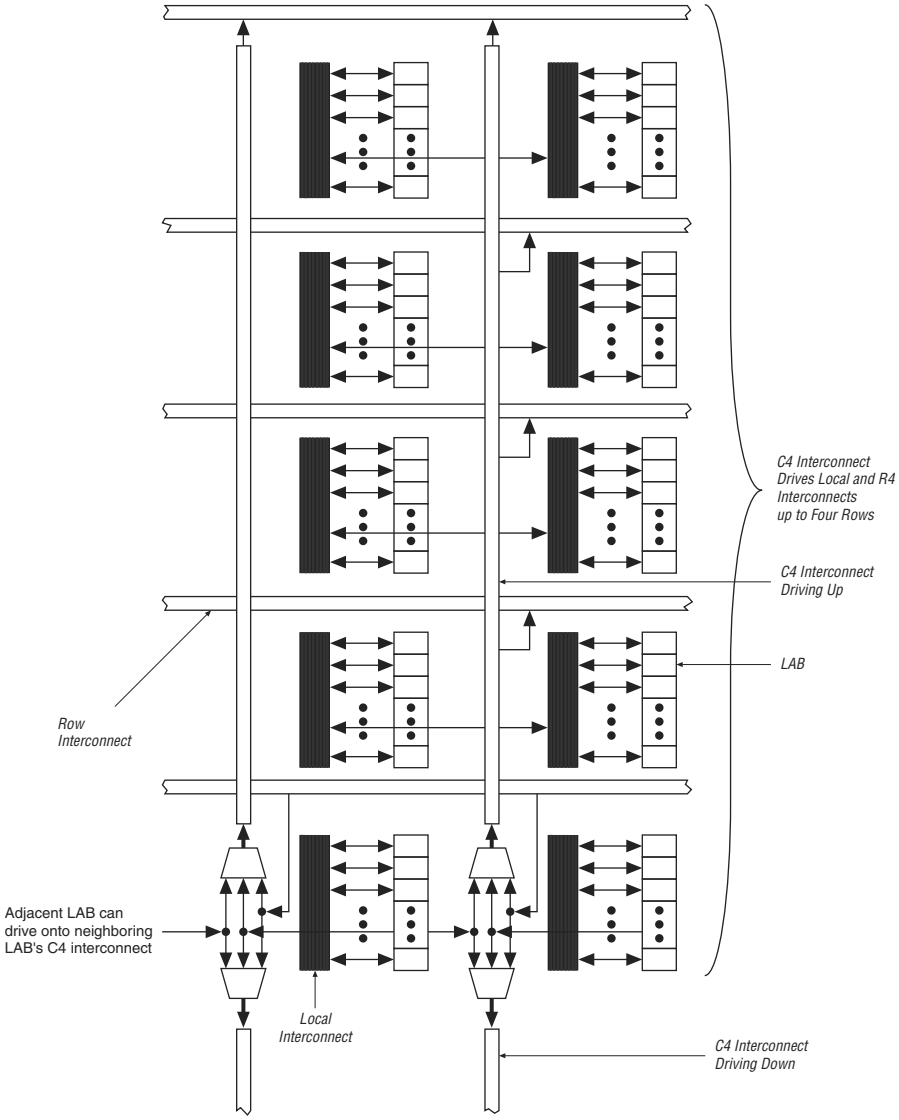
Clock Multiplier Unit

Each transceiver block has a clock multiplier unit (CMU) that takes in a reference clock and synthesizes two clocks: a high-speed serial clock to serialize the data and a low-speed parallel clock to clock the transmitter digital logic (PCS).

The CMU is further divided into three sub-blocks:

- One transmitter PLL
- One central clock divider block
- Four local clock divider blocks (one per channel)

Figure 2–41. C4 Interconnect Connections *(Note 1)*

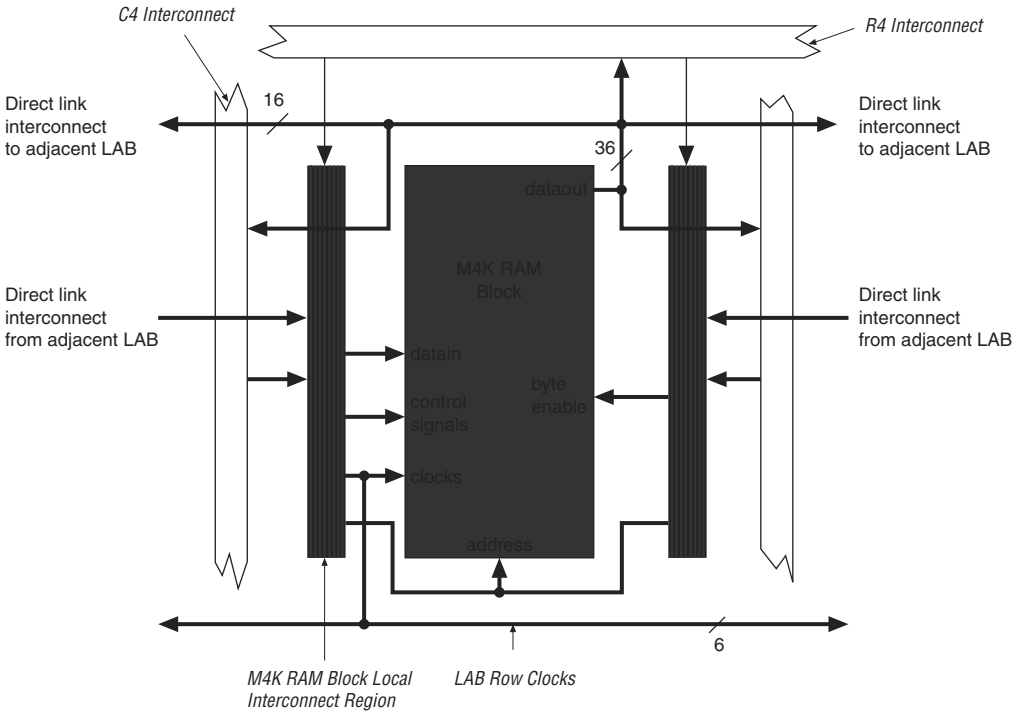


Note to Figure 2–41:

(1) Each C4 interconnect can drive either up or down four rows.

C16 column interconnects span a length of 16 LABs and provide the fastest resource for long column connections between LABs, TriMatrix memory blocks, DSP blocks, and IOEs. C16 interconnects can cross M-RAM blocks and also drive to row and column interconnects at every fourth LAB. C16 interconnects drive LAB local interconnects via C4 and R4 interconnects and do not drive LAB local interconnects directly. All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (that is, TriMatrix memory and DSP blocks) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB. All blocks are fed by the row LAB clocks, `labclk[5..0]`.

Figure 2–45. M4K RAM Block LAB Row Interface



M-RAM Block

The largest TriMatrix memory block, the M-RAM block, is useful for applications where a large volume of data must be stored on-chip. Each block contains 589,824 RAM bits (including parity bits). The M-RAM block can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO

You cannot use an initialization file to initialize the contents of a M-RAM block. All M-RAM block contents power up to an undefined value. Only synchronous operation is supported in the M-RAM block, so all inputs are registered. Output registers can be bypassed.

Similar to all RAM blocks, M-RAM blocks can have different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M-RAM block registers (`renwe`, `address`, byte enable, `datain`, and output registers). You can bypass the output register. The six `labclk` signals or local interconnect can drive the control signals for the A and B ports of the M-RAM block. ALMs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, `clr_b`, `clocken_a`, and `clocken_b` signals, as shown in Figure 2–46.

Table 2–15. DSP Block Signal Sources and Destinations

LAB Row at Interface	Control Signals Generated	Data Inputs	Data Outputs
0	clock0 aclr0 ena0 mult01_saturate addnsub1_round/ accum_round addnsub1 signa sourcea sourceb	A1[17..0] B1[17..0]	OA[17..0] OB[17..0]
1	clock1 aclr1 ena1 accum_saturate mult01_round accum_sload sourcea sourceb mode0	A2[17..0] B2[17..0]	OC[17..0] OD[17..0]
2	clock2 aclr2 ena2 mult23_saturate addnsub3_round/ accum_round addnsub3 sign_b sourcea sourceb	A3[17..0] B3[17..0]	OE[17..0] OF[17..0]
3	clock3 aclr3 ena3 accum_saturate mult23_round accum_sload sourcea sourceb mode1	A4[17..0] B4[17..0]	OG[17..0] OH[17..0]

Enhanced and Fast PLLs

Arria GX devices provide robust clock management and synthesis using up to four enhanced PLLs and four fast PLLs. These PLLs increase performance and provide advanced clock interfacing and clock frequency synthesis. With features such as clock switchover, spread spectrum clocking, reconfigurable bandwidth, phase control, and reconfigurable phase shifting, the Arria GX device's enhanced PLLs provide you with complete control of your clocks and system timing. The fast PLLs provide general purpose clocking with multiplication and phase shifting as well as high-speed outputs for high-speed differential I/O support. Enhanced and fast PLLs work together with the Arria GX high-speed I/O and advanced clock architecture to provide significant improvements in system performance and bandwidth.

The Quartus II software enables the PLLs and their features without requiring any external devices. Table 2–17 lists the PLLs available for each Arria GX device and their type.

Table 2–17. Arria GX Device PLL Availability *(Note 1)*, *(2)*

Device	Fast PLLs								Enhanced PLLs			
	1	**2**	**3** *(3)*	**4** *(3)*	**7**	**8**	**9** *(3)*	**10** *(3)*	**5**	**6**	**11**	**12**
EP1AGX20	✓	✓	—	—	—	—	—	—	✓	✓	—	—
EP1AGX35	✓	✓	—	—	—	—	—	—	✓	✓	—	—
EP1AGX50 *(4)*	✓	✓	—	—	✓	✓	—	—	✓	✓	✓	✓
EP1AGX60 *(5)*	✓	✓	—	—	✓	✓	—	—	✓	✓	✓	✓
EP1AGX90	✓	✓	—	—	✓	✓	—	—	✓	✓	✓	✓

Notes to Table 2–17:

(1) The global or regional clocks in a fast PLL's transceiver block can drive the fast PLL input. A pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

(2) EP1AGX20C, EP1AGX35C/D, EP1AGX50C and EP1AGX60C/D devices only have two fast PLLs (PLLs 1 and 2), but the connectivity from these two PLLs to the global and regional clock networks remains the same as shown in this table.

(3) PLLs 3, 4, 9, and 10 are not available in Arria GX devices.

(4) 4 or 8 PLLs are available depending on C or D device and the package option.

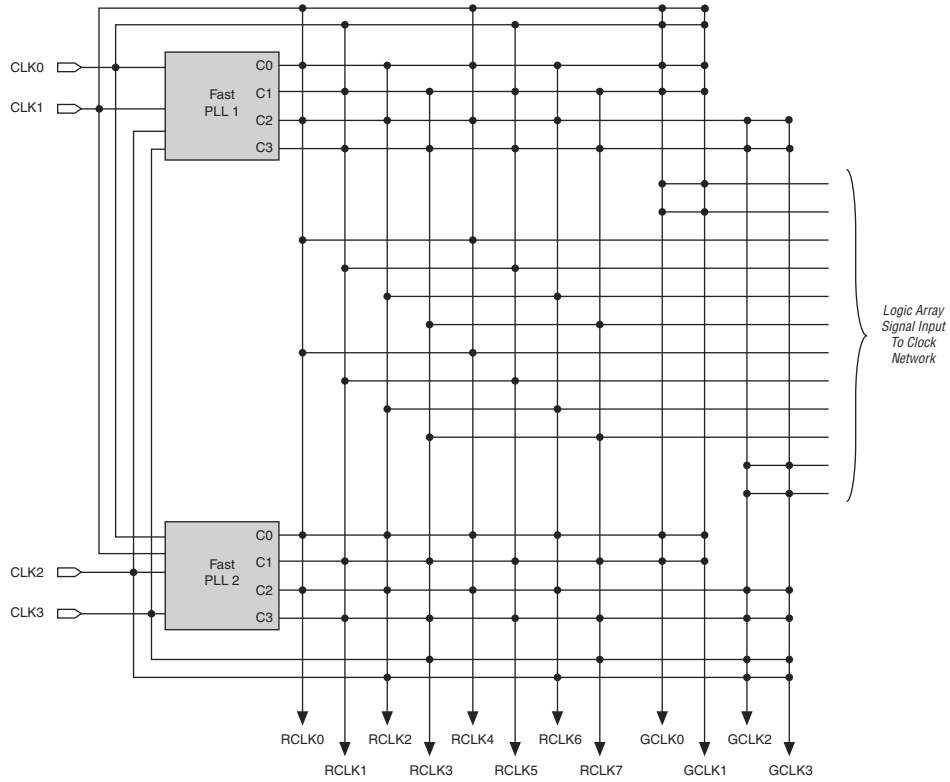
(5) 4or 8 PLLs are available depending on C, D, or E device option.

Table 2–18 lists the enhanced PLL and fast PLL features in Arria GX devices.

Table 2–18. Arria GX PLL Features (Part 1 of 2)

Feature	Enhanced PLL	Fast PLL
Clock multiplication and division	*m*/(*n* × post-scale counter) *(1)*	*m*/(*n* × post-scale counter) *(2)*
Phase shift	Down to 125-ps increments *(3)*, *(4)*	Down to 125-ps increments *(3)*, *(4)*
Clock switchover	✓	✓ *(5)*
PLL reconfiguration	✓	✓
Reconfigurable bandwidth	✓	✓
Spread spectrum clocking	✓	—
Programmable duty cycle	✓	✓
Number of internal clock outputs	6	4
Number of external clock outputs	Three differential/six single-ended	*(6)*

Figure 2–62. Global and Regional Clock Connections from Center Clock Pins and Fast PLL Outputs *(Note 1)*



Note to Figure 2–62:

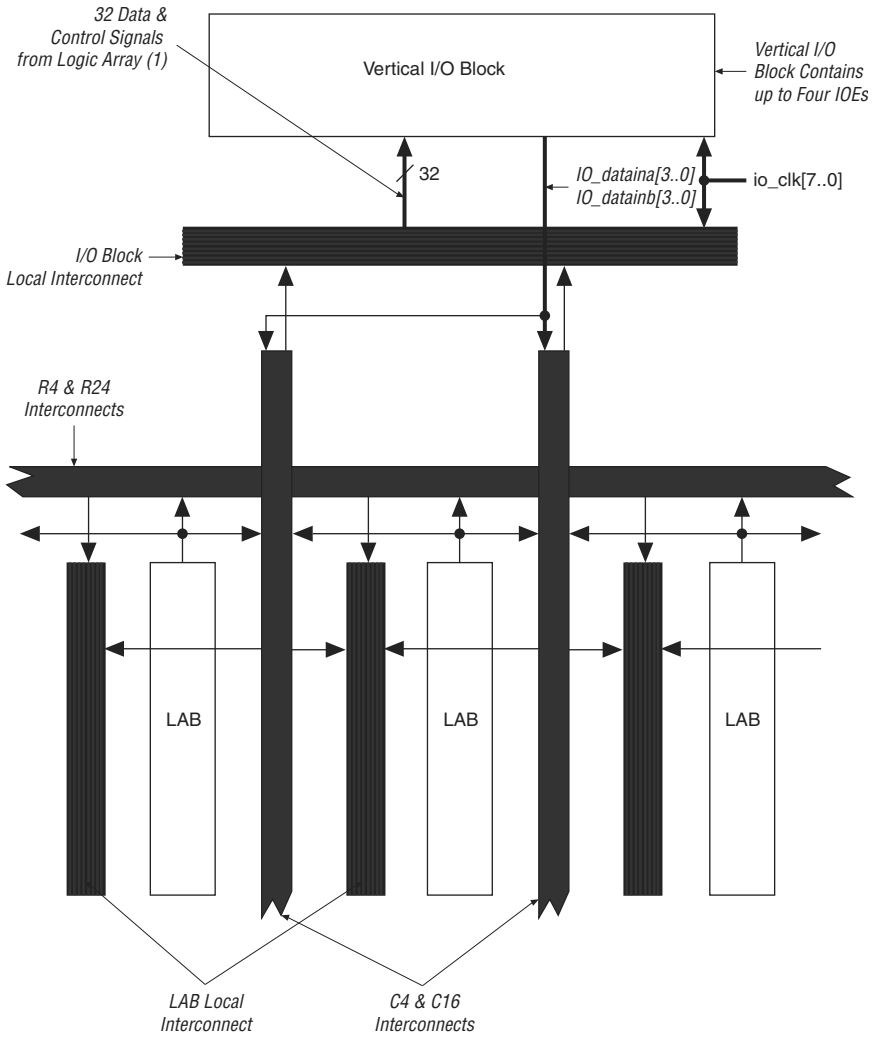
(1) The global or regional clocks in a fast PLL's quadrant can drive the fast PLL input. A dedicated clock input pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

Table 2–20. Global and Regional Clock Connections from Top Clock Pins and Enhanced PLL Outputs

Top Side Global and Regional Clock Network Connectivity	DLLCLK	CLK12	CLK13	CLK14	CLK15	RCLK24	RCLK25	RCLK26	RCLK27	RCLK28	RCLK29	RCLK30	RCLK31
Clock pins													
CLK12p	✓	✓	✓	—	—	✓	—	—	—	✓	—	—	—
CLK13p	✓	✓	✓	—	—	—	✓	—	—	—	✓	—	—
CLK14p	✓	—	—	✓	✓	—	—	✓	—	—	—	✓	—
CLK15p	✓	—	—	✓	✓	—	—	—	✓	—	—	—	✓
CLK12n	—	✓	—	—	—	✓	—	—	—	✓	—	—	—
CLK13n	—	—	✓	—	—	—	✓	—	—	—	✓	—	—
CLK14n	—	—	—	✓	—	—	—	✓	—	—	—	✓	—
CLK15n	—	—	—	—	✓	—	—	—	✓	—	—	—	✓
Drivers from internal logic													
GCLKDRV0	—	✓	—	—	—	—	—	—	—	—	—	—	—
GCLKDRV1	—	—	✓	—	—	—	—	—	—	—	—	—	—
GCLKDRV2	—	—	—	✓	—	—	—	—	—	—	—	—	—
GCLKDRV3	—	—	—	—	✓	—	—	—	—	—	—	—	—
RCLKDRV0	—	—	—	—	—	✓	—	—	—	✓	—	—	—
RCLKDRV1	—	—	—	—	—	—	✓	—	—	—	✓	—	—
RCLKDRV2	—	—	—	—	—	—	—	✓	—	—	—	✓	—
RCLKDRV3	—	—	—	—	—	—	—	—	✓	—	—	—	✓
RCLKDRV4	—	—	—	—	—	✓	—	—	—	✓	—	—	—
RCLKDRV5	—	—	—	—	—	—	✓	—	—	—	✓	—	—
RCLKDRV6	—	—	—	—	—	—	—	✓	—	—	—	✓	—
RCLKDRV7	—	—	—	—	—	—	—	—	✓	—	—	—	✓
Enhanced PLL5 outputs													
c0	✓	✓	✓	—	—	✓	—	—	—	✓	—	—	—
c1	✓	✓	✓	—	—	—	✓	—	—	—	✓	—	—
c2	✓	—	—	✓	✓	—	—	✓	—	—	—	✓	—
c3	✓	—	—	✓	✓	—	—	—	✓	—	—	—	✓
c4	✓	—	—	—	—	✓	—	✓	—	✓	—	✓	—
c5	✓	—	—	—	—	—	✓	—	✓	—	✓	—	✓
Enhanced PLL 11 outputs													
c0	—	✓	✓	—	—	✓	—	—	—	✓	—	—	—
c1	—	✓	✓	—	—	—	✓	—	—	—	✓	—	—
c2	—	—	—	✓	✓	—	—	✓	—	—	—	✓	—
c3	—	—	—	✓	✓	—	—	—	✓	—	—	—	✓
c4	—	—	—	—	—	✓	—	✓	—	✓	—	✓	—
c5	—	—	—	—	—	—	✓	—	✓	—	✓	—	✓

Figure 2–69 shows how a column I/O block connects to the logic array.

Figure 2–69. Column I/O Block Connection to the Interconnect



Note to Figure 2–69:

(1) The 32 data and control signals consist of eight data out lines: four lines each for DDR applications `io_dataouta[3..0]` and `io_dataoutb[3..0]`, four output enables `io_oe[3..0]`, four input clock enables `io_ce_in[3..0]`, four output clock enables `io_ce_out[3..0]`, four clocks `io_clk[3..0]`, four asynchronous clear and preset signals `io_aclr/apreset[3..0]`, and four synchronous clear and preset signals `io_sclr/spreset[3..0]`.

There are 32 control and data signals that feed each row or column I/O block. These control and data signals are driven from the logic array. The row or column IOE clocks, `io_clk[7..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. I/O clocks are generated from global or regional clocks (refer to "PLLs and Clock Networks" on page 2–66).

Table 4–1. Arria GX Device Absolute Maximum Ratings *(Note 1), (2), (3)* (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Units
T_J	Junction temperature	BGA packages under bias	–55	125	C

Notes to Table 4–1:

(1) For more information about operating requirements for Altera® devices, refer to the *Arria GX Device Family Data Sheet* chapter.

(2) Conditions beyond those listed in Table 4–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.

(3) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.

(4) During transitions, the inputs may overshoot to the voltage shown in Table 4–2 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 4–2. Maximum Duty Cycles in Voltage Transitions *(Note 1)*

Symbol	Parameter	Condition	Maximum Duty Cycles (%)
V_I	Maximum duty cycles in voltage transitions	V_I = 4.0 V	100
		V_I = 4.1 V	90
		V_I = 4.2 V	50
		V_I = 4.3 V	30
		V_I = 4.4 V	17
		V_I = 4.5 V	10

Note to Table 4–2:

(1) During transition, the inputs may overshoot to the voltages shown based on the input duty cycle. The DC case is equivalent to 100% duty cycle.

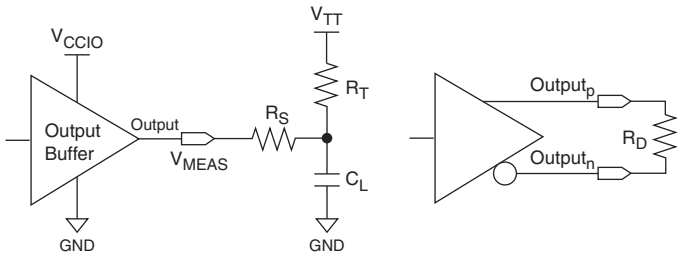
Recommended Operating Conditions

Table 4–3 lists the recommended operating conditions for the Arria GX device family.

Table 4–3. Arria GX Device Recommended Operating Conditions (Part 1 of 2) *(Note 1)* (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCINT}	Supply voltage for internal logic and input buffers	Rise time ≤ 100 ms *(3)*	1.15	1.25	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	Rise time ≤ 100 ms *(3), (6)*	3.135 (3.00)	3.465 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	Rise time ≤ 100 ms *(3)*	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	Rise time ≤ 100 ms *(3)*	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	Rise time ≤ 100 ms *(3)*	1.425	1.575	V
	Supply voltage for output buffers, 1.2-V operation	Rise time ≤ 100 ms *(3)*	1.15	1.25	V
V_{CCPD}	Supply voltage for pre-drivers as well as configuration and JTAG I/O buffers.	100 µs ≤ rise time ≤ 100 ms *(4)*	3.135	3.465	V
V_I	Input voltage (refer to Table 4–2)	*(2), (5)*	–0.5	4.0	V
V_O	Output voltage	—	0	V_{CCIO}	V

Figure 4–7. Output Delay Timing Reporting Setup Modeled by Quartus II



Notes to Figure 4–7:

(1) Output pin timing is reported at the output pin of the FPGA device. Additional delays for loading and board trace delay need to be accounted for with IBIS model simulations.

(2) V_{CCPD} is 3.085 V unless otherwise specified.

(3) V_{CCINT} is 1.12 V unless otherwise specified.

Table 4–44. Output Timing Measurement Methodology for Output Pins *(Note 1), (2), (3)*

I/O Standard	Loading and Termination						Measurement Point
	R_S (Ω)	R_D (Ω)	R_T (Ω)	V_{CCIO} (V)	V_{TT} (V)	C_L (pF)	V_{MEAS} (V)
LVTTL *(4)*	—	—	—	3.135	—	0	1.5675
LVCMOS *(4)*	—	—	—	3.135	—	0	1.5675
2.5 V *(4)*	—	—	—	2.375	—	0	1.1875
1.8 V *(4)*	—	—	—	1.710	—	0	0.855
1.5 V *(4)*	—	—	—	1.425	—	0	0.7125
PCI *(5)*	—	—	—	2.970	—	10	1.485
PCI-X *(5)*	—	—	—	2.970	—	10	1.485
SSTL-2 Class I	25	—	50	2.325	1.123	0	1.1625
SSTL-2 Class II	25	—	25	2.325	1.123	0	1.1625
SSTL-18 Class I	25	—	50	1.660	0.790	0	0.83
SSTL-18 Class II	25	—	25	1.660	0.790	0	0.83
1.8-V HSTL Class I	—	—	50	1.660	0.790	0	0.83
1.8-V HSTL Class II	—	—	25	1.660	0.790	0	0.83
1.5-V HSTL Class I	—	—	50	1.375	0.648	0	0.6875
1.5-V HSTL Class II	—	—	25	1.375	0.648	0	0.6875
1.2-V HSTL with OCT	—	—	—	1.140	—	0	0.570
Differential SSTL-2 Class I	25	—	50	2.325	1.123	0	1.1625
Differential SSTL-2 Class II	25	—	25	2.325	1.123	0	1.1625
Differential SSTL-18 Class I	50	—	50	1.660	0.790	0	0.83
Differential SSTL-18 Class II	25	—	25	1.660	0.790	0	0.83
1.5-V differential HSTL Class I	—	—	50	1.375	0.648	0	0.6875
1.5-V differential HSTL Class II	—	—	25	1.375	0.648	0	0.6875
1.8-V differential HSTL Class I	—	—	50	1.660	0.790	0	0.83

Table 4–48. EP1AGX20 Row Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.117	0.117	0.273	ns
RCLK PLL input adder	0.011	0.011	0.019	ns
RCLK output adder	–0.117	–0.117	–0.273	ns
RCLK PLL output adder	–0.011	–0.011	–0.019	ns

Table 4–49 describes I/O timing specifications.

Table 4–49. EP1AGX20 Column Pins Input Timing Parameters (Part 1 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.251	1.251	2.915	ns
		t_H	–1.146	–1.146	–2.638	ns
	GCLK PLL	t_{SU}	2.693	2.693	6.021	ns
		t_H	–2.588	–2.588	–5.744	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.251	1.251	2.915	ns
		t_H	–1.146	–1.146	–2.638	ns
	GCLK PLL	t_{SU}	2.693	2.693	6.021	ns
		t_H	–2.588	–2.588	–5.744	ns
2.5 V	GCLK	t_{SU}	1.261	1.261	2.897	ns
		t_H	–1.156	–1.156	–2.620	ns
	GCLK PLL	t_{SU}	2.703	2.703	6.003	ns
		t_H	–2.598	–2.598	–5.726	ns
1.8 V	GCLK	t_{SU}	1.327	1.327	3.107	ns
		t_H	–1.222	–1.222	–2.830	ns
	GCLK PLL	t_{SU}	2.769	2.769	6.213	ns
		t_H	–2.664	–2.664	–5.936	ns
1.5 V	GCLK	t_{SU}	1.330	1.330	3.200	ns
		t_H	–1.225	–1.225	–2.923	ns
	GCLK PLL	t_{SU}	2.772	2.772	6.306	ns
		t_H	–2.667	–2.667	–6.029	ns
SSTL-2 CLASS I	GCLK	t_{SU}	1.075	1.075	2.372	ns
		t_H	–0.970	–0.970	–2.095	ns
	GCLK PLL	t_{SU}	2.517	2.517	5.480	ns
		t_H	–2.412	–2.412	–5.203	ns

Table 4–51. EP1AGX20 Column Pins Output Timing Parameters (Part 4 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V PCI	—	GCLK	t_{CO}	2.755	2.755	5.791	ns
		GCLK PLL	t_{CO}	1.313	1.313	2.685	ns
3.3-V PCI-X	—	GCLK	t_{CO}	2.755	2.755	5.791	ns
		GCLK PLL	t_{CO}	1.313	1.313	2.685	ns
LVDS	—	GCLK	t_{CO}	3.621	3.621	6.969	ns
		GCLK PLL	t_{CO}	2.190	2.190	3.880	ns

Table 4–52 through Table 4–53 list EP1AGX20 regional clock (RCLK) adder values that should be added to GCLK values. These adder values are used to determine I/O timing when the I/O pin is driven using the regional clock. This applies for all I/O standards supported by Arria GX with general purpose I/O pins.

Table 4–52 describes row pin delay adders when using the regional clock in Arria GX devices.

Table 4–52. EP1AGX20 Row Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.117	0.117	0.273	ns
RCLK PLL input adder	0.011	0.011	0.019	ns
RCLK output adder	–0.117	–0.117	–0.273	ns
RCLK PLL output adder	–0.011	–0.011	–0.019	ns

Table 4–53 lists column pin delay adders when using the regional clock in Arria GX devices.

Table 4–53. EP1AGX20 Column Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.081	0.081	0.223	ns
RCLK PLL input adder	–0.012	–0.012	–0.008	ns
RCLK output adder	–0.081	–0.081	–0.224	ns
RCLK PLL output adder	1.11	1.11	2.658	ns

Table 4–63. EP1AGX50 Column Pins Output Timing Parameters (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.695	2.695	5.893	ns
		GCLK PLL	t_{CO}	1.239	1.239	2.780	ns
3.3-V LVCMOS	12 mA	GCLK	t_{CO}	2.663	2.663	5.809	ns
		GCLK PLL	t_{CO}	1.211	1.211	2.702	ns
3.3-V LVCMOS	16 mA	GCLK	t_{CO}	2.666	2.666	5.776	ns
		GCLK PLL	t_{CO}	1.218	1.218	2.670	ns
3.3-V LVCMOS	20 mA	GCLK	t_{CO}	2.651	2.651	5.758	ns
		GCLK PLL	t_{CO}	1.205	1.205	2.652	ns
3.3-V LVCMOS	24 mA	GCLK	t_{CO}	2.638	2.638	5.736	ns
		GCLK PLL	t_{CO}	1.194	1.194	2.630	ns
2.5 V	4 mA	GCLK	t_{CO}	2.754	2.754	6.240	ns
		GCLK PLL	t_{CO}	1.293	1.293	3.107	ns
2.5 V	8 mA	GCLK	t_{CO}	2.697	2.697	5.963	ns
		GCLK PLL	t_{CO}	1.241	1.241	2.845	ns
2.5 V	12 mA	GCLK	t_{CO}	2.672	2.672	5.837	ns
		GCLK PLL	t_{CO}	1.220	1.220	2.728	ns
2.5 V	16 mA	GCLK	t_{CO}	2.654	2.654	5.760	ns
		GCLK PLL	t_{CO}	1.202	1.202	2.654	ns
1.8 V	2 mA	GCLK	t_{CO}	2.804	2.804	7.295	ns
		GCLK PLL	t_{CO}	1.333	1.333	4.099	ns
1.8 V	4 mA	GCLK	t_{CO}	2.808	2.808	6.479	ns
		GCLK PLL	t_{CO}	1.338	1.338	3.325	ns
1.8 V	6 mA	GCLK	t_{CO}	2.717	2.717	6.195	ns
		GCLK PLL	t_{CO}	1.262	1.262	3.061	ns
1.8 V	8 mA	GCLK	t_{CO}	2.719	2.719	6.098	ns
		GCLK PLL	t_{CO}	1.264	1.264	2.970	ns
1.8 V	10 mA	GCLK	t_{CO}	2.671	2.671	6.012	ns
		GCLK PLL	t_{CO}	1.218	1.218	2.893	ns
1.8 V	12 mA	GCLK	t_{CO}	2.671	2.671	5.953	ns
		GCLK PLL	t_{CO}	1.219	1.219	2.836	ns
1.5 V	2 mA	GCLK	t_{CO}	2.779	2.779	6.815	ns
		GCLK PLL	t_{CO}	1.313	1.313	3.629	ns
1.5 V	4 mA	GCLK	t_{CO}	2.703	2.703	6.210	ns
		GCLK PLL	t_{CO}	1.249	1.249	3.060	ns
1.5 V	6 mA	GCLK	t_{CO}	2.705	2.705	6.118	ns
		GCLK PLL	t_{CO}	1.252	1.252	2.942	ns
1.5 V	8 mA	GCLK	t_{CO}	2.660	2.660	6.014	ns
		GCLK PLL	t_{CO}	1.211	1.211	2.889	ns

Table 4–63. EP1AGX50 Column Pins Output Timing Parameters (Part 3 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.648	2.648	5.777	ns
		GCLK PLL	t_{CO}	1.202	1.202	2.675	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.628	2.628	5.722	ns
		GCLK PLL	t_{CO}	1.185	1.185	2.625	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.606	2.606	5.649	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.552	ns
SSTL-2 CLASS II	20 mA	GCLK	t_{CO}	2.606	2.606	5.636	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.539	ns
SSTL-2 CLASS II	24 mA	GCLK	t_{CO}	2.601	2.601	5.634	ns
		GCLK PLL	t_{CO}	1.160	1.160	2.537	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.643	2.643	5.749	ns
		GCLK PLL	t_{CO}	1.193	1.193	2.639	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.649	2.649	5.708	ns
		GCLK PLL	t_{CO}	1.203	1.203	2.607	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.626	2.626	5.686	ns
		GCLK PLL	t_{CO}	1.182	1.182	2.588	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.630	2.630	5.685	ns
		GCLK PLL	t_{CO}	1.187	1.187	2.586	ns
SSTL-18 CLASS I	12 mA	GCLK	t_{CO}	2.625	2.625	5.669	ns
		GCLK PLL	t_{CO}	1.181	1.181	2.572	ns
SSTL-18 CLASS II	8 mA	GCLK	t_{CO}	2.614	2.614	5.635	ns
		GCLK PLL	t_{CO}	1.170	1.170	2.538	ns
SSTL-18 CLASS II	16 mA	GCLK	t_{CO}	2.623	2.623	5.613	ns
		GCLK PLL	t_{CO}	1.182	1.182	2.516	ns
SSTL-18 CLASS II	18 mA	GCLK	t_{CO}	2.616	2.616	5.621	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.524	ns
SSTL-18 CLASS II	20 mA	GCLK	t_{CO}	2.616	2.616	5.619	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.522	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.637	2.637	5.676	ns
		GCLK PLL	t_{CO}	1.196	1.196	2.570	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.645	2.645	5.659	ns
		GCLK PLL	t_{CO}	1.207	1.207	2.562	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.623	2.623	5.648	ns
		GCLK PLL	t_{CO}	1.185	1.185	2.551	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.627	2.627	5.654	ns
		GCLK PLL	t_{CO}	1.189	1.189	2.557	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.619	2.619	5.647	ns
		GCLK PLL	t_{CO}	1.181	1.181	2.550	ns

Table 4–75. EP1AGX90 Column Pins Output Timing Parameters (Part 4 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
1.5-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.845	2.845	6.264	ns
		GCLK PLL	t_{CO}	0.783	0.783	2.133	ns
1.5-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.839	2.839	6.262	ns
		GCLK PLL	t_{CO}	0.777	0.777	2.131	ns
1.5-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.826	2.826	6.074	ns
		GCLK PLL	t_{CO}	0.764	0.764	1.943	ns
1.5-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.829	2.829	6.084	ns
		GCLK PLL	t_{CO}	0.767	0.767	1.953	ns
1.5-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.831	2.831	6.097	ns
		GCLK PLL	t_{CO}	0.769	0.769	1.966	ns
3.3-V PCI	—	GCLK	t_{CO}	2.987	2.987	6.414	ns
		GCLK PLL	t_{CO}	0.923	0.923	2.279	ns
3.3-V PCI-X	—	GCLK	t_{CO}	2.987	2.987	6.414	ns
		GCLK PLL	t_{CO}	0.923	0.923	2.279	ns
LVDS	—	GCLK	t_{CO}	3.835	3.835	7.541	ns
		GCLK PLL	t_{CO}	1.769	1.769	3.404	ns

Table 4–76 through Table 4–77 list the EP1AGX90 regional clock (RCLK) adder values that should be added to the GCLK values. These adder values are used to determine I/O timing when the I/O pin is driven using the regional clock. This applies for all I/O standards supported by Arria GX with general purpose I/O pins.

Table 4–76 lists row pin delay adders when using the regional clock in Arria GX devices.

Table 4–76. EP1AGX90 Row Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.175	0.175	0.418	ns
RCLK PLL input adder	0.007	0.007	0.015	ns
RCLK output adder	–0.175	–0.175	–0.418	ns
RCLK PLL output adder	–0.007	–0.007	–0.015	ns

Table 4–102. Arria GX Maximum Input Toggle Rate for Column I/O Pins

I/O Standards	–6 Speed Grade	Units
SSTL-18 CLASS II	467	MHz
1.8-V HSTL CLASS I	467	MHz
1.8-V HSTL CLASS II	467	MHz
1.5-V HSTL CLASS I	467	MHz
1.5-V HSTL CLASS II	467	MHz
3.3-V PCI	420	MHz
3.3-V PCI-X	420	MHz

Table 4–103 shows the maximum input clock toggle rates for Arria GX device row I/O pins.

Table 4–103. Arria GX Maximum Input Toggle Rate for Row I/O Pins

I/O Standards	–6 Speed Grade	Units
3.3-V LVTTL	420	MHz
3.3-V LVCMOS	420	MHz
2.5 V	420	MHz
1.8 V	420	MHz
1.5 V	420	MHz
SSTL-2 CLASS I	467	MHz
SSTL-2 CLASS II	467	MHz
SSTL-18 CLASS I	467	MHz
SSTL-18 CLASS II	467	MHz
1.8-V HSTL CLASS I	467	MHz
1.8-V HSTL CLASS II	467	MHz
1.5-V HSTL CLASS I	467	MHz
1.5-V HSTL CLASS II	467	MHz
LVDS	392	MHz

Table 4–104 shows the maximum input clock toggle rates for Arria GX device dedicated clock pins.

Table 4–104. Arria GX Maximum Input Clock Rate for Dedicated Clock Pins (Part 1 of 2)

I/O Standards	–6 Speed Grade	Units
3.3-V LVTTL	373	MHz
3.3-V LVCMOS	373	MHz
2.5 V	373	MHz
1.8 V	373	MHz
1.5 V	373	MHz
SSTL-2 CLASS I	467	MHz
SSTL-2 CLASS II	467	MHz
3.3-V PCI	373	MHz

Table 4–107. Arria GX Maximum Output Clock Rate for Dedicated Clock Pins (Part 4 of 4)

I/O Standards	Drive Strength	–6 Speed Grade	Units
1.5 V	SERIES_50_OHMS	373	MHz
SSTL-2 CLASS I	SERIES_50_OHMS	467	MHz
SSTL-2 CLASS II	SERIES_25_OHMS	467	MHz
SSTL-18 CLASS I	SERIES_50_OHMS	327	MHz
SSTL-18 CLASS II	SERIES_25_OHMS	420	MHz
1.8-V HSTL CLASS I	SERIES_50_OHMS	561	MHz
1.8-V HSTL CLASS II	SERIES_25_OHMS	420	MHz
1.5-V HSTL CLASS I	SERIES_50_OHMS	467	MHz
1.2-V HSTL	SERIES_50_OHMS	233	MHz
DIFFERENTIAL SSTL-2	SERIES_50_OHMS	467	MHz
DIFFERENTIAL 2.5-V SSTL CLASS II	SERIES_25_OHMS	467	MHz
DIFFERENTIAL 1.8-V SSTL CLASS I	SERIES_50_OHMS	327	MHz
DIFFERENTIAL 1.8-V SSTL CLASS II	SERIES_25_OHMS	420	MHz
DIFFERENTIAL 1.8-V HSTL CLASS I	SERIES_50_OHMS	561	MHz
DIFFERENTIAL 1.8-V HSTL CLASS II	SERIES_25_OHMS	420	MHz
DIFFERENTIAL 1.5-V HSTL CLASS I	SERIES_50_OHMS	467	MHz
DIFFERENTIAL 1.2-V HSTL	SERIES_50_OHMS	233	MHz

Duty Cycle Distortion

Duty cycle distortion (DCD) describes how much the falling edge of a clock is off from its ideal position. The ideal position is when both the clock high time (CLKH) and the clock low time (CLKL) equal half of the clock period (T), as shown in Figure 4–10. DCD is the deviation of the non-ideal falling edge from the ideal falling edge, such as D1 for the falling edge A and D2 for the falling edge B (refer to Figure 4–10). The maximum DCD for a clock is the larger value of D1 and D2.

Document Revision History

Table 4–124 lists the revision history for this chapter.

Table 4–124. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
December 2009, v2.0	■ Updated Table 4–104, Table 4–105, and Table 4–106. ■ Document template update. ■ Minor text edits.	—
April 2009 v1.4	■ Updated Table 4–6 and Table 4–7. ■ Updated "Maximum Input and Output Clock Toggle Rate" section.	—
May 2008 v1.3	Updated: ■ Table 4–5 ■ Table 4–7 ■ Table 4–8 ■ Table 4–9 ■ Table 4–10 ■ Table 4–11 ■ Table 4–12 ■ Table 4–13 ■ Table 4–14 ■ Table 4–15 ■ Table 4–16 ■ Table 4–17 ■ Table 4–43 ■ Table 4–116 ■ Table 4–117	—
	Updated: ■ Figure 4–4	—
	Minor text edits.	—
August 2007 v1.2	Removed "Preliminary" from each page.	—
	Removed "Preliminary" note from Tables 4–44, 4–45, and 4–47.	—
	Added "Referenced Documents" section.	—
June 2007 v1.1	Updated Table 4–99.	—
	Added GIGE information.	—
May 2007 v1.0	Initial release.	—