Intel - EP1AGX50DF1152C6N Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2508
Number of Logic Elements/Cells	50160
Total RAM Bits	2475072
Number of I/O	514
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1agx50df1152c6n

Table 1–1. Arria GX Device Features (Part 2 of 2)

Feature	EP1AGX20C	EP1AGX35C/D		EP1AGX50C/D		EP1AGX60C/D/E			EP1AGX90E
	C	C	D	C	D	C	D	E	E
Source-synchronous transmit channels	29	29	29	29	29, 42	29	29	42	45
M512 RAM blocks (32 × 18 bits)	166	197		313		326			478
M4K RAM blocks (128 × 36 bits)	118	140		242		252			400
M-RAM blocks (4096 × 144 bits)	1	1		2		2			4
Total RAM bits	1,229,184	1,348,416		2,475,072		2,528,640			4,477,824
Embedded multipliers (18 × 18)	40	56		104		128			176
DSP blocks	10	14		26		32			44
PLLs	4	4		4	4, 8	4		8	8
Maximum user I/O pins	230, 341	230	341	229	350, 514	229	350	514	538

Arria GX devices are available in space-saving FBGA packages (refer to Table 1–2). All Arria GX devices support vertical migration within the same package. With vertical migration support, designers can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities. For I/O pin migration across densities, the designer must cross-reference the available I/O pins with the device pin-outs for all planned densities of a given package type to identify which I/O pins are migratable.

Table 1–2. Arria GX Package Options (Pin Counts and Transceiver Channels) (Part 1 of 2)

Device	Transceiver Channels	Source-Synchronous Channels		Maximum User I/O Pin Count		
		Receive	Transmit	484-Pin FBGA (23 mm)	780-Pin FBGA (29 mm)	1152-Pin FBGA (35 mm)
EP1AGX20C	4	31	29	230	341	—
EP1AGX35C	4	31	29	230	—	—
EP1AGX50C	4	31	29	229	—	—
EP1AGX60C	4	31	29	229	—	—
EP1AGX35D	8	31	29	—	341	—
EP1AGX50D	8	31, 42	29, 42	—	350	514

Each transceiver channel is full-duplex and consists of a transmitter channel and a receiver channel.

The transmitter channel contains the following sub-blocks:

- Transmitter phase compensation first-in first-out (FIFO) buffer
- Byte serializer (optional)
- 8B/10B encoder (optional)
- Serializer (parallel-to-serial converter)
- Transmitter differential output buffer

The receiver channel contains the following:

- Receiver differential input buffer
- Receiver lock detector and run length checker
- CRU
- Deserializer
- Pattern detector
- Word aligner
- Lane deskew
- Rate matcher (optional)
- 8B/10B decoder (optional)
- Byte deserializer (optional)
- Receiver phase compensation FIFO buffer

You can configure the transceiver channels to the desired functional modes using the ALT2GXB MegaCore instance in the Quartus® II MegaWizard™ Plug-in Manager for the Arria GX device family. Depending on the selected functional mode, the Quartus II software automatically configures the transceiver channels to employ a subset of the sub-blocks listed above.

Transmitter Path

This section describes the data path through the Arria GX transmitter. The sub-blocks are described in order from the PLD-transmitter parallel interface to the serial transmitter buffer.

Clock Multiplier Unit

Each transceiver block has a clock multiplier unit (CMU) that takes in a reference clock and synthesizes two clocks: a high-speed serial clock to serialize the data and a low-speed parallel clock to clock the transmitter digital logic (PCS).

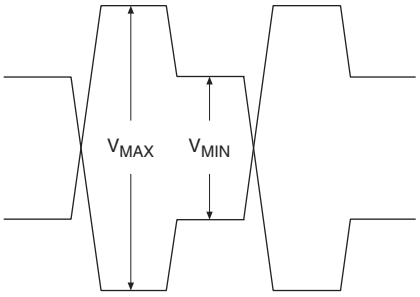
The CMU is further divided into three sub-blocks:

- One transmitter PLL
- One central clock divider block
- Four local clock divider blocks (one per channel)

Programmable Pre-Emphasis

The programmable pre-emphasis module controls the output driver to boost high frequency components and compensate for losses in the transmission medium, as shown in Figure 2–10. Pre-emphasis is set statically using the ALTGXB megafunction.

Figure 2–10. Pre-Emphasis Signaling



$$\text{Pre-Emphasis \%} = \left(\frac{V_{MAX}}{V_{MIN}} - 1\right) \times 100$$

Pre-emphasis percentage is defined as $(V_{MAX}/V_{MIN} - 1) \times 100$, where V_{MAX} is the differential emphasized voltage (peak-to-peak) and V_{MIN} is the differential steady-state voltage (peak-to-peak).

PCI Express (PIPE) Receiver Detect

The Arria GX transmitter buffer has a built-in receiver detection circuit for use in PCI Express (PIPE) mode. This circuit provides the ability to detect if there is a receiver downstream by sending out a pulse on the channel and monitoring the reflection. This mode requires a tri-stated transmitter buffer (in electrical idle mode).

PCI Express (PIPE) Electric Idles (or Individual Transmitter Tri-State)

The Arria GX transmitter buffer supports PCI Express (PIPE) electrical idles. This feature is only active in PCI Express (PIPE) mode. The `tx_forceelecidle` port puts the transmitter buffer in electrical idle mode. This port is available in all PCI Express (PIPE) power-down modes and has specific usage in each mode.

Receiver Path

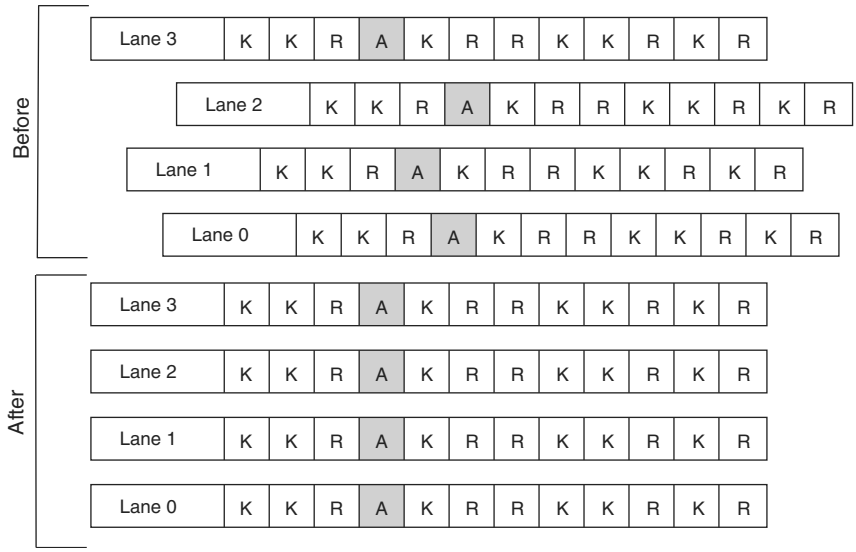
This section describes the data path through the Arria GX receiver. The sub-blocks are described in order from the receiver buffer to the PLD-receiver parallel interface.

Receiver Buffer

The Arria GX receiver input buffer supports the 1.2-V and 1.5-V PCML I/O standards at rates up to 3.125 Gbps. The common mode voltage of the receiver input buffer is programmable between 0.85 V and 1.2 V. You must select the 0.85 V common mode voltage for AC- and DC-coupled PCML links and 1.2 V common mode voltage for DC-coupled LVDS links.

Figure 2–16 shows misaligned channels before the channel aligner and the aligned channels after the channel aligner.

Figure 2–16. Before and After the Channel Aligner



Rate Matcher

In asynchronous systems, the upstream transmitter and local receiver can be clocked with independent reference clock sources. Frequency differences in the order of a few hundred PPM can potentially corrupt the data at the receiver.

The rate matcher compensates for small clock frequency differences between the upstream transmitter and the local receiver clocks by inserting or removing skip characters from the inter packet gap (IPG) or idle streams. It inserts a skip character if the local receiver is running a faster clock than the upstream transmitter. It deletes a skip character if the local receiver is running a slower clock than the upstream transmitter. The Quartus II software automatically configures the appropriate skip character as specified in the IEEE 802.3 for GIGE mode and PCI-Express Base Specification for PCI Express (PIPE) mode. The rate matcher is bypassed in Serial RapidIO and must be implemented in the PLD logic array or external circuits depending on your system design.

Table 2–5 lists the maximum frequency difference that the rate matcher can tolerate in XAUI, PCI Express (PIPE), GIGE, and Basic functional modes.

Table 2–5. Rate Matcher PPM Tolerance

Function Mode	PPM
XAUI	± 100
PCI Express (PIPE)	± 300
GIGE	± 100
Basic	± 300

For more information about transceiver clocking in all supported functional modes, refer to the *Arria GX Transceiver Architecture* chapter.

PLD Clock Utilization by Transceiver Blocks

Arria GX devices have up to 16 global clock (GCLK) lines and 16 regional clock (RCLK) lines that are used to route the transceiver clocks. The following transceiver clocks use the available global and regional clock resources:

- `pll_inclk` (if driven from an FPGA input pin)
- `rx_cruclk` (if driven from an FPGA input pin)
- `tx_clkout/coreclkout` (CMU low-speed parallel clock forwarded to the PLD)
- Recovered clock from each channel (`rx_clkout`) in non-rate matcher mode
- Calibration clock (`cal_blk_clk`)
- Fixed clock (`fixedclk` used for receiver detect circuitry in PCI Express [PIPE] mode only)

Figure 2–23 and Figure 2–24 show the available GCLK and RCLK resources in Arria GX devices.

Figure 2–23. Global Clock Resources in Arria GX Devices

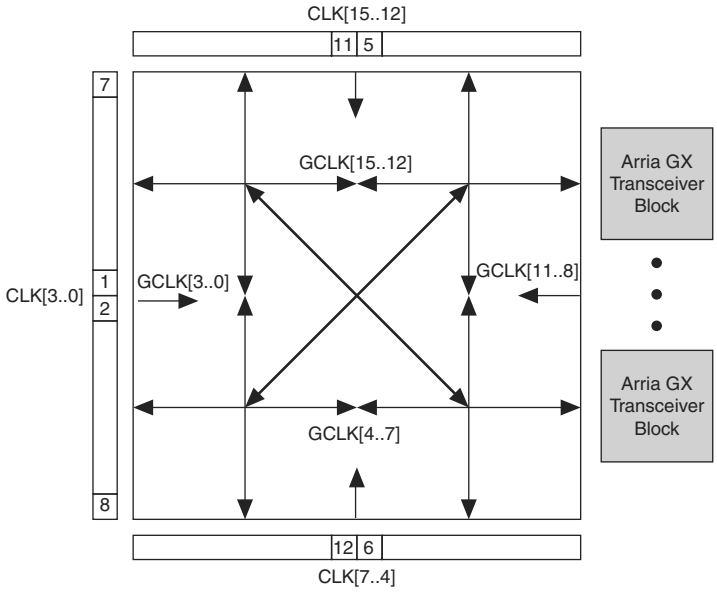
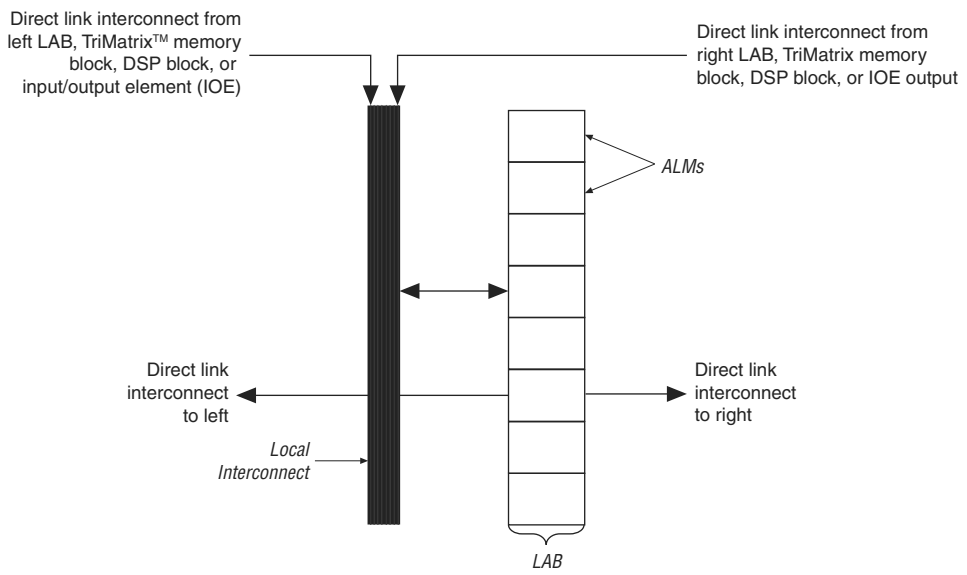


Figure 2–26 shows the direct link connection.

Figure 2–26. Direct Link Connection



LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its ALMs. The control signals include three clocks, three clock enables, two asynchronous clears, synchronous clear, asynchronous preset or load, and synchronous load control signals, providing a maximum of 11 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

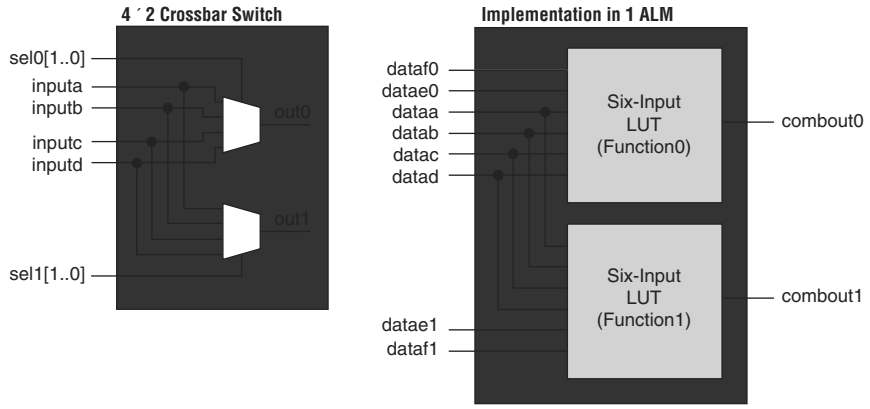
Each LAB can use three clocks and three clock enable signals. However, there can only be up to two unique clocks per LAB, as shown in the LAB control signal generation circuit in Figure 2–27. Each LAB's clock and clock enable signals are linked. For example, any ALM in a particular LAB using the `labclk1` signal also uses `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses two LAB-wide clock signals. De-asserting the clock enable signal turns off the corresponding LAB-wide clock. Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. The asynchronous load acts as a preset when the asynchronous load data input is tied high. When the asynchronous load/preset signal is used, the `labclkena0` signal is no longer available.

The LAB row clocks `[5..0]` and LAB local interconnect generate the LAB-wide control signals. The MultiTrack interconnects have inherently low skew. This low skew allows the MultiTrack interconnects to distribute clock and control signals in addition to data.

To pack two five-input functions into one ALM, the functions must have at least two common inputs. The common inputs are dataa and datab. The combination of a four-input function with a five-input function requires one common input (either dataa or datab).

To implement two six-input functions in one ALM, four inputs must be shared and the combinational function must be the same. For example, a 4 × 2 crossbar switch (two 4-to-1 multiplexers with common inputs and unique select lines) can be implemented in one ALM, as shown in Figure 2–31. The shared inputs are dataa, datab, datac, and datad, while the unique select lines are datae0 and dataf0 for function0, and datae1 and dataf1 for function1. This crossbar switch consumes four LUTs in a four-input LUT-based architecture.

Figure 2–31. 4 × 2 Crossbar Switch Example



In a sparsely used device, functions that can be placed into one ALM can be implemented in separate ALMs. The Quartus II Compiler spreads a design out to achieve the best possible performance. As a device begins to fill up, the Quartus II software automatically uses the full potential of the Arria GX ALM. The Quartus II Compiler automatically searches for functions of common inputs or completely independent functions to be placed into one ALM and to make efficient use of the device resources. In addition, you can manually control resource usage by setting location assignments. Any six-input function can be implemented utilizing inputs dataa, datab, datac, datad, and either datae0 and dataf0 or datae1 and dataf1. If datae0 and dataf0 are used, the output is driven to register0, and/or register0 is bypassed and the data drives out to the interconnect using the top set of output drivers (refer to Figure 2–32). If datae1 and dataf1 are used, the output drives to register1 and/or bypasses register1 and drives to the interconnect using the bottom set of output drivers. The Quartus II Compiler automatically selects the inputs to the LUT. Asynchronous load data for the register comes from the datae or dataf input of the ALM. ALMs in normal mode support register packing.

As indicated, the Arria GX DSP block can support one 36 × 36-bit multiplier in a single DSP block and is true for any combination of signed, unsigned, or mixed sign multiplications.

Figure 2–50 shows one of the columns with surrounding LAB rows.

Figure 2–50. DSP Blocks Arranged in Columns

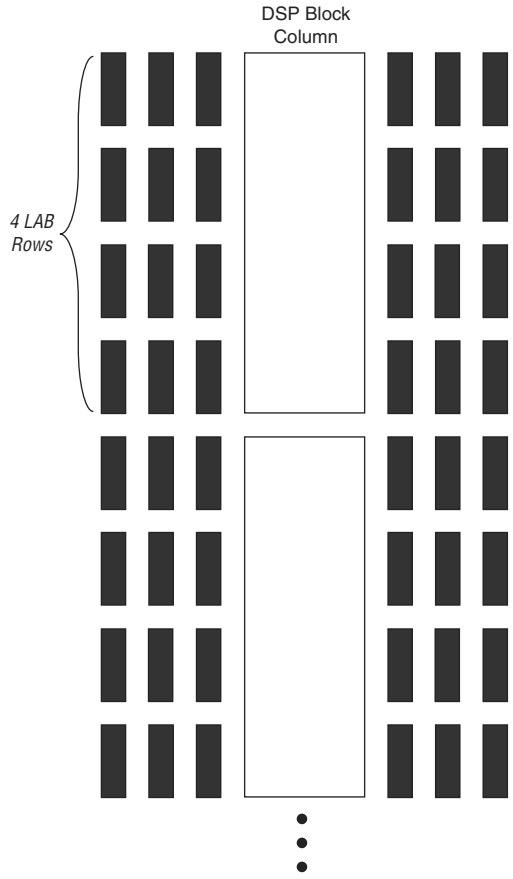


Table 2–13 lists the number of DSP blocks in each Arria GX device. DSP block multipliers can optionally feed an adder/subtractor or accumulator in the block depending on the configuration, which makes routing to ALMs easier, saves ALM routing resources, and increases performance because all connections and blocks are in the DSP block.

Figure 2–52 and Figure 2–53 show the DSP block interfaces to LAB rows.

Figure 2–52. DSP Block Interconnect Interface

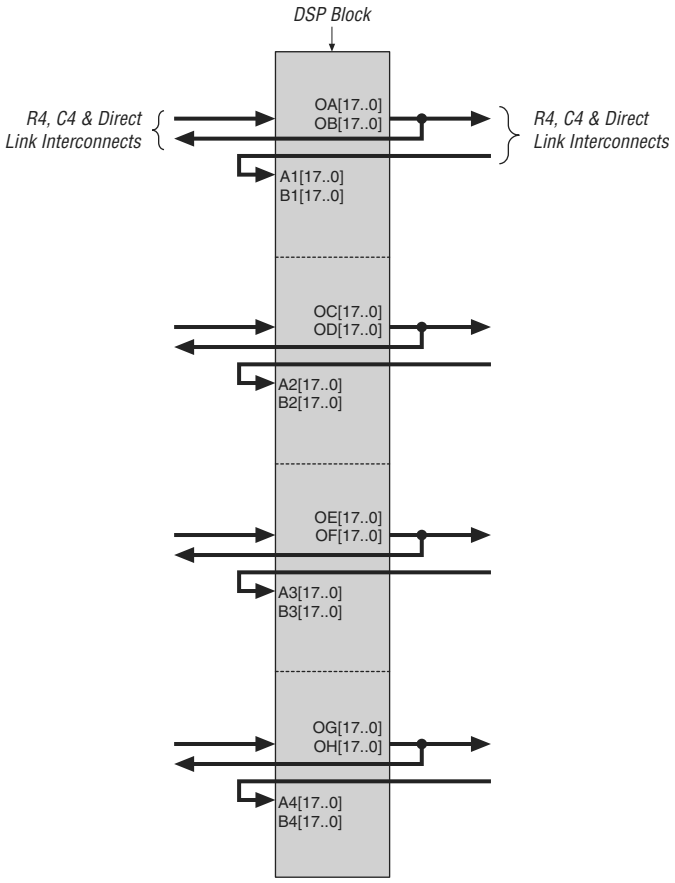
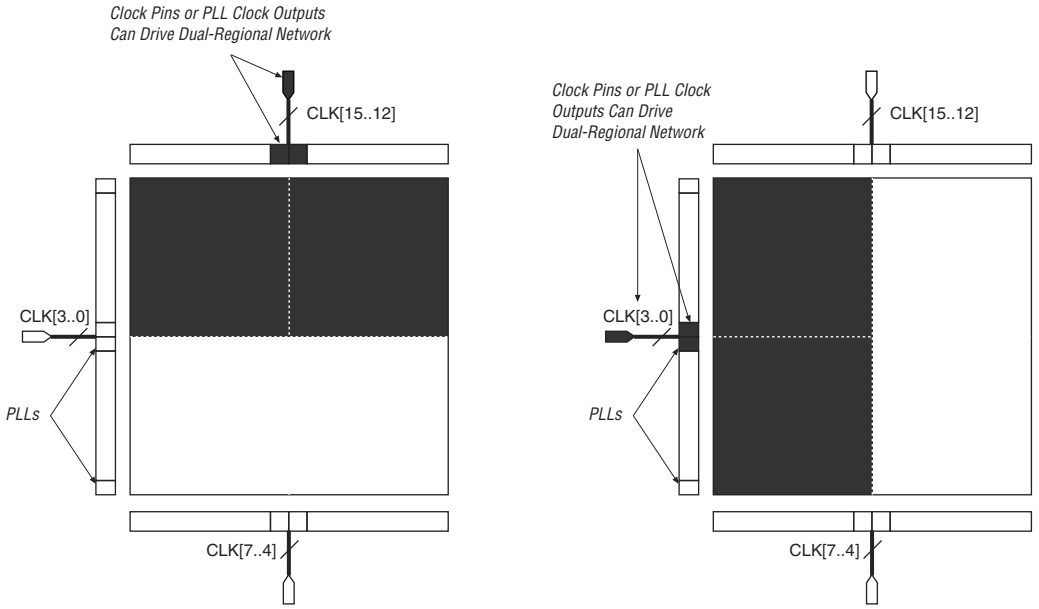


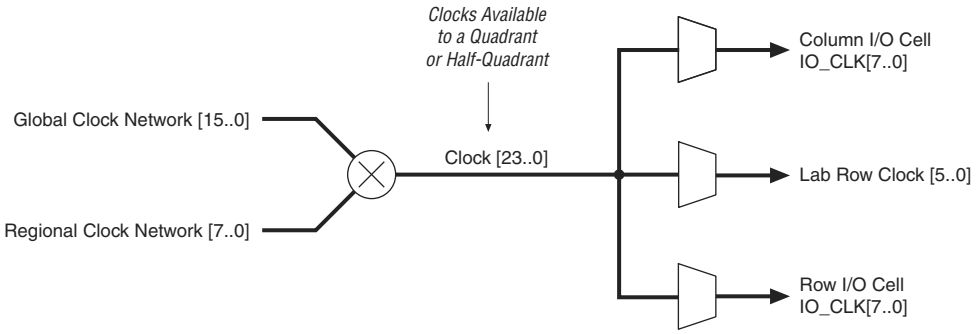
Figure 2–56. Dual-Regional Clocks



Combined Resources

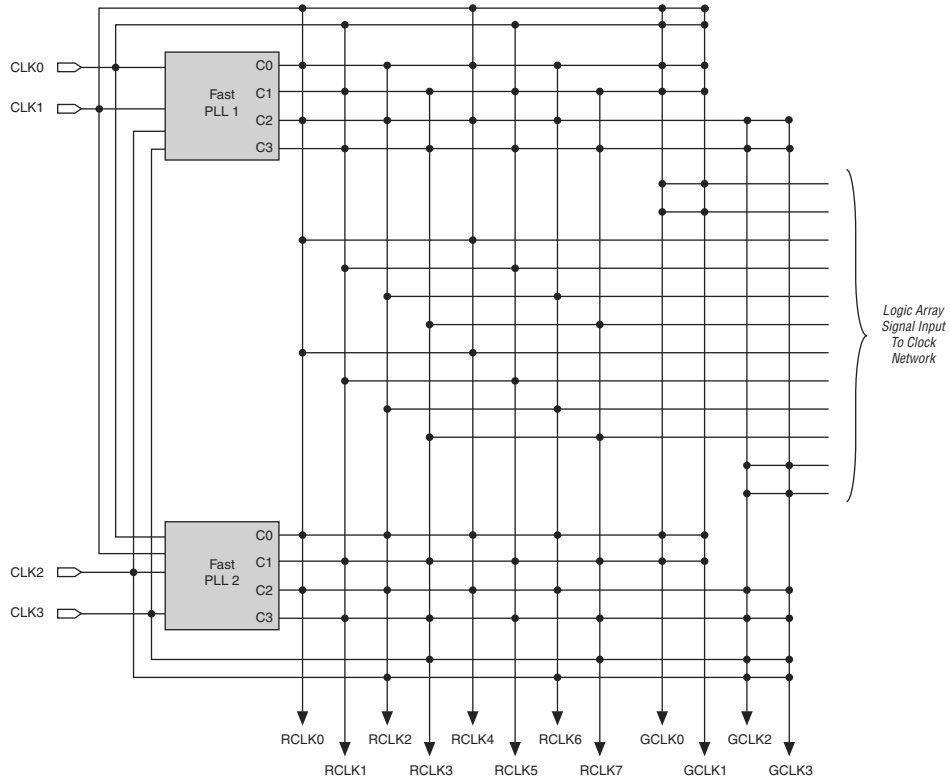
Within each quadrant, there are 24 distinct dedicated clocking resources consisting of 16 global clock lines and eight regional clock lines. Multiplexers are used with these clocks to form buses to drive LAB row clocks, column IOE clocks, or row IOE clocks. Another multiplexer is used at the LAB level to select three of the six row clocks to feed the ALM registers in the LAB (refer to Figure 2–57).

Figure 2–57. Hierarchical Clock Networks Per Quadrant



You can use the Quartus II software to control whether a clock input pin drives either a GCLK, RCLK, or dual-RCLK network. The Quartus II software automatically selects the clocking resources if not specified.

Figure 2–62. Global and Regional Clock Connections from Center Clock Pins and Fast PLL Outputs *(Note 1)*



Note to Figure 2–62:

(1) The global or regional clocks in a fast PLL's quadrant can drive the fast PLL input. A dedicated clock input pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

Table 2–20. Global and Regional Clock Connections from Top Clock Pins and Enhanced PLL Outputs

Top Side Global and Regional Clock Network Connectivity	DLLCLK	CLK12	CLK13	CLK14	CLK15	RCLK24	RCLK25	RCLK26	RCLK27	RCLK28	RCLK29	RCLK30	RCLK31
Clock pins													
CLK12p	✓	✓	✓	—	—	✓	—	—	—	✓	—	—	—
CLK13p	✓	✓	✓	—	—	—	✓	—	—	—	✓	—	—
CLK14p	✓	—	—	✓	✓	—	—	✓	—	—	—	✓	—
CLK15p	✓	—	—	✓	✓	—	—	—	✓	—	—	—	✓
CLK12n	—	✓	—	—	—	✓	—	—	—	✓	—	—	—
CLK13n	—	—	✓	—	—	—	✓	—	—	—	✓	—	—
CLK14n	—	—	—	✓	—	—	—	✓	—	—	—	✓	—
CLK15n	—	—	—	—	✓	—	—	—	✓	—	—	—	✓
Drivers from internal logic													
GCLKDRV0	—	✓	—	—	—	—	—	—	—	—	—	—	—
GCLKDRV1	—	—	✓	—	—	—	—	—	—	—	—	—	—
GCLKDRV2	—	—	—	✓	—	—	—	—	—	—	—	—	—
GCLKDRV3	—	—	—	—	✓	—	—	—	—	—	—	—	—
RCLKDRV0	—	—	—	—	—	✓	—	—	—	✓	—	—	—
RCLKDRV1	—	—	—	—	—	—	✓	—	—	—	✓	—	—
RCLKDRV2	—	—	—	—	—	—	—	✓	—	—	—	✓	—
RCLKDRV3	—	—	—	—	—	—	—	—	✓	—	—	—	✓
RCLKDRV4	—	—	—	—	—	✓	—	—	—	✓	—	—	—
RCLKDRV5	—	—	—	—	—	—	✓	—	—	—	✓	—	—
RCLKDRV6	—	—	—	—	—	—	—	✓	—	—	—	✓	—
RCLKDRV7	—	—	—	—	—	—	—	—	✓	—	—	—	✓
Enhanced PLL5 outputs													
c0	✓	✓	✓	—	—	✓	—	—	—	✓	—	—	—
c1	✓	✓	✓	—	—	—	✓	—	—	—	✓	—	—
c2	✓	—	—	✓	✓	—	—	✓	—	—	—	✓	—
c3	✓	—	—	✓	✓	—	—	—	✓	—	—	—	✓
c4	✓	—	—	—	—	✓	—	✓	—	✓	—	✓	—
c5	✓	—	—	—	—	—	✓	—	✓	—	✓	—	✓
Enhanced PLL 11 outputs													
c0	—	✓	✓	—	—	✓	—	—	—	✓	—	—	—
c1	—	✓	✓	—	—	—	✓	—	—	—	✓	—	—
c2	—	—	—	✓	✓	—	—	✓	—	—	—	✓	—
c3	—	—	—	✓	✓	—	—	—	✓	—	—	—	✓
c4	—	—	—	—	—	✓	—	✓	—	✓	—	✓	—
c5	—	—	—	—	—	—	✓	—	✓	—	✓	—	✓

In addition to the number of configuration methods supported, Arria GX devices also offer decompression and remote system upgrade features. The decompression feature allows Arria GX FPGAs to receive a compressed configuration bitstream and decompress this data in real-time, reducing storage requirements and configuration time. The remote system upgrade feature allows real-time system upgrades from remote locations of Arria GX designs. For more information, refer to "Configuration Schemes" on page 3–5.

Operating Modes

The Arria GX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power up, and before and during configuration. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

SRAM configuration elements allow you to reconfigure Arria GX devices in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, re-initializes the device, and resumes user-mode operation. You can perform in-field upgrades by distributing new configuration files either within the system or remotely.

PORSEL is a dedicated input pin used to select power-on reset (POR) delay times of 12 ms or 100 ms during power up. When the PORSEL pin is connected to ground, the POR time is 100 ms. When the PORSEL pin is connected to V_{CC}, the POR time is 12 ms.

The nIO_PULLUP pin is a dedicated input that chooses whether the internal pull-up resistors on the user I/O pins and dual-purpose configuration I/O pins (nCSO, ASDO, DATA[7..0], nWS, nRS, RDYnBSY, nCS, CS, RUnLU, PGM[2..0], CLKUSR, INIT_DONE, DEV_OE, DEV_CLR) are on or off before and during configuration. A logic high (1.5, 1.8, 2.5, 3.3 V) turns off the weak internal pull-up resistors, while a logic low turns them on.

Arria GX devices also offer a new power supply, V_{CCPD}, which must be connected to 3.3 V in order to power the 3.3-V/2.5-V buffer available on the configuration input pins and JTAG pins. V_{CCPD} applies to all the JTAG input pins (TCK, TMS, TDI, and TRST) and the following configuration pins: nCONFIG, DCLK (when used as an input), nIO_PULLUP, DATA[7..0], RUnLU, nCE, nWS, nRS, CS, nCS, and CLKUSR. The V_{CCSEL} pin allows the V_{CCIO} setting (of the banks where the configuration inputs reside) to be independent of the voltage required by the configuration inputs. Therefore, when selecting the V_{CCIO} voltage, you do not have to take the VIL and VIH levels driven to the configuration inputs into consideration. The configuration input pins, nCONFIG, DCLK (when used as an input), nIO_PULLUP, RUnLU, nCE, nWS, nRS, CS, nCS, and CLKUSR, have a dual buffer design: a 3.3-V/2.5-V input buffer and a 1.8-V/1.5-V input buffer. The V_{CCSEL} input pin selects which input buffer is used. The 3.3-V/2.5-V input buffer is powered by V_{CCPD}, while the 1.8-V/1.5-V input buffer is powered by V_{CCIO}.

Figure 4–3 and Figure 4–4 show differential receiver input and transmitter output waveforms, respectively.

Figure 4–3. Receiver Input Waveform

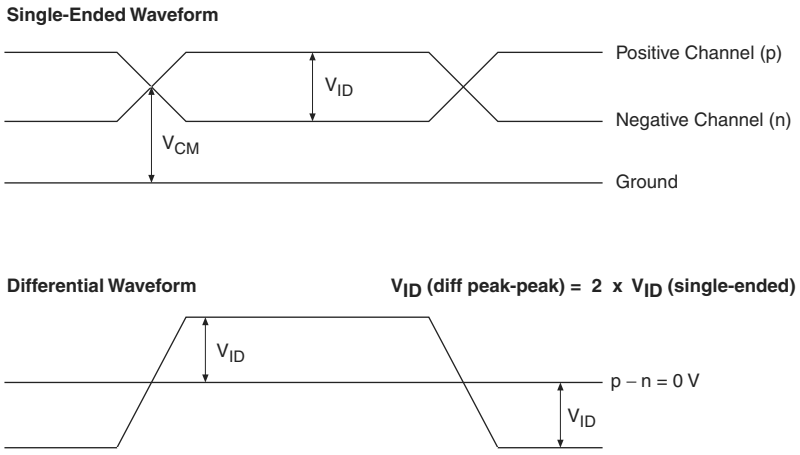


Figure 4–4. Transmitter Output Waveform

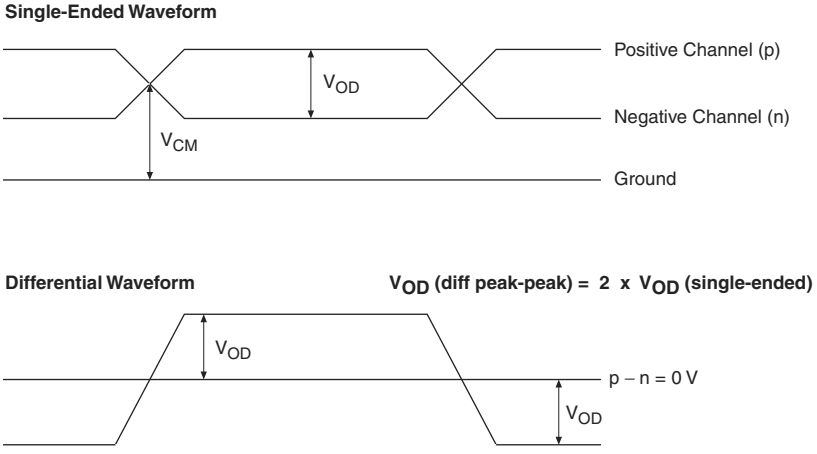


Table 4–7 lists the Arria GX transceiver block AC specification.

Table 4–7. Arria GX Transceiver Block AC Specification *(Note 1)*, *(2)*, *(3)* (Part 1 of 4)

Description	Condition	–6 Speed Grade Commercial & Industrial	Units
XAUI Transmit Jitter Generation *(4)*			
Total jitter at 3.125 Gbps	REFCLK = 156.25 MHz Pattern = CJPAT V_{OD} = 1200 mV No Pre-emphasis	0.3	UI

Table 4–9. PCS Latency (Part 2 of 2) (Part 2 of 2)

Functional Mode	Configuration	Receiver PCS Latency									
		Word Aligner	Deskew FIFO	Rate Matcher *(3)*	8B/10B Decoder	Receiver State Machine	Byte Deserializer	Byte Order	Receiver Phase Comp FIFO	Receiver PIPE	Sum *(2)*
BASIC Single Width	8/10-bit channel width; with Rate Matcher	4–5	—	11–13	1	—	1	1	1–2	1	19–23
	8/10-bit channel width; without Rate Matcher	4–5	—	—	1	—	1	1	1–2	—	8–10
	16/20-bit channel width; with Rate Matcher	2–2.5	—	5.5–6.5	0.5	—	1	1	1–2	—	11–14
	16/20-bit channel width; without Rate Matcher	2–2.5	—	—	0.5	—	1	1	1–2	—	6–7

Notes to Table 4–9:

(1) The latency numbers are with respect to the PLD-transceiver interface clock cycles.

(2) The total latency number is rounded off in the Sum column.

(3) The rate matcher latency shown is the steady state latency. Actual latency may vary depending on the skip ordered set gap allowed by the protocol, actual PPM difference between the reference clocks, and so forth.

Table 4–10 through Table 4–13 show the typical V_{OD} for data rates from 600 Mbps to 3.125 Gbps. The specification is for measurement at the package ball.

Table 4–10. Typical V_{OD} Setting, TX Term = 100 Ω

V_{cc} HTX = 1.5 V	V_{OD} Setting (mV)				
	400	600	800	1000	1200
V_{OD} Typical (mV)	430	625	830	1020	1200

Table 4–11. Typical V_{OD} Setting, TX Term = 100 Ω

V_{cc} HTX = 1.2 V	V_{OD} Setting (mV)				
	320	480	640	800	960
V_{OD} Typical (mV)	344	500	664	816	960

Table 4–12. Typical Pre-Emphasis (First Post-Tap), *(Note 1)*

V_{cc} HTX = 1.5 V	First Post Tap Pre-Emphasis Level				
V_{OD} Setting (mV)	1	2	3	4	5
	TX Term = 100 Ω				
400	24%	62%	112%	184%	—
600	—	31%	56%	86%	122%
800	—	20%	35%	53%	73%

Table 4–74. EP1AGX90 Row Pins Output Timing Parameters (Part 2 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
1.8 V	2 mA	GCLK	t_{CO}	3.087	3.087	7.723	ns
		GCLK PLL	t_{CO}	1.034	1.034	3.605	ns
1.8 V	4 mA	GCLK	t_{CO}	3.076	3.076	6.944	ns
		GCLK PLL	t_{CO}	1.023	1.023	2.826	ns
1.8 V	6 mA	GCLK	t_{CO}	2.965	2.965	6.643	ns
		GCLK PLL	t_{CO}	0.912	0.912	2.525	ns
1.8 V	8 mA	GCLK	t_{CO}	2.934	2.934	6.529	ns
		GCLK PLL	t_{CO}	0.881	0.881	2.411	ns
1.5 V	2 mA	GCLK	t_{CO}	3.047	3.047	7.222	ns
		GCLK PLL	t_{CO}	0.994	0.994	3.104	ns
1.5 V	4 mA	GCLK	t_{CO}	2.940	2.940	6.621	ns
		GCLK PLL	t_{CO}	0.887	0.887	2.503	ns
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.890	2.890	6.294	ns
		GCLK PLL	t_{CO}	0.824	0.824	2.157	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.866	2.866	6.218	ns
		GCLK PLL	t_{CO}	0.800	0.800	2.081	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.832	2.832	6.087	ns
		GCLK PLL	t_{CO}	0.766	0.766	1.950	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.872	2.872	6.227	ns
		GCLK PLL	t_{CO}	0.819	0.819	2.109	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.878	2.878	6.162	ns
		GCLK PLL	t_{CO}	0.800	0.800	2.006	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.854	2.854	6.145	ns
		GCLK PLL	t_{CO}	0.776	0.776	1.989	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.857	2.857	6.124	ns
		GCLK PLL	t_{CO}	0.779	0.779	1.968	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.853	2.853	6.137	ns
		GCLK PLL	t_{CO}	0.800	0.800	2.019	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.858	2.858	6.107	ns
		GCLK PLL	t_{CO}	0.780	0.780	1.951	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.840	2.840	6.103	ns
		GCLK PLL	t_{CO}	0.762	0.762	1.947	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.844	2.844	6.092	ns
		GCLK PLL	t_{CO}	0.766	0.766	1.936	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.835	2.835	6.091	ns
		GCLK PLL	t_{CO}	0.757	0.757	1.935	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.852	2.852	6.114	ns
		GCLK PLL	t_{CO}	0.799	0.799	1.996	ns

Table 4–99 lists performance notes.

Table 4–99. Arria GX Performance Notes

Applications		Resources Used			Performance
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	–6 Speed Grade
LE	16-to-1 multiplexer	5	0	0	168.41
	32-to-1 multiplexer	11	0	0	334.11
	16-bit counter	16	0	0	374.0
	64-bit counter	64	0	0	168.41
TriMatrix Memory M512 block	Simple dual-port RAM 32 x 18 bit	0	1	0	348.0
	FIFO 32 x 18 bit	0	1	0	333.22
TriMatrix Memory M4K block	Simple dual-port RAM 128 x 36 bit	0	1	0	344.71
	True dual-port RAM 128 x 18 bit	0	1	0	348.0
TriMatrix Memory MegaRAM block	Single port RAM 4K x 144 bit	0	2	0	244.0
	Simple dual-port RAM 4K x 144 bit	0	1	0	292.0
	True dual-port RAM 4K x 144 bit	0	2	0	244.0
	Single port RAM 8K x 72 bit	0	1	0	247.0
	Simple dual-port RAM 8K x 72 bit	0	1	0	292.0
	Single port RAM 16K x 36 bit	0	1	0	254.0
	Simple dual-port RAM 16K x 36 bit	0	1	0	292.0
	True dual-port RAM 16K x 36 bit	0	1	0	251.0
	Single port RAM 32K x 18 bit	0	1	0	317.36
	Simple dual-port RAM 32K x 18 bit	0	1	0	292.0
	True dual-port RAM 32K x 18 bit	0	1	0	251.0
	Single port RAM 64K x 9 bit	0	1	0	254.0
	Simple dual-port RAM 64K x 9 bit	0	1	0	292.0
	True dual-port RAM 64K x 9 bit	0	1	0	251.0

Table 4–102. Arria GX Maximum Input Toggle Rate for Column I/O Pins

I/O Standards	–6 Speed Grade	Units
SSTL-18 CLASS II	467	MHz
1.8-V HSTL CLASS I	467	MHz
1.8-V HSTL CLASS II	467	MHz
1.5-V HSTL CLASS I	467	MHz
1.5-V HSTL CLASS II	467	MHz
3.3-V PCI	420	MHz
3.3-V PCI-X	420	MHz

Table 4–103 shows the maximum input clock toggle rates for Arria GX device row I/O pins.

Table 4–103. Arria GX Maximum Input Toggle Rate for Row I/O Pins

I/O Standards	–6 Speed Grade	Units
3.3-V LVTTL	420	MHz
3.3-V LVCMOS	420	MHz
2.5 V	420	MHz
1.8 V	420	MHz
1.5 V	420	MHz
SSTL-2 CLASS I	467	MHz
SSTL-2 CLASS II	467	MHz
SSTL-18 CLASS I	467	MHz
SSTL-18 CLASS II	467	MHz
1.8-V HSTL CLASS I	467	MHz
1.8-V HSTL CLASS II	467	MHz
1.5-V HSTL CLASS I	467	MHz
1.5-V HSTL CLASS II	467	MHz
LVDS	392	MHz

Table 4–104 shows the maximum input clock toggle rates for Arria GX device dedicated clock pins.

Table 4–104. Arria GX Maximum Input Clock Rate for Dedicated Clock Pins (Part 1 of 2)

I/O Standards	–6 Speed Grade	Units
3.3-V LVTTL	373	MHz
3.3-V LVCMOS	373	MHz
2.5 V	373	MHz
1.8 V	373	MHz
1.5 V	373	MHz
SSTL-2 CLASS I	467	MHz
SSTL-2 CLASS II	467	MHz
3.3-V PCI	373	MHz

Table 4–117. Fast PLL Specifications (Part 2 of 2)

Name	Description	Min	Typ	Max	Units
$t_{ARESET\_RECONFIG}$	Minimum pulse width on the areset signal when using PLL reconfiguration. Reset the PLL after scandone goes high.	500	—	—	ns

Note to Table 4–117:

(1) This is limited by the I/O f_{MAX}.

External Memory Interface Specifications

Table 4–118 through Table 4–122 list Arria GX device specifications for the dedicated circuitry used for interfacing with external memory devices.

Table 4–118. DLL Frequency Range Specifications

Frequency Mode	Frequency Range (MHz)
0	100 to 175
1	150 to 230
2	200 to 310

Table 4–119. DQS Jitter Specifications for DLL-Delayed Clock (tDQS_JITTER) , *(Note 1)*

Number of DQS Delay Buffer Stages *(2)*	Commercial (ps)	Industrial (ps)
1	80	110
2	110	130
3	130	180
4	160	210

Notes to Table 4–119:

(1) Peak-to-peak period jitter on the phase-shifted DQS clock. For example, jitter on two delay stages under commercial conditions is 200 ps peak-to-peak or 100 ps.

(2) Delay stages used for requested DQS phase shift are reported in a project's Compilation Report in the Quartus II software.

Table 4–120. DQS Phase-Shift Error Specifications for DLL-Delayed Clock (t_{DQS_PSERR})

Number of DQS Delay Buffer Stages	–6 Speed Grade (ps)
1	35
2	70
3	105
4	140

Table 4–121. DQS Bus Clock Skew Adder Specifications ($t_{DQS\_CLOCK\_SKEW\_ADDER}$)

Mode	DQS Clock Skew Adder (ps)
4 DQ per DQS	40
9 DQ per DQS	70
18 DQ per DQS	75
36 DQ per DQS	95

Table 4–122. DQS Phase Offset Delay Per Stage (ps) *Note (1), (2), (3)*

Speed Grade	Positive Offset		Negative Offset	
	Min	Max	Min	Max
–6	10	16	8	12

Notes to Table 4–122:

(1) The delay settings are linear.
(2) The valid settings for phase offset are –32 to +31.
(3) The typical value equals the average of the minimum and maximum values.

JTAG Timing Specifications

Figure 4–13 shows the timing requirements for the JTAG signals

Figure 4–13. Arria GX JTAG Waveforms.