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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2508
Number of Logic Elements/Cells	50160
Total RAM Bits	2475072
Number of I/O	514
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1agx50df1152i6n

- Main device features:
  - TriMatrix memory consisting of three RAM block sizes to implement true dual-port memory and first-in first-out (FIFO) buffers with performance up to 380 MHz
  - Up to 16 global clock networks with up to 32 regional clock networks per device
  - High-speed DSP blocks provide dedicated implementation of multipliers, multiply-accumulate functions, and finite impulse response (FIR) filters
  - Up to four enhanced phase-locked loops (PLLs) per device provide spread spectrum, programmable bandwidth, clock switch-over, and advanced multiplication and phase shifting
  - Support for numerous single-ended and differential I/O standards
  - High-speed source-synchronous differential I/O support on up to 47 channels
  - Support for source-synchronous bus standards, including SPI-4 Phase 2 (POS-PHY Level 4), SFI-4.1, XSBI, UTOPIA IV, NPSI, and CSIX-L1
  - Support for high-speed external memory including DDR and DDR2 SDRAM, and SDR SDRAM
  - Support for multiple intellectual property megafunctions from Altera® MegaCore® functions and Altera Megafunction Partners Program (AMPP℠)
  - Support for remote configuration updates

Table 1–1 lists Arria GX device features for FineLine BGA (FBGA) with flip chip packages.

Table 1–1. Arria GX Device Features (Part 1 of 2)

Feature	EP1AGX20C	EP1AGX35C/D		EP1AGX50C/D		EP1AGX60C/D/E			EP1AGX90E
	C	C	D	C	D	C	D	E	E
Package	484-pin, 780-pin (Flip chip)	484-pin (Flip chip)	780-pin (Flip chip)	484-pin (Flip chip)	780-pin, 1152-pin (Flip chip)	484-pin (Flip chip)	780-pin (Flip chip)	1152-pin (Flip chip)	1152-pin (Flip chip)
ALMs	8,632	13,408		20,064		24,040			36,088
Equivalent logic elements (LEs)	21,580	33,520		50,160		60,100			90,220
Transceiver channels	4	4	8	4	8	4	8	12	12
Transceiver data rate	600 Mbps to 3.125 Gbps	600 Mbps to 3.125 Gbps		600 Mbps to 3.125 Gbps		600 Mbps to 3.125 Gbps			600 Mbps to 3.125 Gbps
Source-synchronous receive channels	31	31	31	31	31, 42	31	31	42	47

Figure 2–7 shows the serializer block diagram.

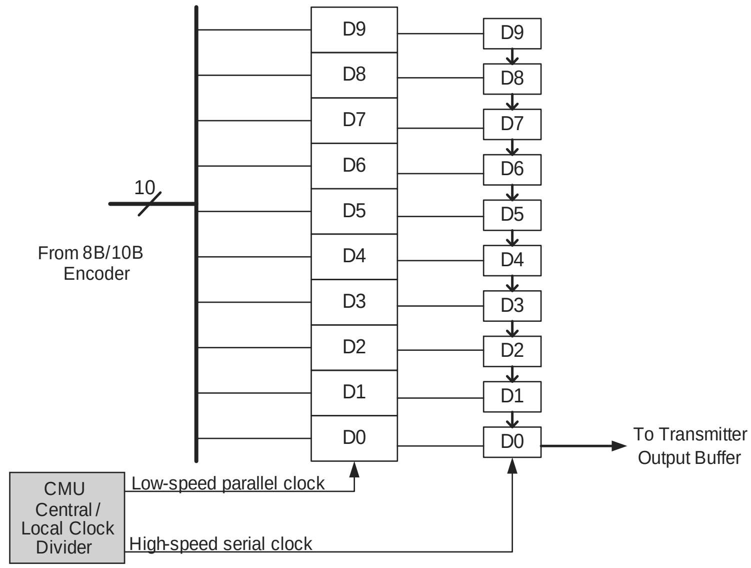


Figure 2–7. Serializer

Transmitter Buffer

The Arria GX transceiver buffers support the 1.2- and 1.5-V PCML I/O standard at rates up to 3.125 Gbps. The common mode voltage (V_{CM}) of the output driver may be set to 600 or 700 mV.

For more information about the Arria GX transceiver buffers, refer to the *Arria GX Transceiver Architecture* chapter.

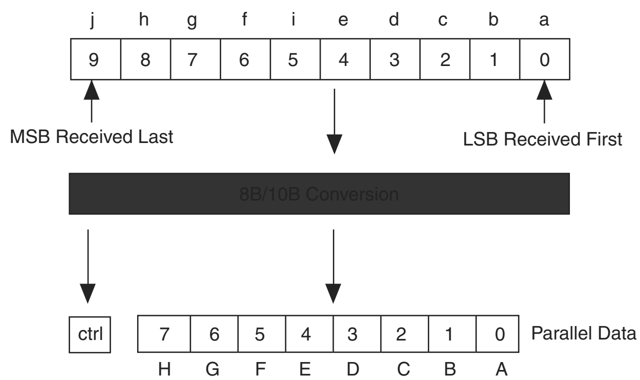
The output buffer, as shown in Figure 2–8, is directly driven by the high-speed data serializer and consists of a programmable output driver, a programmable pre-emphasis circuit, and OCT circuitry.

8B/10B Decoder

The 8B/10B decoder is used in all supported functional modes. The 8B/10B decoder takes in 10-bit data from the rate matcher and decodes it into 8-bit data + 1-bit control identifier, thereby restoring the original transmitted data at the receiver. The 8B/10B decoder indicates whether the received 10-bit character is a data or control code through the `rx_ctrldetect` port. If the received 10-bit code group is a control character (`Kx.y`), the `rx_ctrldetect` signal is driven high and if it is a data character (`Dx.y`), the `rx_ctrldetect` signal is driven low.

Figure 2–17 shows a 10-bit code group decoded to an 8-bit data and a 1-bit control indicator.

Figure 2–17. 10-Bit to 8-Bit Conversion



If the received 10-bit code is not a part of valid Dx.y or Kx.y code groups, the 8B/10B decoder block asserts an error flag on the `rx_errdetect` port. If the received 10-bit code is detected with incorrect running disparity, the 8B/10B decoder block asserts an error flag on the `rx_disperr` and `rx_errdetect` ports. The error flag signals (`rx_errdetect` and `rx_disperr`) have the same data path delay from the 8B/10B decoder to the PLD-transceiver interface as the bad code group.

Receiver State Machine

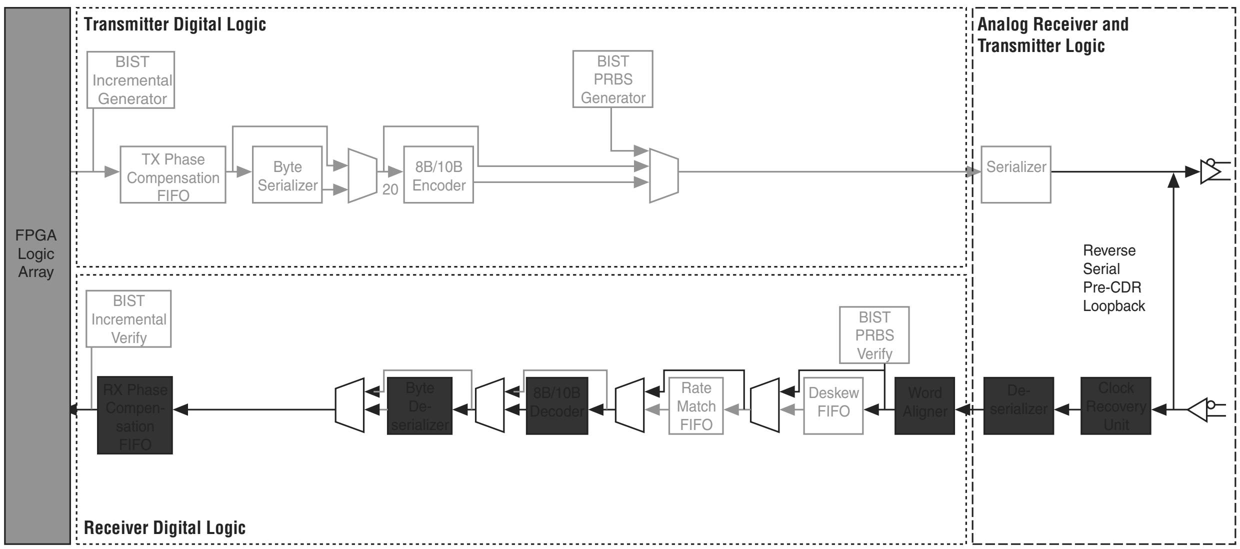
The receiver state machine operates in Basic, GIGE, PCI Express (PIPE), and XAUI modes. In GIGE mode, the receiver state machine replaces invalid code groups with K30.7. In XAUI mode, the receiver state machine translates the XAUI PCS code group to the XAUI XGMII code group.

Reverse Serial Pre-CDR Loopback

Reverse serial pre-CDR loopback mode uses the analog portion of the transceiver. An external source (pattern generator or transceiver) generates the source data. The high-speed serial source data arrives at the high-speed differential receiver input buffer, loops back before the CRU unit, and is transmitted though the high-speed differential transmitter output buffer. It is for test or verification use only to verify the signal being received after the gain and equalization improvements of the input buffer. The signal at the output is not exactly what is received because the signal goes through the output buffer and the V_{OD} is changed to the V_{OD} setting level. Pre-emphasis settings have no effect.

Figure 2–20 shows the Arria GX block in reverse serial pre-CDR loopback mode.

Figure 2–20. Arria GX Block in Reverse Serial Pre-CDR Loopback Mode



PCI Express (PIPE) Reverse Parallel Loopback

Figure 2–21 shows the data path for PCI Express (PIPE) reverse parallel loopback. The reverse parallel loopback configuration is compliant with the PCI Express (PIPE) specification and is available only on PCI Express (PIPE) mode.

Figure 2–21. PCI Express (PIPE) Reverse Parallel Loopback

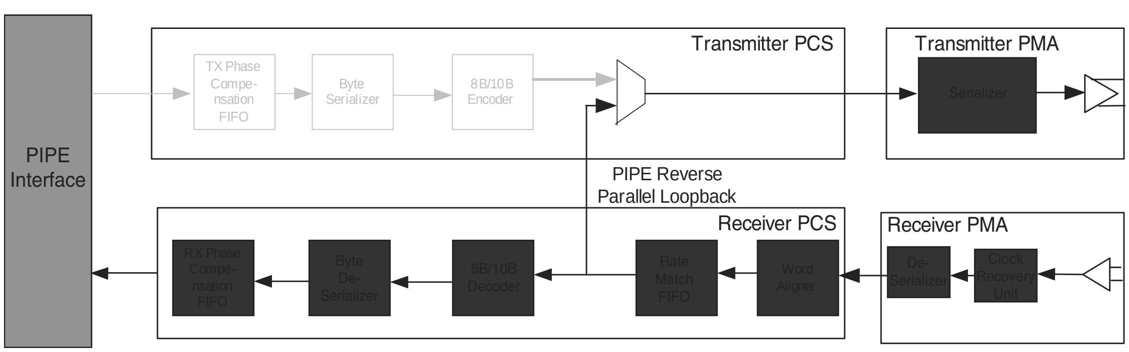
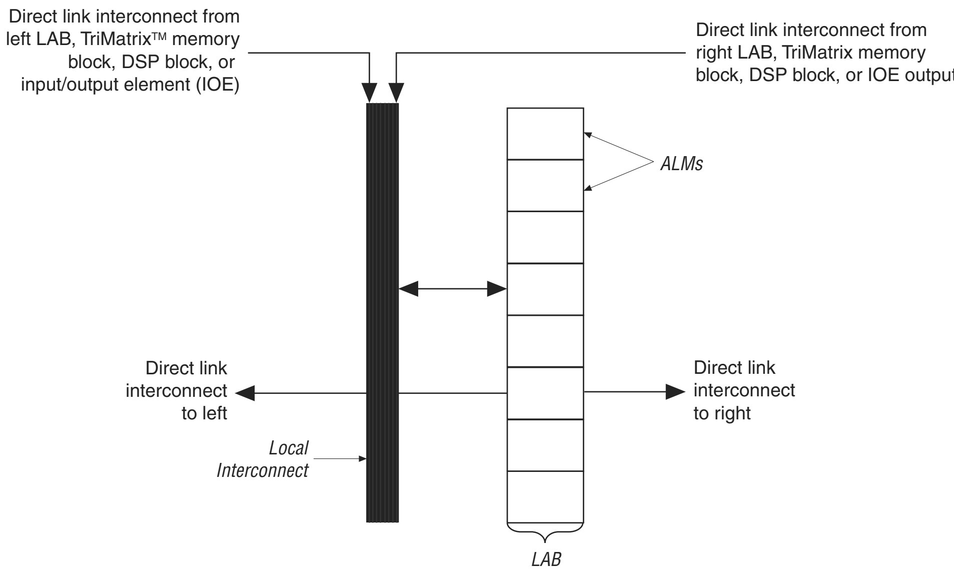


Figure 2–26 shows the direct link connection.

Figure 2–26. Direct Link Connection



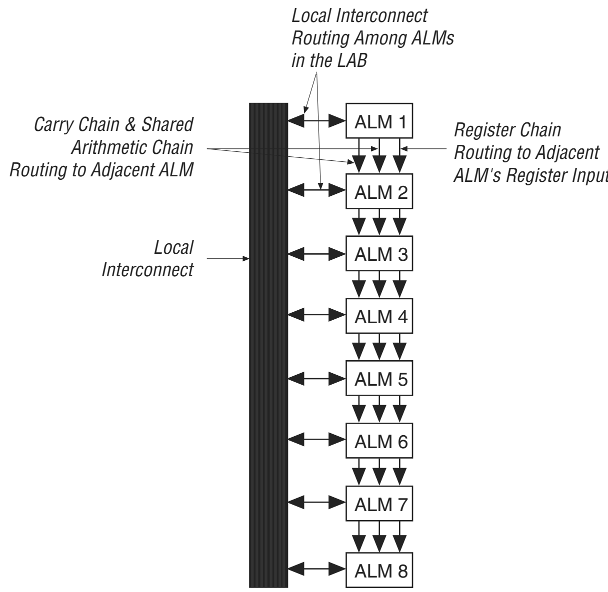
LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its ALMs. The control signals include three clocks, three clock enables, two asynchronous clears, synchronous clear, asynchronous preset or load, and synchronous load control signals, providing a maximum of 11 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use three clocks and three clock enable signals. However, there can only be up to two unique clocks per LAB, as shown in the LAB control signal generation circuit in Figure 2–27. Each LAB's clock and clock enable signals are linked. For example, any ALM in a particular LAB using the `labclk1` signal also uses `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses two LAB-wide clock signals. De-asserting the clock enable signal turns off the corresponding LAB-wide clock. Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. The asynchronous load acts as a preset when the asynchronous load data input is tied high. When the asynchronous load/preset signal is used, the `labclkena0` signal is no longer available.

The LAB row clocks `[5..0]` and LAB local interconnect generate the LAB-wide control signals. The MultiTrack interconnects have inherently low skew. This low skew allows the MultiTrack interconnects to distribute clock and control signals in addition to data.

Figure 2–40. Shared Arithmetic Chain, Carry Chain and Register Chain Interconnects



C4 interconnects span four LABs, M512, or M4K blocks up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. Figure 2–41 shows the C4 interconnect connections from a LAB in a column. C4 interconnects can drive and be driven by all types of architecture blocks, including DSP blocks, TriMatrix memory blocks, and column and row IOEs. For LAB interconnection, a primary LAB or its LAB neighbor can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

Table 2–13. DSP Blocks in Arria GX Devices *(Note 1)*

Device	DSP Blocks	Total 9 × 9 Multipliers	Total 18 × 18 Multipliers	Total 36 × 36 Multipliers
EP1AGX20	10	80	40	10
EP1AGX35	14	112	56	14
EP1AGX50	26	208	104	26
EP1AGX60	32	256	128	32
EP1AGX90	44	352	176	44

Note to Table 2–13:

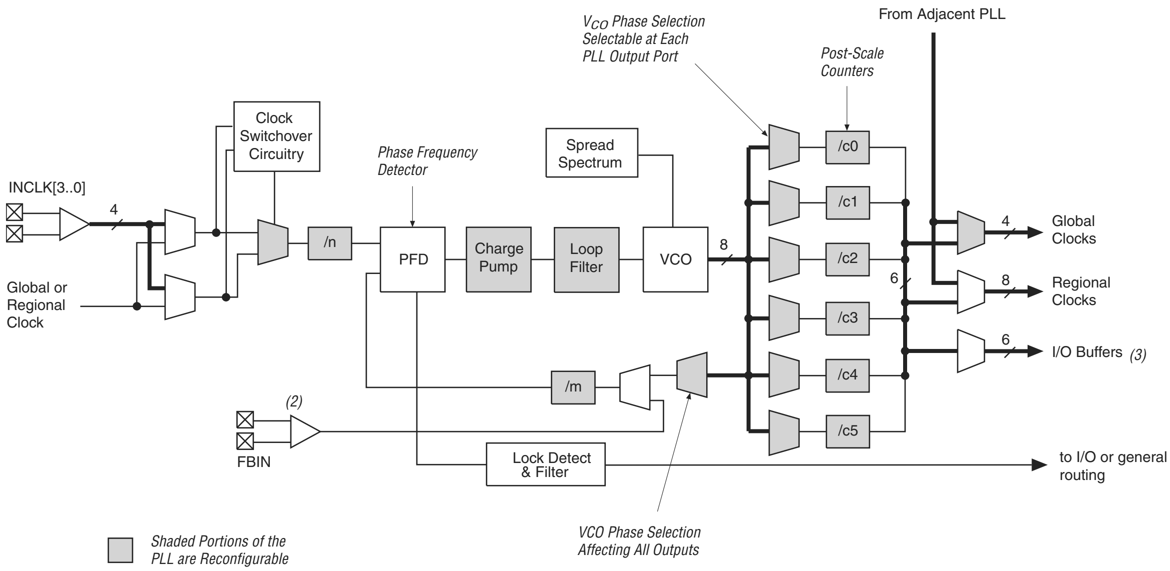
(1) This list only shows functions that can fit into a single DSP block. Multiple DSP blocks can support larger multiplication functions.

Additionally, DSP block input registers can efficiently implement shift registers for FIR filter applications. DSP blocks support Q1.15 format rounding and saturation. Figure 2–51 shows a top-level diagram of the DSP block configured for 18 × 18-bit multiplier mode.

Enhanced PLLs

Arria GX devices contain up to four enhanced PLLs with advanced clock management features. These features include support for external clock feedback mode, spread-spectrum clocking, and counter cascading. Figure 2–65 shows a diagram of the enhanced PLL.

Figure 2–65. Arria GX Enhanced PLL *(Note 1)*



Notes to Figure 2–65:

(1) Each clock source can come from any of the four clock pins that are physically located on the same side of the device as the PLL.

(2) If the feedback input is used, you will lose one (or two, if FBIN is differential) external clock output pin.

(3) Each enhanced PLL has three differential external clock outputs or six single-ended external clock outputs.

(4) The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal cannot drive the PLL.

Fast PLLs

Arria GX devices contain up to four fast PLLs with high-speed serial interfacing ability. Fast PLLs offer high-speed outputs to manage the high-speed differential I/O interfaces. Figure 2–66 shows a diagram of the fast PLL.

Table 4–6. Arria GX Transceiver Block AC Specification (Part 3 of 3)

Symbol / Description	Conditions	–6 Speed Grade Commercial and Industrial			Units
		Min	Typ	Max	
Transmitter PLL					
VCO frequency range	—	500	—	1562.5	MHz
Bandwidth at 3.125 Gbps	BW = Low	—	3	—	MHz
	BW = Med	—	5	—	
	BW = High	—	9	—	
Bandwidth at 2.5 Gbps	BW = Low	—	1	—	MHz
	BW = Med	—	2	—	
	BW = High	—	4	—	
TX PLL lock time from `gxb_powerdown` de-assertion *(9)*, *(14)*	—	—	—	100	us
PCS					
Interface speed per mode	—	25	—	156.25	MHz
Digital Reset Pulse Width	—	Minimum is 2 parallel clock cycles			—

Notes to Table 4–6:

(1) Spread spectrum clocking is allowed only in PCI Express (PIPE) mode if the upstream transmitter and the receiver share the same clock source.
(2) The reference clock DC coupling option is only available in PCI Express (PIPE) mode for the HCSL I/O standard.
(3) The `fixedclk` is used in PIPE mode receiver detect circuitry.
(4) The device cannot tolerate prolonged operation at this absolute maximum.
(5) The rate matcher supports only up to ± 300 PPM for PIPE mode and ± 100 PPM for GIGE mode.
(6) This parameter is measured by embedding the run length data in a PRBS sequence.
(7) Signal detect threshold detector circuitry is available only in PCI Express (PIPE mode).
(8) Time taken for `rx_pll_locked` to go high from `rx_analogreset` deassertion. Refer to Figure 4–1.
(9) For lock times specific to the protocols, refer to protocol characterization documents.
(10) Time for which the CDR needs to stay in LTR mode after `rx_pll_locked` is asserted and before `rx_locktodata` is asserted in manual mode. Refer to Figure 4–1.
(11) Time taken to recover valid data from GXB after the `rx_locktodata` signal is asserted in manual mode. Measurement results are based on PRBS31, for native data rates only. Refer to Figure 4–1.
(12) Time taken to recover valid data from GXB after the `rx_freqlocked` signal goes high in automatic mode. Measurement results are based on PRBS31, for native data rates only. Refer to Figure 4–2.
(13) This is applicable only to PCI Express (PIPE) ×4 and XAUI ×4 mode.
(14) Time taken to lock `TX PLL` from `gxb_powerdown` deassertion.
(15) The 1.2 V RX VICM settings is intended for DC-coupled LVDS links.

Figure 4–1 shows the lock time parameters in manual mode. Figure 4–2 shows the lock time parameters in automatic mode.

☞ LTD = Lock to data
LTR = Lock to reference clock

Table 4–8 and Table 4–9 list the transmitter and receiver PCS latency for each mode, respectively.

Table 4–8. PCS Latency *(Note 1)*

Functional Mode	Configuration	Transmitter PCS Latency					
		TX PIPE	TX Phase Comp FIFO	Byte Serializer	TX State Machine	8B/10B Encoder	Sum *(2)*
XAUI	—	—	2–3	1	0.5	0.5	4–5
PIPE	×1, ×4, ×8 8-bit channel width	1	3–4	1	—	1	6–7
	×1, ×4, ×8 16-bit channel width	1	3–4	1	—	0.5	6–7
GIGE	—	—	2–3	1	—	1	4–5
Serial RapidIO	1.25 Gbps, 2.5 Gbps, 3.125 Gbps	—	2–3	1	—	0.5	4–5
SDI	HD10-bit channel width	—	2–3	1	—	1	4–5
	HD, 3G 20-bit channel width	—	2–3	1	—	0.5	4–5
BASIC Single Width	8-bit/10-bit channel width	—	2–3	1	—	1	4–5
	16-bit/20-bit channel width	—	2–3	1	—	0.5	4–5

Notes to Table 4–8:

(1) The latency numbers are with respect to the PLD-transceiver interface clock cycles.

(2) The total latency number is rounded off in the Sum column.

Table 4–9. PCS Latency (Part 1 of 2) (Part 1 of 2)

Functional Mode	Configuration	Receiver PCS Latency									
		Word Aligner	Deskew FIFO	Rate Matcher *(3)*	8B/10B Decoder	Receiver State Machine	Byte Deserializer	Byte Order	Receiver Phase Comp FIFO	Receiver PIPE	Sum *(2)*
XAUI	—	2–2.5	2–2.5	5.5–6.5	0.5	1	1	1	1–2	—	14–17
PIPE	×1, ×4 8-bit channel width	4–5	—	11–13	1	—	1	1	2–3	1	21–25
	×1, ×4 16-bit channel width	2–2.5	—	5.5–6.5	0.5	—	1	1	2–3	1	13–16
GIGE	—	4–5	—	11–13	1	—	1	1	1–2	—	19–23
Serial RapidIO	1.25 Gbps, 2.5 Gbps, 3.125 Gbps	2–2.5	—	—	0.5	—	1	1	1–2	—	6–7
SDI	HD 10-bit channel width	5	—	—	1	—	1	1	1–2	—	9–10
	HD, 3G 20-bit channel width	2.5	—	—	0.5	—	1	1	1–2	—	6–7

Table 4–14. Arria GX Device DC Operating Conditions (Part 2 of 2) *(Note 1)*

Symbol	Parameter	Conditions	Device	Min	Typ	Max	Units
R_{CONF} *(4)*	Value of I/O pin pull-up resistor before and during configuration	V_i = 0, V_{CCIO} = 3.3 V	—	10	25	50	kΩ
		V_i = 0, V_{CCIO} = 2.5 V	—	15	35	70	kΩ
		V_i = 0, V_{CCIO} = 1.8 V	—	30	50	100	kΩ
		V_i = 0, V_{CCIO} = 1.5 V	—	40	75	150	kΩ
		V_i = 0, V_{CCIO} = 1.2 V	—	50	90	170	kΩ
	Recommended value of I/O pin external pull-down resistor before and during configuration	—	—	—	1	2	kΩ

Notes to Table 4–14:

(1) Typical values are for T_A = 25 °C, V_{CCINT} = 1.2 V, and V_{CCIO} = 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

(2) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, 1.5, and 1.2 V).

(3) Maximum values depend on the actual TJ and design utilization. For maximum values, refer to the Excel-based PowerPlay Early Power Estimator (available at PowerPlay Early Power Estimators (EPE) and Power Analyzer) or the Quartus® II PowerPlay Power Analyzer feature for maximum values. For more information, refer to "Power Consumption" on page 4–25.

(4) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.

I/O Standard Specifications

Table 4–15 through Table 4–38 show the Arria GX device family I/O standard specifications.

Table 4–15. LVTTL Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO} *(1)*	Output supply voltage	—	3.135	3.465	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.3	0.8	V
V_{OH}	High-level output voltage	I_{OH} = –4 mA *(2)*	2.4	—	V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA *(2)*	—	0.45	V

Notes to Table 4–15:

(1) Arria GX devices comply to the narrow range for the supply voltage as specified in the EIA/JEDEC Standard, JESD8-B.

(2) This specification is supported across all the programmable drive strength settings available for this I/O standard.

Table 4–16. LVCMOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO} *(1)*	Output supply voltage	—	3.135	3.465	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.3	0.8	V
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, I_{OH} = –0.1 mA *(2)*	V_{CCIO} – 0.2	—	V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, I_{OL} = 0.1 mA *(2)*	—	0.2	V

Notes to Table 4–16:

(1) Arria GX devices comply to the narrow range for the supply voltage as specified in the EIA/JEDEC Standard, JESD8-B.

(2) This specification is supported across all the programmable drive strength available for this I/O standard.

Table 4–30. SSTL-2 Class II Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IL} (DC)	Low-level DC input voltage	—	–0.3	—	V_{REF} – 0.18	V
V_{IH} (AC)	High-level AC input voltage	—	V_{REF} + 0.35	—	—	V
V_{IL} (AC)	Low-level AC input voltage	—	—	—	V_{REF} – 0.35	V
V_{OH}	High-level output voltage	I_{OH} = –16.4 mA *(1)*	V_{TT} + 0.76	—	—	V
V_{OL}	Low-level output voltage	I_{OL} = 16.4 mA *(1)*	—	—	V_{TT} – 0.76	V

Note to Table 4–30:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Arria GX Architecture* chapter.

Table 4–31. SSTL-2 Class I & II Differential Specifications *(Note 1)*

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	2.375	2.5	2.625	V
V_{SWING} (DC)	DC differential input voltage	0.36	—	—	V
V_X (AC)	AC differential input cross point voltage	(V_{CCIO}/2) – 0.2	—	(V_{CCIO}/2) + 0.2	V
V_{SWING} (AC)	AC differential input voltage	0.7	—	—	V
V_{ISO}	Input clock signal offset voltage	—	0.5 V_{CCIO}	—	V
ΔV_{ISO}	Input clock signal offset voltage variation	—	200	—	mV
V_{OX} (AC)	AC differential output cross point voltage	(V_{CCIO}/2) – 0.2	—	(V_{CCIO}/2) + 0.2	V

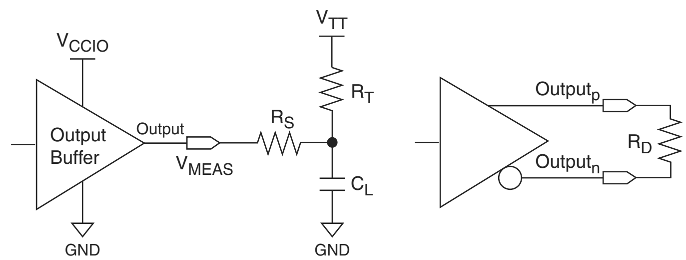
Note to Table 4–31:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Arria GX Architecture* chapter.

Table 4–32. 1.2-V HSTL Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	1.14	1.2	1.26	V
V_{REF}	Reference voltage	0.48 V_{CCIO}	0.5 V_{CCIO}	0.52 V_{CCIO}	V
V_{IH} (DC)	High-level DC input voltage	V_{REF} + 0.08	—	V_{CCIO} + 0.15	V
V_{IL} (DC)	Low-level DC input voltage	–0.15	—	V_{REF} – 0.08	V
V_{IH} (AC)	High-level AC input voltage	V_{REF} + 0.15	—	V_{CCIO} + 0.24	V
V_{IL} (AC)	Low-level AC input voltage	–0.24	—	V_{REF} – 0.15	V
V_{OH}	High-level output voltage	V_{REF} + 0.15	—	V_{CCIO} + 0.15	V
V_{OL}	Low-level output voltage	–0.15	—	V_{REF} – 0.15	V

Figure 4–7. Output Delay Timing Reporting Setup Modeled by Quartus II



Notes to Figure 4–7:

(1) Output pin timing is reported at the output pin of the FPGA device. Additional delays for loading and board trace delay need to be accounted for with IBIS model simulations.

(2) V_{CCPD} is 3.085 V unless otherwise specified.

(3) V_{CCINT} is 1.12 V unless otherwise specified.

Table 4–44. Output Timing Measurement Methodology for Output Pins *(Note 1), (2), (3)*

I/O Standard	Loading and Termination						Measurement Point
	R_S (Ω)	R_D (Ω)	R_T (Ω)	V_{CCIO} (V)	V_{TT} (V)	C_L (pF)	V_{MEAS} (V)
LVTTL *(4)*	—	—	—	3.135	—	0	1.5675
LVCMOS *(4)*	—	—	—	3.135	—	0	1.5675
2.5 V *(4)*	—	—	—	2.375	—	0	1.1875
1.8 V *(4)*	—	—	—	1.710	—	0	0.855
1.5 V *(4)*	—	—	—	1.425	—	0	0.7125
PCI *(5)*	—	—	—	2.970	—	10	1.485
PCI-X *(5)*	—	—	—	2.970	—	10	1.485
SSTL-2 Class I	25	—	50	2.325	1.123	0	1.1625
SSTL-2 Class II	25	—	25	2.325	1.123	0	1.1625
SSTL-18 Class I	25	—	50	1.660	0.790	0	0.83
SSTL-18 Class II	25	—	25	1.660	0.790	0	0.83
1.8-V HSTL Class I	—	—	50	1.660	0.790	0	0.83
1.8-V HSTL Class II	—	—	25	1.660	0.790	0	0.83
1.5-V HSTL Class I	—	—	50	1.375	0.648	0	0.6875
1.5-V HSTL Class II	—	—	25	1.375	0.648	0	0.6875
1.2-V HSTL with OCT	—	—	—	1.140	—	0	0.570
Differential SSTL-2 Class I	25	—	50	2.325	1.123	0	1.1625
Differential SSTL-2 Class II	25	—	25	2.325	1.123	0	1.1625
Differential SSTL-18 Class I	50	—	50	1.660	0.790	0	0.83
Differential SSTL-18 Class II	25	—	25	1.660	0.790	0	0.83
1.5-V differential HSTL Class I	—	—	50	1.375	0.648	0	0.6875
1.5-V differential HSTL Class II	—	—	25	1.375	0.648	0	0.6875
1.8-V differential HSTL Class I	—	—	50	1.660	0.790	0	0.83

Table 4–45. Timing Measurement Methodology for Input Pins *(Note 1)*, *(2)*, *(3)*, *(4)* (Part 2 of 2)

I/O Standard	Measurement Conditions			Measurement Point
	V_{CCIO} (V)	V_{REF} (V)	Edge Rate (ns)	VMEAS (V)
Differential SSTL-18 Class II	1.660	0.830	1.660	0.83
1.5-V differential HSTL Class I	1.375	0.688	1.375	0.6875
1.5-V differential HSTL Class II	1.375	0.688	1.375	0.6875
1.8-V differential HSTL Class I	1.660	0.830	1.660	0.83
1.8-V differential HSTL Class II	1.660	0.830	1.660	0.83
LVDS	2.325	—	0.100	1.1625
LVPECL	3.135	—	0.100	1.5675

Notes to Table 4–45:

(1) Input buffer sees no load at buffer input.

(2) Input measuring point at buffer input is 0.5 V_{CCIO}.

(3) Output measuring point is 0.5 V_{CC} at internal node.

(4) Input edge rate is 1 V/ns.

(5) Less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V with less than 30-mV ripple.

(6) V_{CCPD} = 2.97 V, less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V.

Clock Network Skew Adders

The Quartus II software models skew within dedicated clock networks such as global and regional clocks. Therefore, the intra-clock network skew adder is not specified. Table 4–46 specifies the intra clock skew between any two clock networks driving any registers in the Arria GX device.

Table 4–46. Clock Network Specifications

Name	Description	Min	Typ	Max	Units
Clock skew adder EP1AGX20/35 *(1)*	Inter-clock network, same side	—	—	± 50	ps
	Inter-clock network, entire chip	—	—	± 100	ps
Clock skew adder EP1AGX50/60 *(1)*	Inter-clock network, same side	—	—	± 50	ps
	Inter-clock network, entire chip	—	—	± 100	ps
Clock skew adder EP1AGX90 *(1)*	Inter-clock network, same side	—	—	± 55	ps
	Inter-clock network, entire chip	—	—	± 110	ps

Note to Table 4–46:

(1) This is in addition to intra-clock network skew, which is modeled in the Quartus II software.

Default Capacitive Loading of Different I/O Standards

See Table 4–47 for default capacitive loading of different I/O standards.

Table 4–47. Default Loading of Different I/O Standards for Arria GX Devices (Part 1 of 2)

I/O Standard	Capacitive Load	Units
LVTTL	0	pF
LVCMOS	0	pF
2.5 V	0	pF

Table 4–48. EP1AGX20 Row Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.117	0.117	0.273	ns
RCLK PLL input adder	0.011	0.011	0.019	ns
RCLK output adder	–0.117	–0.117	–0.273	ns
RCLK PLL output adder	–0.011	–0.011	–0.019	ns

Table 4–49 describes I/O timing specifications.

Table 4–49. EP1AGX20 Column Pins Input Timing Parameters (Part 1 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.251	1.251	2.915	ns
		t_H	–1.146	–1.146	–2.638	ns
	GCLK PLL	t_{SU}	2.693	2.693	6.021	ns
		t_H	–2.588	–2.588	–5.744	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.251	1.251	2.915	ns
		t_H	–1.146	–1.146	–2.638	ns
	GCLK PLL	t_{SU}	2.693	2.693	6.021	ns
		t_H	–2.588	–2.588	–5.744	ns
2.5 V	GCLK	t_{SU}	1.261	1.261	2.897	ns
		t_H	–1.156	–1.156	–2.620	ns
	GCLK PLL	t_{SU}	2.703	2.703	6.003	ns
		t_H	–2.598	–2.598	–5.726	ns
1.8 V	GCLK	t_{SU}	1.327	1.327	3.107	ns
		t_H	–1.222	–1.222	–2.830	ns
	GCLK PLL	t_{SU}	2.769	2.769	6.213	ns
		t_H	–2.664	–2.664	–5.936	ns
1.5 V	GCLK	t_{SU}	1.330	1.330	3.200	ns
		t_H	–1.225	–1.225	–2.923	ns
	GCLK PLL	t_{SU}	2.772	2.772	6.306	ns
		t_H	–2.667	–2.667	–6.029	ns
SSTL-2 CLASS I	GCLK	t_{SU}	1.075	1.075	2.372	ns
		t_H	–0.970	–0.970	–2.095	ns
	GCLK PLL	t_{SU}	2.517	2.517	5.480	ns
		t_H	–2.412	–2.412	–5.203	ns

Table 4–49. EP1AGX20 Column Pins Input Timing Parameters (Part 2 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
SSTL-2 CLASS II	GCLK	t_{SU}	1.075	1.075	2.372	ns
		t_H	–0.970	–0.970	–2.095	ns
	GCLK PLL	t_{SU}	2.517	2.517	5.480	ns
		t_H	–2.412	–2.412	–5.203	ns
SSTL-18 CLASS I	GCLK	t_{SU}	1.113	1.113	2.479	ns
		t_H	–1.008	–1.008	–2.202	ns
	GCLK PLL	t_{SU}	2.555	2.555	5.585	ns
		t_H	–2.450	–2.450	–5.308	ns
SSTL-18 CLASS II	GCLK	t_{SU}	1.114	1.114	2.479	ns
		t_H	–1.009	–1.009	–2.202	ns
	GCLK PLL	t_{SU}	2.556	2.556	5.587	ns
		t_H	–2.451	–2.451	–5.310	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	1.113	1.113	2.479	ns
		t_H	–1.008	–1.008	–2.202	ns
	GCLK PLL	t_{SU}	2.555	2.555	5.585	ns
		t_H	–2.450	–2.450	–5.308	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	1.114	1.114	2.479	ns
		t_H	–1.009	–1.009	–2.202	ns
	GCLK PLL	t_{SU}	2.556	2.556	5.587	ns
		t_H	–2.451	–2.451	–5.310	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.131	1.131	2.607	ns
		t_H	–1.026	–1.026	–2.330	ns
	GCLK PLL	t_{SU}	2.573	2.573	5.713	ns
		t_H	–2.468	–2.468	–5.436	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.132	1.132	2.607	ns
		t_H	–1.027	–1.027	–2.330	ns
	GCLK PLL	t_{SU}	2.574	2.574	5.715	ns
		t_H	–2.469	–2.469	–5.438	ns
3.3-V PCI	GCLK	t_{SU}	1.256	1.256	2.903	ns
		t_H	–1.151	–1.151	–2.626	ns
	GCLK PLL	t_{SU}	2.698	2.698	6.009	ns
		t_H	–2.593	–2.593	–5.732	ns
3.3-V PCI-X	GCLK	t_{SU}	1.256	1.256	2.903	ns
		t_H	–1.151	–1.151	–2.626	ns
	GCLK PLL	t_{SU}	2.698	2.698	6.009	ns
		t_H	–2.593	–2.593	–5.732	ns

Table 4–49. EP1AGX20 Column Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
LVDS	GCLK	t_{SU}	1.106	1.106	2.489	ns
		t_H	–1.001	–1.001	–2.212	ns
	GCLK PLL	t_{SU}	2.530	2.530	5.564	ns
		t_H	–2.425	–2.425	–5.287	ns

Table 4–50 describes I/O timing specifications.

Table 4–50. EP1AGX20 Row Pins output Timing Parameters (Part 1 of 2)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	2.904	2.904	6.699	ns
		GCLK PLL	t_{CO}	1.485	1.485	3.627	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.776	2.776	6.059	ns
		GCLK PLL	t_{CO}	1.357	1.357	2.987	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.720	2.720	6.022	ns
		GCLK PLL	t_{CO}	1.301	1.301	2.950	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.776	2.776	6.059	ns
		GCLK PLL	t_{CO}	1.357	1.357	2.987	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.670	2.670	5.753	ns
		GCLK PLL	t_{CO}	1.251	1.251	2.681	ns
2.5 V	4 mA	GCLK	t_{CO}	2.759	2.759	6.033	ns
		GCLK PLL	t_{CO}	1.340	1.340	2.961	ns
2.5 V	8 mA	GCLK	t_{CO}	2.656	2.656	5.775	ns
		GCLK PLL	t_{CO}	1.237	1.237	2.703	ns
2.5 V	12 mA	GCLK	t_{CO}	2.637	2.637	5.661	ns
		GCLK PLL	t_{CO}	1.218	1.218	2.589	ns
1.8 V	2 mA	GCLK	t_{CO}	2.829	2.829	7.052	ns
		GCLK PLL	t_{CO}	1.410	1.410	3.980	ns
1.8 V	4 mA	GCLK	t_{CO}	2.818	2.818	6.273	ns
		GCLK PLL	t_{CO}	1.399	1.399	3.201	ns
1.8 V	6 mA	GCLK	t_{CO}	2.707	2.707	5.972	ns
		GCLK PLL	t_{CO}	1.288	1.288	2.900	ns
1.8 V	8 mA	GCLK	t_{CO}	2.676	2.676	5.858	ns
		GCLK PLL	t_{CO}	1.257	1.257	2.786	ns
1.5 V	2 mA	GCLK	t_{CO}	2.789	2.789	6.551	ns
		GCLK PLL	t_{CO}	1.370	1.370	3.479	ns
1.5 V	4 mA	GCLK	t_{CO}	2.682	2.682	5.950	ns
		GCLK PLL	t_{CO}	1.263	1.263	2.878	ns

Table 4–59 lists column pin delay adders when using the regional clock in Arria GX devices.

Table 4–59. EP1AGX35 Column Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
`RCLK` input adder	0.099	0.099	0.254	ns
`RCLK` PLL input adder	–0.012	–0.012	–0.01	ns
`RCLK` output adder	–0.086	–0.086	–0.244	ns
`RCLK` PLL output adder	1.253	1.253	3.133	ns

EP1AGX50 I/O Timing Parameters

Table 4–60 through Table 4–63 list the maximum I/O timing parameters for EP1AGX50 devices for I/O standards which support general purpose I/O pins.

Table 4–60 lists I/O timing specifications.

Table 4–60. EP1AGX50 Row Pins Input Timing Parameters (Part 1 of 2)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	`GCLK`	t_{SU}	1.550	1.550	3.542	ns
		t_H	–1.445	–1.445	–3.265	ns
	`GCLK PLL`	t_{SU}	2.978	2.978	6.626	ns
		t_H	–2.873	–2.873	–6.349	ns
3.3-V LVCMOS	`GCLK`	t_{SU}	1.550	1.550	3.542	ns
		t_H	–1.445	–1.445	–3.265	ns
	`GCLK PLL`	t_{SU}	2.978	2.978	6.626	ns
		t_H	–2.873	–2.873	–6.349	ns
2.5 V	`GCLK`	t_{SU}	1.562	1.562	3.523	ns
		t_H	–1.457	–1.457	–3.246	ns
	`GCLK PLL`	t_{SU}	2.990	2.990	6.607	ns
		t_H	–2.885	–2.885	–6.330	ns
1.8 V	`GCLK`	t_{SU}	1.628	1.628	3.730	ns
		t_H	–1.523	–1.523	–3.453	ns
	`GCLK PLL`	t_{SU}	3.056	3.056	6.814	ns
		t_H	–2.951	–2.951	–6.537	ns
1.5 V	`GCLK`	t_{SU}	1.631	1.631	3.825	ns
		t_H	–1.526	–1.526	–3.548	ns
	`GCLK PLL`	t_{SU}	3.059	3.059	6.909	ns
		t_H	–2.954	–2.954	–6.632	ns

Table 4–73. EP1AGX90 Column Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
1.5-V HSTL CLASS II	GCLK	t_{SU}	0.901	0.901	1.986	ns
		t_H	–0.796	–0.796	–1.709	ns
	GCLK PLL	t_{SU}	2.965	2.965	6.121	ns
		t_H	–2.860	–2.860	–5.844	ns
3.3-V PCI	GCLK	t_{SU}	1.023	1.023	2.278	ns
		t_H	–0.918	–0.918	–2.001	ns
	GCLK PLL	t_{SU}	3.087	3.087	6.413	ns
		t_H	–2.982	–2.982	–6.136	ns
3.3-V PCI-X	GCLK	t_{SU}	1.023	1.023	2.278	ns
		t_H	–0.918	–0.918	–2.001	ns
	GCLK PLL	t_{SU}	3.087	3.087	6.413	ns
		t_H	–2.982	–2.982	–6.136	ns
LVDS	GCLK	t_{SU}	0.891	0.891	1.920	ns
		t_H	–0.786	–0.786	–1.643	ns
	GCLK PLL	t_{SU}	2.963	2.963	6.066	ns
		t_H	–2.858	–2.858	–5.789	ns

Table 4–74 lists I/O timing specifications.

Table 4–74. EP1AGX90 Row Pins Output Timing Parameters (Part 1 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	3.170	3.170	7.382	ns
		GCLK PLL	t_{CO}	1.099	1.099	3.238	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	3.042	3.042	6.742	ns
		GCLK PLL	t_{CO}	0.971	0.971	2.598	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.986	2.986	6.705	ns
		GCLK PLL	t_{CO}	0.915	0.915	2.561	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	3.042	3.042	6.742	ns
		GCLK PLL	t_{CO}	0.971	0.971	2.598	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.936	2.936	6.436	ns
		GCLK PLL	t_{CO}	0.865	0.865	2.292	ns
2.5 V	4 mA	GCLK	t_{CO}	3.025	3.025	6.716	ns
		GCLK PLL	t_{CO}	0.954	0.954	2.572	ns
2.5 V	8 mA	GCLK	t_{CO}	2.922	2.922	6.458	ns
		GCLK PLL	t_{CO}	0.851	0.851	2.314	ns
2.5 V	12 mA	GCLK	t_{CO}	2.903	2.903	6.344	ns
		GCLK PLL	t_{CO}	0.832	0.832	2.200	ns

Table 4–99 lists performance notes.

Table 4–99. Arria GX Performance Notes

Applications		Resources Used			Performance
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	–6 Speed Grade
LE	16-to-1 multiplexer	5	0	0	168.41
	32-to-1 multiplexer	11	0	0	334.11
	16-bit counter	16	0	0	374.0
	64-bit counter	64	0	0	168.41
TriMatrix Memory M512 block	Simple dual-port RAM 32 x 18 bit	0	1	0	348.0
	FIFO 32 x 18 bit	0	1	0	333.22
TriMatrix Memory M4K block	Simple dual-port RAM 128 x 36 bit	0	1	0	344.71
	True dual-port RAM 128 x 18 bit	0	1	0	348.0
TriMatrix Memory MegaRAM block	Single port RAM 4K x 144 bit	0	2	0	244.0
	Simple dual-port RAM 4K x 144 bit	0	1	0	292.0
	True dual-port RAM 4K x 144 bit	0	2	0	244.0
	Single port RAM 8K x 72 bit	0	1	0	247.0
	Simple dual-port RAM 8K x 72 bit	0	1	0	292.0
	Single port RAM 16K x 36 bit	0	1	0	254.0
	Simple dual-port RAM 16K x 36 bit	0	1	0	292.0
	True dual-port RAM 16K x 36 bit	0	1	0	251.0
	Single port RAM 32K x 18 bit	0	1	0	317.36
	Simple dual-port RAM 32K x 18 bit	0	1	0	292.0
	True dual-port RAM 32K x 18 bit	0	1	0	251.0
	Single port RAM 64K x 9 bit	0	1	0	254.0
	Simple dual-port RAM 64K x 9 bit	0	1	0	292.0
	True dual-port RAM 64K x 9 bit	0	1	0	251.0