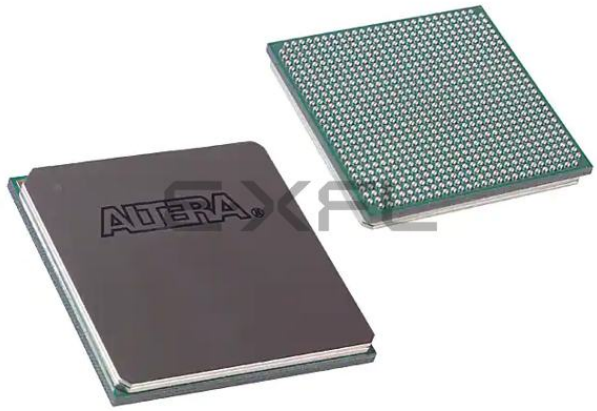

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2508
Number of Logic Elements/Cells	50160
Total RAM Bits	2475072
Number of I/O	350
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	780-BBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1agx50df780c6

AGX51002-2.0

Transceivers

Arria® GX devices incorporate up to 12 high-speed serial transceiver channels that build on the success of the Stratix® II GX device family. Arria GX transceivers are structured into full-duplex (transmitter and receiver) four-channel groups called transceiver blocks located on the right side of the device. You can configure the transceiver blocks to support the following serial connectivity protocols (functional modes):

- PCI Express (PIPE)
- Gigabit Ethernet (GIGE)
- XAUI
- Basic (600 Mbps to 3.125 Gbps)
- SDI (HD, 3G)
- Serial RapidIO (1.25 Gbps, 2.5 Gbps, 3.125 Gbps)

Transceivers within each block are independent and have their own set of dividers. Therefore, each transceiver can operate at different frequencies. Each block can select from two reference clocks to provide two clock domains that each transceiver can select from.

Table 2–1 lists the number of transceiver channels for each member of the Arria GX family.

Table 2–1. Arria GX Transceiver Channels

Device	Number of Transceiver Channels
EP1AGX20C	4
EP1AGX35C	4
EP1AGX35D	8
EP1AGX50C	4
EP1AGX50D	8
EP1AGX60C	4
EP1AGX60D	8
EP1AGX60E	12
EP1AGX90E	12

Transmit State Machine

The transmit state machine operates in either PCI Express (PIPE) mode, XAUI mode, or GIGE mode, depending on the protocol used.

GIGE Mode

In GIGE mode, the transmit state machine converts all idle ordered sets (/K28.5/, /Dx.y/) to either /I1/ or /I2/ ordered sets. The /I1/ set consists of a negative-ending disparity /K28.5/ (denoted by /K28.5/-), followed by a neutral /D5.6/. The /I2/ set consists of a positive-ending disparity /K28.5/ (denoted by /K28.5/+) and a negative-ending disparity /D16.2/ (denoted by /D16.2/-). The transmit state machines do not convert any of the ordered sets to match /C1/ or /C2/, which are the configuration ordered sets. (/C1/ and /C2/ are defined by [/K28.5/, /D21.5/] and [/K28.5/, /D2.2/], respectively). Both the /I1/ and /I2/ ordered sets guarantee a negative-ending disparity after each ordered set.

XAUI Mode

The transmit state machine translates the XAUI XGMII code group to the XAUI PCS code group. Table 2–3 lists the code conversion.

Table 2–3. On-Chip Termination Support by I/O Banks

XGMII TXC	XGMII TXD	PCS Code-Group	Description
0	00 through FF	Dxx.y	Normal data
1	07	K28.0 or K28.3 or K28.5	Idle in ||I||
1	07	K28.5	Idle in ||T||
1	9C	K28.4	Sequence
1	FB	K27.7	Start
1	FD	K29.7	Terminate
1	FE	K30.7	Error
1	Refer to IEEE 802.3 reserved code groups	Refer to IEEE 802.3 reserved code groups	Reserved code groups
1	Other value	K30.7	Invalid XGMII character

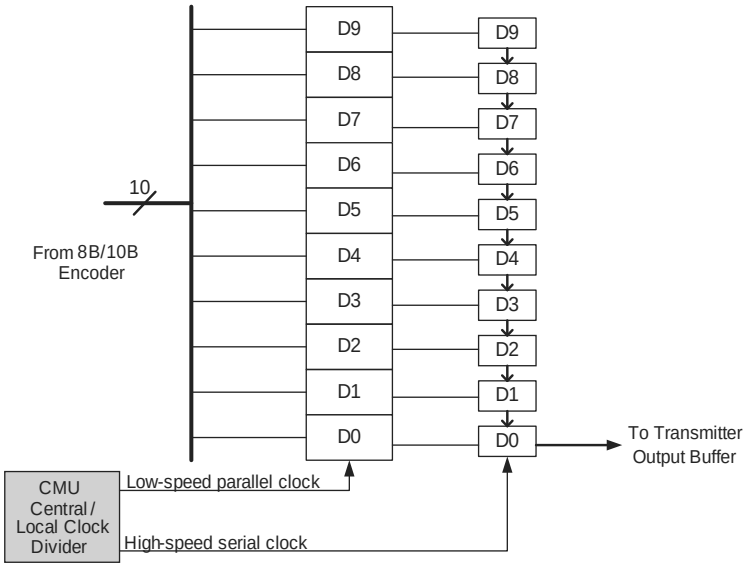
The XAUI PCS idle code groups, /K28.0/ (/R/) and /K28.5/ (/K/), are automatically randomized based on a PRBS7 pattern with an $\times 7 + \times 6 + 1$ polynomial. The /K28.3/ (/A/) code group is automatically generated between 16 and 31 idle code groups. The idle randomization on the /A/, /K/, and /R/ code groups is automatically done by the transmit state machine.

Serializer (Parallel-to-Serial Converter)

The serializer block clocks in 8- or 10-bit encoded data from the 8B/10B encoder using the low-speed parallel clock and clocks out serial data using the high-speed serial clock from the central or local clock divider blocks. The serializer feeds the data LSB to MSB to the transmitter output buffer.

Figure 2–7 shows the serializer block diagram.

Figure 2–7. Serializer



Transmitter Buffer

The Arria GX transceiver buffers support the 1.2- and 1.5-V PCML I/O standard at rates up to 3.125 Gbps. The common mode voltage (V_{CM}) of the output driver may be set to 600 or 700 mV.

For more information about the Arria GX transceiver buffers, refer to the *Arria GX Transceiver Architecture* chapter.

The output buffer, as shown in Figure 2–8, is directly driven by the high-speed data serializer and consists of a programmable output driver, a programmable pre-emphasis circuit, and OCT circuitry.

For more information about transceiver clocking in all supported functional modes, refer to the *Arria GX Transceiver Architecture* chapter.

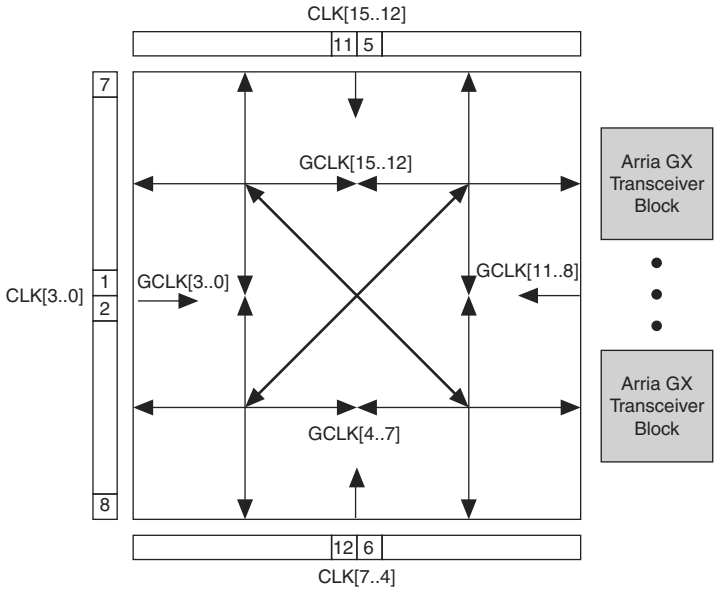
PLD Clock Utilization by Transceiver Blocks

Arria GX devices have up to 16 global clock (GCLK) lines and 16 regional clock (RCLK) lines that are used to route the transceiver clocks. The following transceiver clocks use the available global and regional clock resources:

- `pll_inclk` (if driven from an FPGA input pin)
- `rx_cruclk` (if driven from an FPGA input pin)
- `tx_clkout/coreclkout` (CMU low-speed parallel clock forwarded to the PLD)
- Recovered clock from each channel (`rx_clkout`) in non-rate matcher mode
- Calibration clock (`cal_blk_clk`)
- Fixed clock (`fixedclk` used for receiver detect circuitry in PCI Express [PIPE] mode only)

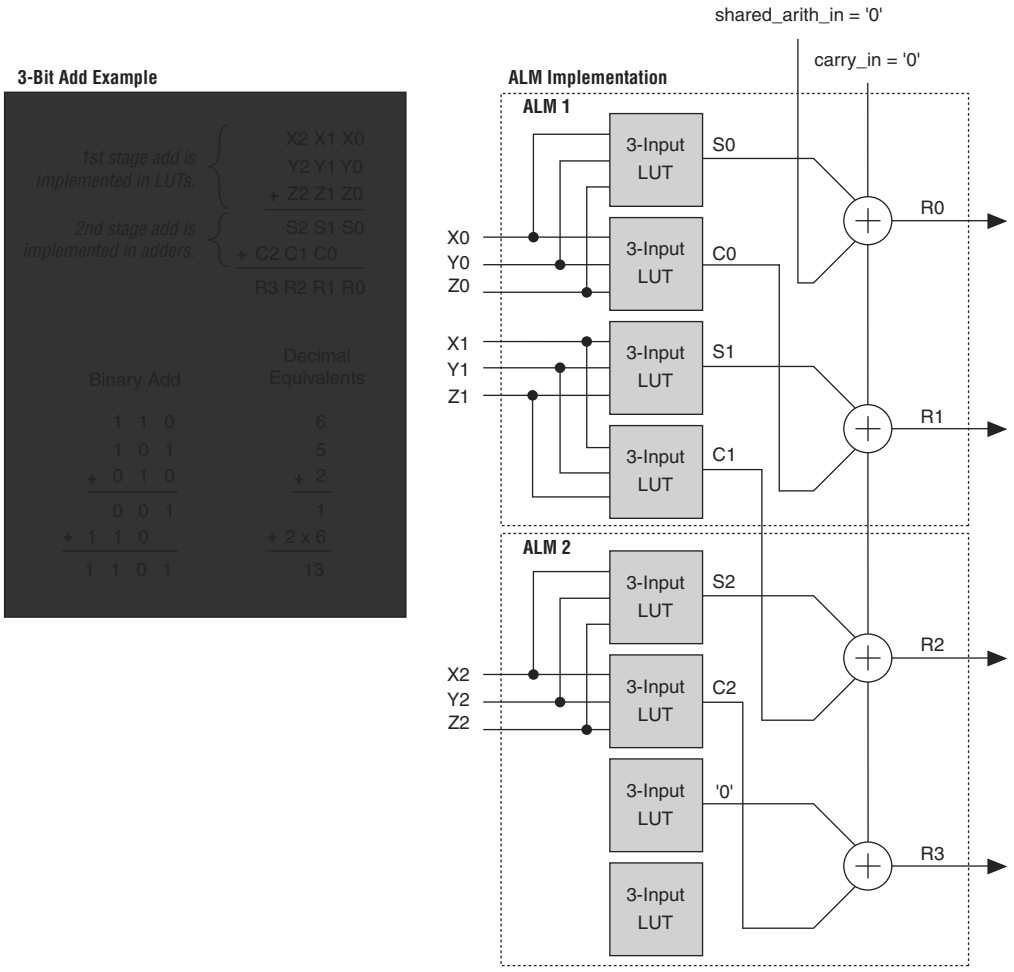
Figure 2–23 and Figure 2–24 show the available GCLK and RCLK resources in Arria GX devices.

Figure 2–23. Global Clock Resources in Arria GX Devices



Adder trees are used in many different applications. For example, the summation of partial products in a logic-based multiplier can be implemented in a tree structure. Another example is a correlator function that can use a large adder tree to sum filtered data samples in a given time frame to recover or to de-spread data which was transmitted utilizing spread spectrum technology. An example of a three-bit add operation utilizing the shared arithmetic mode is shown in Figure 2–37. The partial sum (`S[2..0]`) and the partial carry (`C[2..0]`) is obtained using LUTs, while the result (`R[2..0]`) is computed using dedicated adders.

Figure 2–37. Example of a 3-Bit Add Utilizing Shared Arithmetic Mode



Shared Arithmetic Chain

In addition to dedicated carry chain routing, the shared arithmetic chain available in shared arithmetic mode allows the ALM to implement a three-input add, which significantly reduces the resources necessary to implement large adder trees or correlator functions. Shared arithmetic chains can begin in either the first or fifth ALM in a LAB. The Quartus II Compiler automatically links LABs to create shared arithmetic chains longer than 16 (eight ALMs in arithmetic or shared arithmetic mode). For enhanced fitting, a long shared arithmetic chain runs vertically allowing fast horizontal connections to TriMatrix memory and DSP blocks. A shared arithmetic chain can continue as far as a full column. Similar to carry chains, shared arithmetic

Figure 2–52 and Figure 2–53 show the DSP block interfaces to LAB rows.

Figure 2–52. DSP Block Interconnect Interface

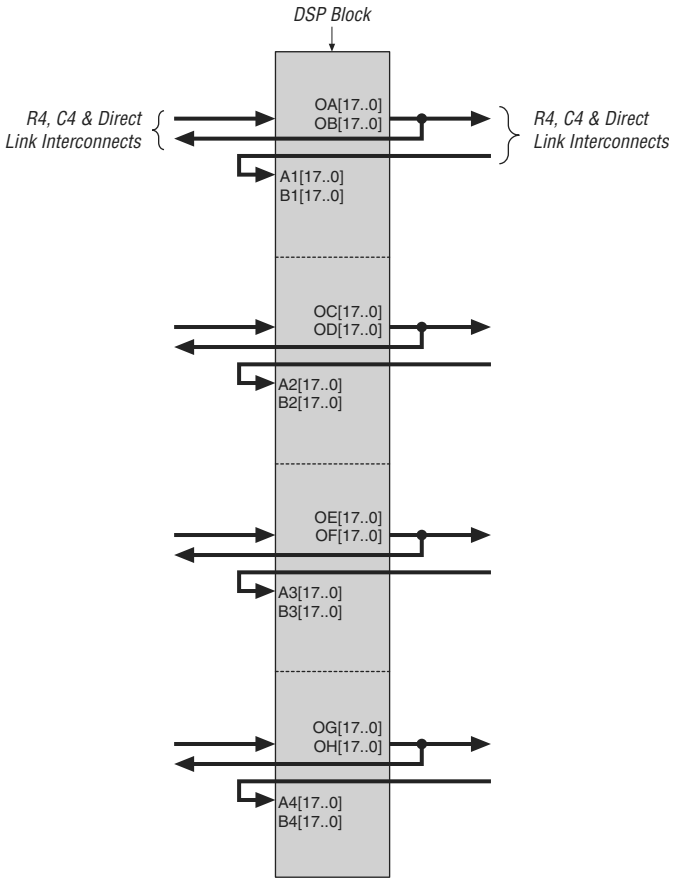
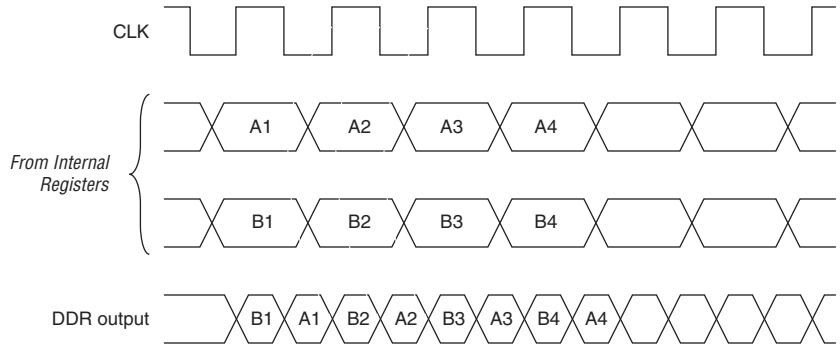


Table 2–15. DSP Block Signal Sources and Destinations

LAB Row at Interface	Control Signals Generated	Data Inputs	Data Outputs
0	clock0 aclr0 ena0 mult01_saturate addnsub1_round/ accum_round addnsub1 signa sourcea sourceb	A1[17..0] B1[17..0]	OA[17..0] OB[17..0]
1	clock1 aclr1 ena1 accum_saturate mult01_round accum_sload sourcea sourceb mode0	A2[17..0] B2[17..0]	OC[17..0] OD[17..0]
2	clock2 aclr2 ena2 mult23_saturate addnsub3_round/ accum_round addnsub3 sign_b sourcea sourceb	A3[17..0] B3[17..0]	OE[17..0] OF[17..0]
3	clock3 aclr3 ena3 accum_saturate mult23_round accum_sload sourcea sourceb mode1	A4[17..0] B4[17..0]	OG[17..0] OH[17..0]

Figure 2–76. Output Timing Diagram in DDR Mode



The Arria GX IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations. The negative-edge-clocked OE register holds the OE signal inactive until the falling edge of the clock to meet DDR SDRAM timing requirements.

External RAM Interfacing

In addition to the six I/O registers in each IOE, Arria GX devices also have dedicated phase-shift circuitry for interfacing with external memory interfaces, including DDR, DDR2 SDRAM, and SDR SDRAM. In every Arria GX device, the I/O banks at the top (Banks 3 and 4) and bottom (Banks 7 and 8) of the device support DQ and DQS signals with DQ bus modes of ×4, ×8/×9, ×16/×18, or ×32/×36. Table 2–23 shows the number of DQ and DQS buses that are supported per device.

Table 2–23. DQS and DQ Bus Mode Support *(Note 1)*

Device	Package	Number of ×4 Groups	Number of ×8/×9 Groups	Number of ×16/×18 Groups	Number of ×32/×36 Groups
EP1AGX20	484-pin FineLine BGA	2	0	0	0
EP1AGX35	484-pin FineLine BGA	2	0	0	0
	780-pin FineLine BGA	18	8	4	0
EP1AGX50/60	484-pin FineLine BGA	2	0	0	0
	780-pin FineLine BGA	18	8	4	0
	1,152-pin FineLine BGA	36	18	8	4
EP1AGX90	1,152-pin FineLine BGA	36	18	8	4

Note to Table 2–23:

(1) Numbers are preliminary until devices are available.

A compensated delay element on each DQS pin automatically aligns input DQS synchronization signals with the data window of their corresponding DQ data signals. The DQS signals drive a local DQS bus in the top and bottom I/O banks. This DQS bus is an additional resource to the I/O clocks and is used to clock DQ input registers with the DQS signal.

device, PLL 1 can drive a maximum of 16 transmitter channels in I/O Bank 2 or a maximum of 29 transmitter channels in I/O Banks 1 and 2. The Quartus II software can also merge receiver and transmitter PLLs when a receiver is driving a transmitter. In this case, one fast PLL can drive both the maximum numbers of receiver and transmitter channels.

For more information, refer to the "Differential Pin Placement Guidelines" section in the *High-Speed Differential I/O Interfaces with DPA in Arria GX Devices* chapter.

Table 2–30. EP1AGX20 Device Differential Channels *(Note 1)*

Package	Transmitter/Receiver	Total Channels	Center Fast PLLs	
			PLL1	PLL2
484-pin FineLine BGA	Transmitter	29	16	13
			13	16
	Receiver	31	17	14
			14	17
780-pin FineLine GBA	Transmitter	29	16	13
			13	16
	Receiver	31	17	14
			14	17

Note to Table 2–30:

(1) The total number of receiver channels includes the four non-dedicated clock channels that can be optionally used as data channels.

Table 2–31. EP1AGX35 Device Differential Channels *(Note 1)*

Package	Transmitter/Receiver	Total Channels	Center Fast PLLs	
			PLL1	PLL2
484-pin FineLine BGA	Transmitter	29	16	13
			13	16
	Receiver	31	17	14
			14	17
780-pin FineLine BGA	Transmitter	29	16	13
			13	16
	Receiver	31	17	14
			14	17

Note to Table 2–31:

(1) The total number of receiver channels includes the four non-dedicated clock channels that can be optionally used as data channels.

Table 2–32. EP1AGX50 Device Differential Channels *(Note 1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs		Corner Fast PLLs	
			PLL1	PLL2	PLL7	PLL8
484-pin FineLine BGA	Transmitter	29	16	13	—	—
			13	16	—	—
	Receiver	31	17	14	—	—
			14	17	—	—
780-pin FineLine BGA	Transmitter	29	16	13	—	—
			13	16	—	—
	Receiver	31	17	14	—	—
			14	17	—	—
1,152-pin FineLine BGA	Transmitter	42	21	21	21	21
			21	21	—	—
	Receiver	42	21	21	21	21
			21	21	—	—

Note to Table 2–32:

(1) The total number of receiver channels includes the four non-dedicated clock channels that can be optionally used as data channels.

Table 2–33. EP1AGX60 Device Differential Channels *(Note 1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs		Corner Fast PLLs	
			PLL1	PLL2	PLL7	PLL8
484-pin FineLine BGA	Transmitter	29	16	13	—	—
			13	16	—	—
	Receiver	31	17	14	—	—
			14	17	—	—
780-pin FineLine BGA	Transmitter	29	16	13	—	—
			13	16	—	—
	Receiver	31	17	14	—	—
			14	17	—	—
1,152-pin FineLine BGA	Transmitter	42	21	21	21	21
			21	21	—	—
	Receiver	42	21	21	21	21
			21	21	—	—

Note to Table 2–33:

(1) The total number of receiver channels includes the four non-dedicated clock channels that can be optionally used as data channels.

The Arria GX device instruction register length is 10 bits and the USERCODE register length is 32 bits. Table 3–2 and Table 3–3 show the boundary-scan register length and device IDCODE information for Arria GX devices.

Table 3–2. Arria GX Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP1AGX20	1320
EP1AGX35	1320
EP1AGX50	1668
EP1AGX60	1668
EP1AGX90	2016

Table 3–3. 2-Bit Arria GX Device IDCODE

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit)
EP1AGX20	0000	0010 0001 0010 0001	000 0110 1110	1
EP1AGX35	0000	0010 0001 0010 0001	000 0110 1110	1
EP1AGX50	0000	0010 0001 0010 0010	000 0110 1110	1
EP1AGX60	0000	0010 0001 0010 0010	000 0110 1110	1
EP1AGX90	0000	0010 0001 0010 0011	000 0110 1110	1

SignalTap II Embedded Logic Analyzer

Arria GX devices feature the SignalTap II embedded logic analyzer, which monitors design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry. You can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages, such as FineLine BGA (FBGA) packages, because it can be difficult to add a connection to a pin during the debugging process after a board is designed and manufactured.

Configuration

The logic, circuitry, and interconnects in the Arria GX architecture are configured with CMOS SRAM elements. Altera® FPGAs are reconfigurable and every device is tested with a high coverage production test program so you do not have to perform fault testing and can instead focus on simulation and design verification.

Arria GX devices are configured at system power up with data stored in an Altera configuration device or provided by an external controller (for example, a MAX® II device or microprocessor). You can configure Arria GX devices using the fast passive parallel (FPP), active serial (AS), passive serial (PS), passive parallel asynchronous (PPA), and JTAG configuration schemes. Each Arria GX device has an optimized interface that allows microprocessors to configure it serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat Arria GX devices as memory and configure them by writing to a virtual memory location, making reconfiguration easy.

Table 4–27. SSTL-18 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	High-level output voltage	I_{OH} = –13.4 mA *(1)*	V_{CCIO} – 0.28	—	—	V
V_{OL}	Low-level output voltage	I_{OL} = 13.4 mA *(1)*	—	—	0.28	V

Note to Table 4–27:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Arria GX Architecture* chapter.

Table 4–28. SSTL-18 Class I & II Differential Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	1.71	1.8	1.89	V
V_{SWING} (DC)	DC differential input voltage	0.25	—	—	V
V_X (AC)	AC differential input cross point voltage	(V_{CCIO}/2) – 0.175	—	(V_{CCIO}/2) + 0.175	V
V_{SWING} (AC)	AC differential input voltage	0.5	—	—	V
V_{ISO}	Input clock signal offset voltage	—	0.5 V_{CCIO}	—	V
ΔV_{ISO}	Input clock signal offset voltage variation	—	200	—	mV
V_{OX} (AC)	AC differential cross point voltage	(V_{CCIO}/2) – 0.125	—	(V_{CCIO}/2) + 0.125	V

Table 4–29. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	2.375	2.5	2.625	V
V_{TT}	Termination voltage	—	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage	—	1.188	1.25	1.313	V
V_{IH} (DC)	High-level DC input voltage	—	V_{REF} + 0.18	—	3.0	V
V_{IL} (DC)	Low-level DC input voltage	—	–0.3	—	V_{REF} – 0.18	V
V_{IH} (AC)	High-level AC input voltage	—	V_{REF} + 0.35	—	—	V
V_{IL} (AC)	Low-level AC input voltage	—	—	—	V_{REF} – 0.35	V
V_{OH}	High-level output voltage	I_{OH} = –8.1 mA *(1)*	V_{TT} + 0.57	—		V
V_{OL}	Low-level output voltage	I_{OL} = 8.1 mA *(1)*	—	—	V_{TT} – 0.57	V

Note to Table 4–29:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Arria GX Architecture* chapter.

Table 4–30. SSTL-2 Class II Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	2.375	2.5	2.625	V
V_{TT}	Termination voltage	—	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage	—	1.188	1.25	1.313	V
V_{IH} (DC)	High-level DC input voltage	—	V_{REF} + 0.18	—	V_{CCIO} + 0.3	V

Table 4–33. 1.5-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	1.425	1.5	1.575	V
V_{REF}	Input reference voltage	—	0.713	0.75	0.788	V
V_{TT}	Termination voltage	—	0.713	0.75	0.788	V
V_{IH} (DC)	DC high-level input voltage	—	V_{REF} + 0.1	—	—	V
V_{IL} (DC)	DC low-level input voltage	—	–0.3	—	V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage	—	V_{REF} + 0.2	—	—	V
V_{IL} (AC)	AC low-level input voltage	—	—	—	V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(1)*	V_{CCIO} – 0.4	—	—	V
V_{OL}	Low-level output voltage	I_{OH} = –8 mA *(1)*	—	—	0.4	V

Note to Table 4–33:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Arria GX Architecture* chapter.

Table 4–34. 1.5-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	1.425	1.50	1.575	V
V_{REF}	Input reference voltage	—	0.713	0.75	0.788	V
V_{TT}	Termination voltage	—	0.713	0.75	0.788	V
V_{IH} (DC)	DC high-level input voltage	—	V_{REF} + 0.1	—	—	V
V_{IL} (DC)	DC low-level input voltage	—	–0.3	—	V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage	—	V_{REF} + 0.2	—	—	V
V_{IL} (AC)	AC low-level input voltage	—	—	—	V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(1)*	V_{CCIO} – 0.4	—	—	V
V_{OL}	Low-level output voltage	I_{OH} = –16 mA *(1)*	—	—	0.4	V

Note to Table 4–34:

(1) This specification is supported across all the programmable drive settings available for this I/O standard, as shown in the *Arria GX Architecture* chapter.

Table 4–35. 1.5-V HSTL Class I & II Differential Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage	1.425	1.5	1.575	V
V_{DIF} (DC)	DC input differential voltage	0.2	—	—	V
V_{CM} (DC)	DC common mode input voltage	0.68	—	0.9	V
V_{DIF} (AC)	AC differential input voltage	0.4	—	—	V
V_{OX} (AC)	AC differential cross point voltage	0.68	—	0.9	V

Table 4–67. EP1AGX60 Column Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
LVDS	GCLK	t_{SU}	0.980	0.980	2.062	ns
		t_{H}	–0.875	–0.875	–1.785	ns
	GCLK PLL	t_{SU}	2.557	2.557	5.512	ns
		t_{H}	–2.452	–2.452	–5.235	ns

Table 4–68 lists I/O timing specifications.

Table 4–68. EP1AGX60 Row Pins Output Timing Parameters (Part 1 of 2)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	3.052	3.052	7.142	ns
		GCLK PLL	t_{CO}	1.490	1.490	3.719	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.924	2.924	6.502	ns
		GCLK PLL	t_{CO}	1.362	1.362	3.079	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.868	2.868	6.465	ns
		GCLK PLL	t_{CO}	1.306	1.306	3.042	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.924	2.924	6.502	ns
		GCLK PLL	t_{CO}	1.362	1.362	3.079	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.818	2.818	6.196	ns
		GCLK PLL	t_{CO}	1.256	1.256	2.773	ns
2.5 V	4 mA	GCLK	t_{CO}	2.907	2.907	6.476	ns
		GCLK PLL	t_{CO}	1.345	1.345	3.053	ns
2.5 V	8 mA	GCLK	t_{CO}	2.804	2.804	6.218	ns
		GCLK PLL	t_{CO}	1.242	1.242	2.795	ns
2.5 V	12 mA	GCLK	t_{CO}	2.785	2.785	6.104	ns
		GCLK PLL	t_{CO}	1.223	1.223	2.681	ns
1.8 V	2 mA	GCLK	t_{CO}	2.991	2.991	7.521	ns
		GCLK PLL	t_{CO}	1.419	1.419	4.078	ns
1.8 V	4 mA	GCLK	t_{CO}	2.980	2.980	6.742	ns
		GCLK PLL	t_{CO}	1.408	1.408	3.299	ns
1.8 V	6 mA	GCLK	t_{CO}	2.869	2.869	6.441	ns
		GCLK PLL	t_{CO}	1.297	1.297	2.998	ns
1.8 V	8 mA	GCLK	t_{CO}	2.838	2.838	6.327	ns
		GCLK PLL	t_{CO}	1.266	1.266	2.884	ns
1.5 V	2 mA	GCLK	t_{CO}	2.951	2.951	7.020	ns
		GCLK PLL	t_{CO}	1.379	1.379	3.577	ns
1.5 V	4 mA	GCLK	t_{CO}	2.844	2.844	6.419	ns
		GCLK PLL	t_{CO}	1.272	1.272	2.976	ns

Table 4–69. EP1AGX60 Column Pins Output Timing Parameters (Part 4 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V PCI	—	GCLK	t_{CO}	2.882	2.882	6.213	ns
		GCLK PLL	t_{CO}	1.312	1.312	2.778	ns
3.3-V PCI-X	—	GCLK	t_{CO}	2.882	2.882	6.213	ns
		GCLK PLL	t_{CO}	1.312	1.312	2.778	ns
LVDS	—	GCLK	t_{CO}	3.746	3.746	7.396	ns
		GCLK PLL	t_{CO}	2.185	2.185	3.973	ns

Table 4–70 through Table 4–71 list EP1AGX60 regional clock (RCLK) adder values that should be added to the GCLK values. These adder values are used to determine I/O timing when the I/O pin is driven using the regional clock. This applies for all I/O standards supported by Arria GX with general purpose I/O pins.

Table 4–70 describes row pin delay adders when using the regional clock in Arria GX devices.

Table 4–70. EP1AGX60 Row Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.138	0.138	0.311	ns
RCLK PLL input adder	–0.003	–0.003	–0.006	ns
RCLK output adder	–0.138	–0.138	–0.311	ns
RCLK PLL output adder	0.003	0.003	0.006	ns

Table 4–71 lists column pin delay adders when using the regional clock in Arria GX devices.

Table 4–71. EP1AGX60 Column Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.153	0.153	0.344	ns
RCLK PLL input adder	–1.066	–1.066	–2.338	ns
RCLK output adder	–0.153	–0.153	–0.343	ns
RCLK PLL output adder	1.721	1.721	4.486	ns

EP1AGX90 I/O Timing Parameters

Table 4–72 through Table 4–75 list the maximum I/O timing parameters for EP1AGX90 devices for I/O standards which support general purpose I/O pins.

EP1AGX50 Clock Timing Parameters

Table 4–87 through Table 4–88 list the GCLK clock timing parameters for EP1AGX50 devices.

Table 4–87 lists clock timing specifications.

Table 4–87. EP1AGX50 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.529	1.529	3.587	ns
t_{COUT}	1.534	1.534	3.581	ns
t_{PLLCIN}	–0.024	–0.024	0.181	ns
$t_{PLLCOUT}$	–0.019	–0.019	0.175	ns

Table 4–88 lists clock timing specifications.

Table 4–88. EP1AGX50 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.793	1.793	4.165	ns
t_{COUT}	1.793	1.793	4.165	ns
t_{PLLCIN}	0.238	0.238	0.758	ns
$t_{PLLCOUT}$	0.238	0.238	0.758	ns

Table 4–89 through Table 4–90 list the RCLK clock timing parameters for EP1AGX50 devices.

Table 4–89 lists clock timing specifications.

Table 4–89. EP1AGX50 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.396	1.396	3.287	ns
t_{COUT}	1.401	1.401	3.281	ns
t_{PLLCIN}	–0.017	–0.017	0.195	ns
$t_{PLLCOUT}$	–0.012	–0.012	0.189	ns

To calculate the DCD as a percentage:

(T/2 – DCD) / T = (3,745 ps/2 – 125 ps) / 3,745 ps = 46.66% (for low boundary)

(T/2 + DCD) / T = (3,745 ps/2 + 125 ps) / 3,745 ps = 53.33% (for high boundary)

Therefore, the DCD percentage for the output clock at 267 MHz is from 46.66% to 53.33%.

Table 4–109. Maximum DCD for Non-DDIO Output on Column I/O Pins

Column I/O Output Standard I/O Standard	Maximum DCD (ps) for Non-DDIO Output	Units
	–6 Speed Grade	
3.3-V LVTTL	220	ps
3.3-V LVCMOS	175	ps
2.5 V	155	ps
1.8 V	110	ps
1.5-V LVCMOS	215	ps
SSTL-2 Class I	135	ps
SSTL-2 Class II	130	ps
SSTL-18 Class I	115	ps
SSTL-18 Class II	100	ps
1.8-V HSTL Class I	110	ps
1.8-V HSTL Class II	110	ps
1.5-V HSTL Class I	115	ps
1.5-V HSTL Class II	80	ps
1.2-V HSTL-12	200	ps
LVPECL	80	ps

Table 4–110. Maximum DCD for DDIO Output on Row I/O Pins Without PLL in the Clock Path *Note (1)*

Maximum DCD (ps) for Row DDIO Output I/O Standard	Input I/O Standard (No PLL in the Clock Path)					Units
	TTL/CMOS		SSTL-2	SSTL/HSTL	LVDS	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	3.3V	
3.3-V LVTTL	440	495	170	160	105	ps
3.3-V LVCMOS	390	450	120	110	75	ps
2.5 V	375	430	105	95	90	ps
1.8 V	325	385	90	100	135	ps
1.5-V LVCMOS	430	490	160	155	100	ps
SSTL-2 Class I	355	410	85	75	85	ps
SSTL-2 Class II	350	405	80	70	90	ps
SSTL-18 Class I	335	390	65	65	105	ps
1.8-V HSTL Class I	330	385	60	70	110	ps
1.5-V HSTL Class I	330	390	60	70	105	ps

Table 4–115. High-Speed I/O Specifications (Part 2 of 2) *Note (1), (2)*

Symbol	Conditions			–6 Speed Grade			Units
				Min	Typ	Max	
DPA lock time	Standard	Training Pattern	Transition Density		—	—	Number of repetitions
	SPI-4	000000000011 11111111	10%	256	—	—	
	Parallel Rapid I/O	00001111	25%	256	—	—	
		10010000	50%	256	—	—	
	Miscellaneous	10101010	100%	256	—	—	
		01010101	—	256	—	—	

Notes to Table 4–115:

(1) When J = 4 to 10, the SERDES block is used.

(2) When J = 1 or 2, the SERDES block is bypassed.

(3) The input clock frequency and the W factor must satisfy the following fast PLL VCO specification: 150 ≤ input clock frequency × W ≤ 1,040.

(4) The minimum specification is dependent on the clock source (fast PLL, enhanced PLL, clock pin, and so on) and the clock routing resource (global, regional, or local) used. The I/O differential buffer and input register do not have a minimum toggle rate.

Table 4–123 lists the JTAG timing parameters and values for Arria GX devices.

Table 4–123. Arria GX JTAG Timing Parameters and Values

Symbol	Parameter	Min	Max	Units
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	12	—	ns
t_{JCL}	TCK clock low time	12	—	ns
t_{JPSU}	JTAG port setup time	4	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	9	ns
t_{JPZX}	JTAG port high impedance to valid output	—	9	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	9	ns
t_{JSSU}	Capture register setup time	4	—	ns
t_{JSH}	Capture register hold time	5	—	ns
t_{JSCO}	Update register clock to output	—	12	ns
t_{JSZX}	Update register high impedance to valid output	—	12	ns
t_{JSXZ}	Update register valid output to high impedance	—	12	ns

5. Reference and Ordering Information

AGX51005-2.0

Software

Arria® GX devices are supported by the Altera® Quartus® II design software, which provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap® II logic analyzer, and device configuration.

For more information about the Quartus II software features, refer to the *Quartus II Development Software Handbook* .

The Quartus II software supports the Windows XP/2000/NT, Sun Solaris 8/9, Linux Red Hat v7.3, Linux Red Hat Enterprise 3, and HP-UX operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink interface.

Device Pin-Outs

Arria GX device pin-outs are available on the Altera web site at www.altera.com.

Ordering Information

Figure 5–1 describes the ordering codes for Arria GX devices.

For more information on a specific package, refer to the *Package Information for Arria GX Devices* chapter.