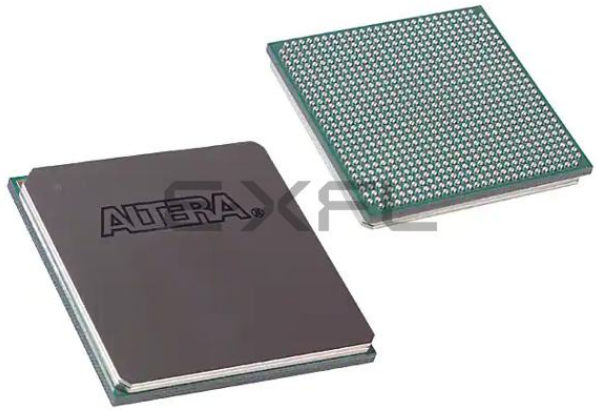

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2508
Number of Logic Elements/Cells	50160
Total RAM Bits	2475072
Number of I/O	350
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1agx50df780c6n

Each transceiver channel is full-duplex and consists of a transmitter channel and a receiver channel.

The transmitter channel contains the following sub-blocks:

- Transmitter phase compensation first-in first-out (FIFO) buffer
- Byte serializer (optional)
- 8B/10B encoder (optional)
- Serializer (parallel-to-serial converter)
- Transmitter differential output buffer

The receiver channel contains the following:

- Receiver differential input buffer
- Receiver lock detector and run length checker
- CRU
- Deserializer
- Pattern detector
- Word aligner
- Lane deskew
- Rate matcher (optional)
- 8B/10B decoder (optional)
- Byte deserializer (optional)
- Receiver phase compensation FIFO buffer

You can configure the transceiver channels to the desired functional modes using the ALT2GXB MegaCore instance in the Quartus® II MegaWizard™ Plug-in Manager for the Arria GX device family. Depending on the selected functional mode, the Quartus II software automatically configures the transceiver channels to employ a subset of the sub-blocks listed above.

Transmitter Path

This section describes the data path through the Arria GX transmitter. The sub-blocks are described in order from the PLD-transmitter parallel interface to the serial transmitter buffer.

Clock Multiplier Unit

Each transceiver block has a clock multiplier unit (CMU) that takes in a reference clock and synthesizes two clocks: a high-speed serial clock to serialize the data and a low-speed parallel clock to clock the transmitter digital logic (PCS).

The CMU is further divided into three sub-blocks:

- One transmitter PLL
- One central clock divider block
- Four local clock divider blocks (one per channel)

- Inter-transceiver block lines driven by reference clock input pins of other transceiver blocks

Altera® recommends using the dedicated reference clock input pins (REFCLK0 or REFCLK1) to provide reference clock for the transmitter PLL.

Table 2–2 lists the adjustable parameters in the transmitter PLL.

Table 2–2. Transmitter PLL Specifications

Parameter	Specifications
Input reference frequency range	50 MHz to 622.08 MHz
Data rate support	600 Mbps to 3.125 Gbps
Bandwidth	Low, medium, or high

The transmitter PLL output feeds the central clock divider block and the local clock divider blocks. These clock divider blocks divide the high-speed serial clock to generate the low-speed parallel clock for the transceiver PCS logic and PLD-transceiver interface clock.

Transmitter Phase Compensation FIFO Buffer

A transmitter phase compensation FIFO is located at each transmitter channel's logic array interface. It compensates for the phase difference between the transmitter PCS clock and the local PLD clock. The transmitter phase compensation FIFO is used in all supported functional modes. The transmitter phase compensation FIFO buffer is eight words deep in PCI Express (PIPE) mode and four words deep in all other modes.

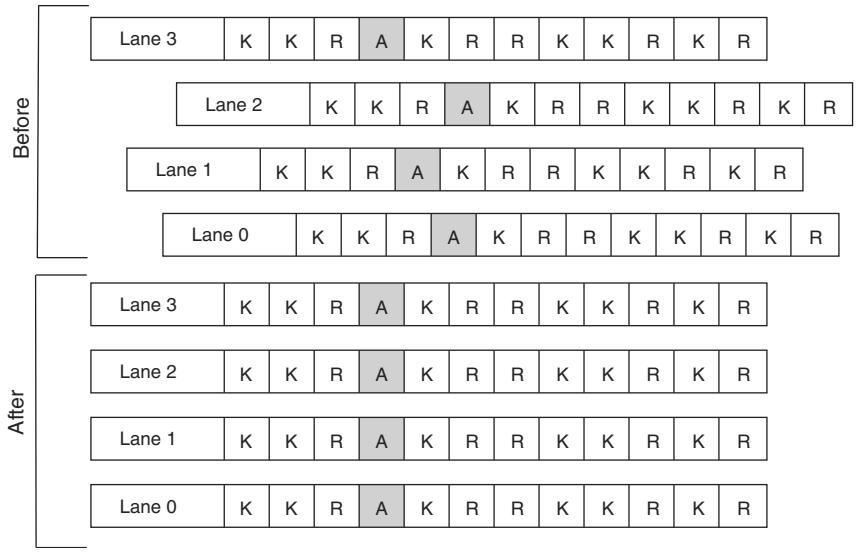
For more information about architecture and clocking, refer to the *Arria GX Transceiver Architecture* chapter.

Byte Serializer

The byte serializer takes in two-byte wide data from the transmitter phase compensation FIFO buffer and serializes it into a one-byte wide data at twice the speed. The transmit data path after the byte serializer is 8 or 10 bits. This allows clocking the PLD-transceiver interface at half the speed when compared with the transmitter PCS logic. The byte serializer is bypassed in GIGE mode. After serialization, the byte serializer transmits the least significant byte (LSByte) first and the most significant byte (MSByte) last.

Figure 2–16 shows misaligned channels before the channel aligner and the aligned channels after the channel aligner.

Figure 2–16. Before and After the Channel Aligner



Rate Matcher

In asynchronous systems, the upstream transmitter and local receiver can be clocked with independent reference clock sources. Frequency differences in the order of a few hundred PPM can potentially corrupt the data at the receiver.

The rate matcher compensates for small clock frequency differences between the upstream transmitter and the local receiver clocks by inserting or removing skip characters from the inter packet gap (IPG) or idle streams. It inserts a skip character if the local receiver is running a faster clock than the upstream transmitter. It deletes a skip character if the local receiver is running a slower clock than the upstream transmitter. The Quartus II software automatically configures the appropriate skip character as specified in the IEEE 802.3 for GIGE mode and PCI-Express Base Specification for PCI Express (PIPE) mode. The rate matcher is bypassed in Serial RapidIO and must be implemented in the PLD logic array or external circuits depending on your system design.

Table 2–5 lists the maximum frequency difference that the rate matcher can tolerate in XAUI, PCI Express (PIPE), GIGE, and Basic functional modes.

Table 2–5. Rate Matcher PPM Tolerance

Function Mode	PPM
XAUI	± 100
PCI Express (PIPE)	± 300
GIGE	± 100
Basic	± 300

The transmitter PLL multiplies the input reference clock to generate a high-speed serial clock at a frequency that is half the data rate of the configured functional mode. This high-speed serial clock (or its divide-by-two version if the functional mode uses byte serializer) is fed to the CMU clock divider block. Depending on the configured functional mode, the CMU clock divider block divides the high-speed serial clock to generate the low-speed parallel clock that clocks the transceiver PCS logic in the associated channel. The low-speed parallel clock is also forwarded to the PLD logic array on the `tx_clkout` or `coreclkout` ports.

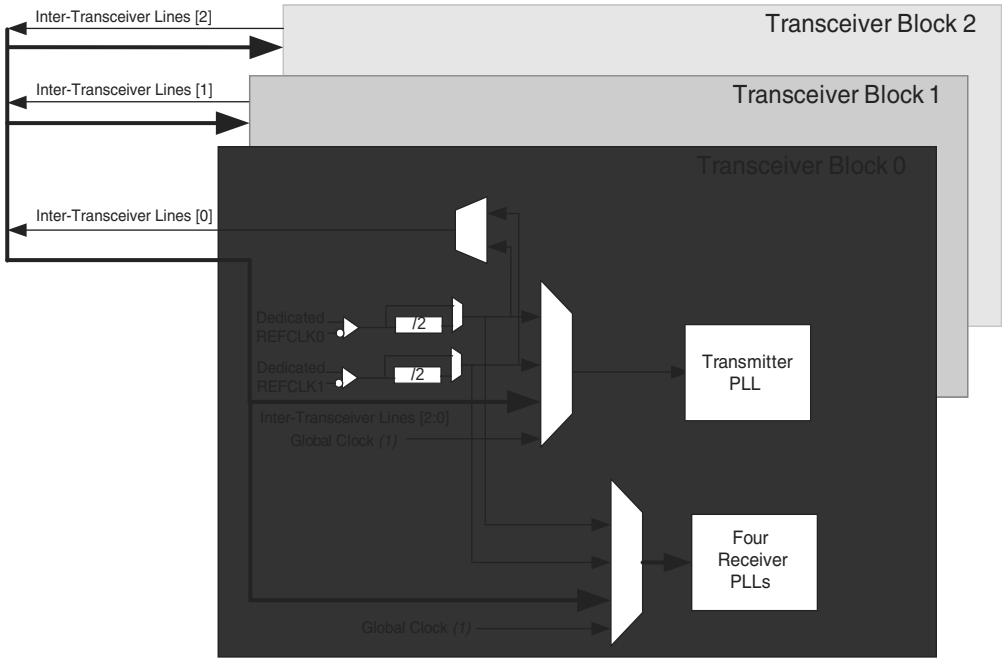
The receiver PLL in each channel is also fed by an input reference clock. The receiver PLL along with the clock recovery unit generates a high-speed serial recovered clock and a low-speed parallel recovered clock. The low-speed parallel recovered clock feeds the receiver PCS logic until the rate matcher. The CMU low-speed parallel clock clocks the rest of the logic from the rate matcher until the receiver phase compensation FIFO. In modes that do not use a rate matcher, the receiver PCS logic is clocked by the recovered clock until the receiver phase compensation FIFO.

The input reference clock to the transmitter and receiver PLLs can be derived from:

- One of two available dedicated reference clock input pins (`REFCLK0` or `REFCLK1`) of the associated transceiver block
- PLD clock network (must be driven directly from an input clock pin and cannot be driven by user logic or enhanced PLL)
- Inter-transceiver block lines driven by reference clock input pins of other transceiver blocks

Figure 2–22 shows the input reference clock sources for the transmitter and receiver PLL.

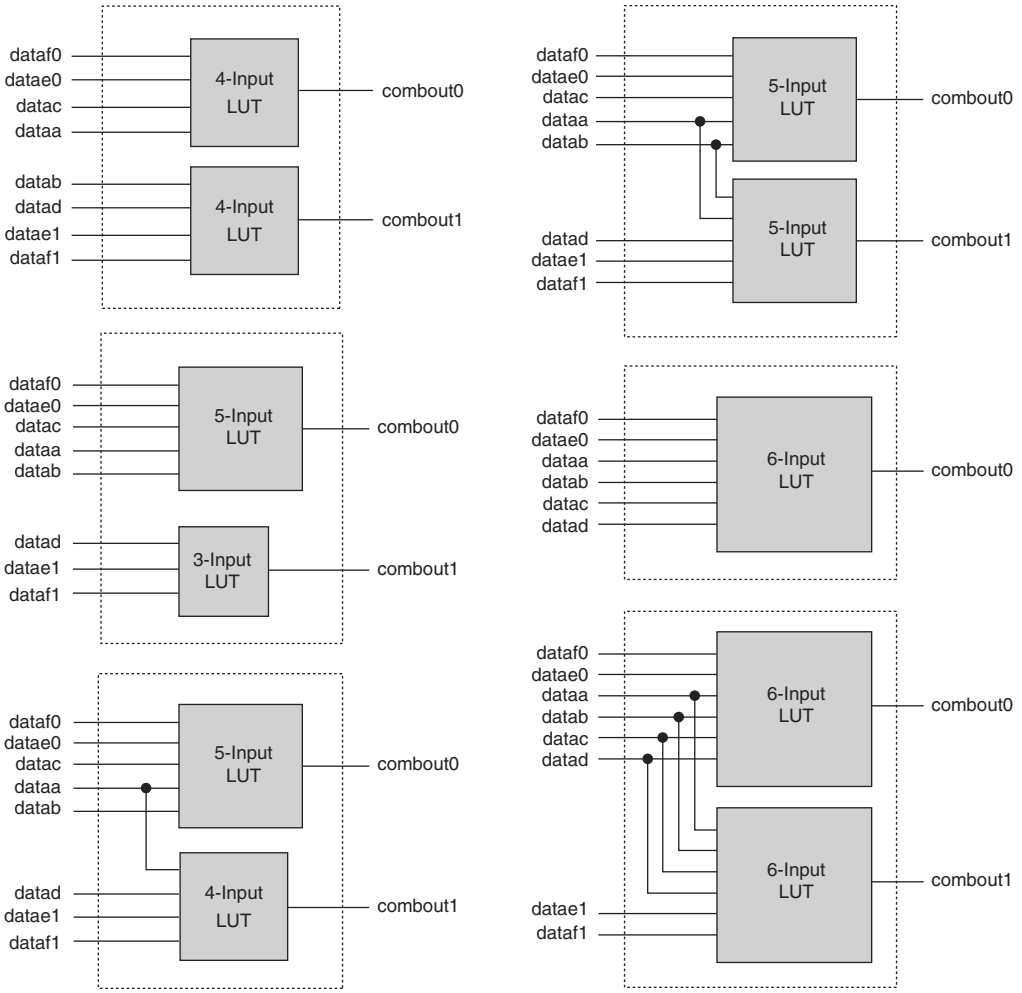
Figure 2–22. Input Reference Clock Sources



Normal Mode

Normal mode is suitable for general logic applications and combinational functions. In this mode, up to eight data inputs from the LAB local interconnect are inputs to the combinational logic. Normal mode allows two functions to be implemented in one Arria GX ALM, or an ALM to implement a single function of up to six inputs. The ALM can support certain combinations of completely independent functions and various combinations of functions which have common inputs. Figure 2–30 shows the supported LUT combinations in normal mode.

Figure 2–30. ALM in Normal Mode *(Note 1)*



Note to Figure 2–30:

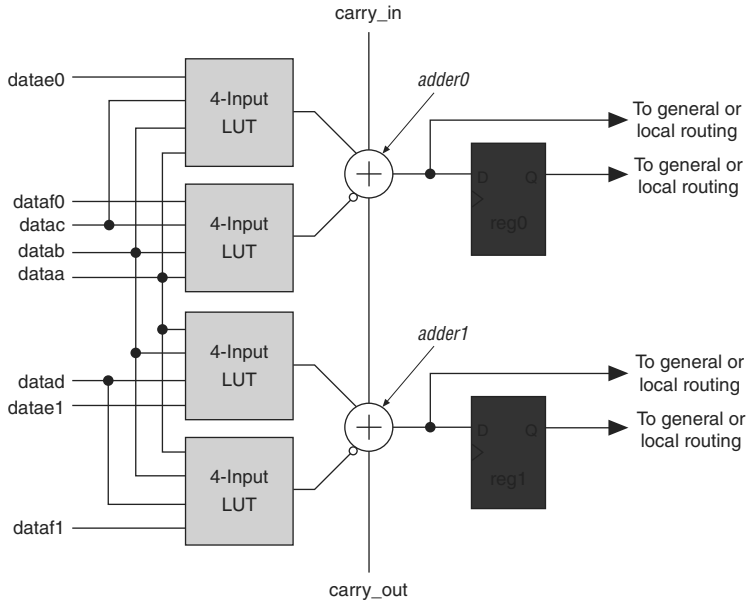
(1) Combinations of functions with less inputs than those shown are also supported. For example, combinations of functions with the following number of inputs are supported: 4 and 3, 3 and 3, 3 and 2, 5 and 2, and so on.

Normal mode provides complete backward compatibility with four-input LUT architectures. Two independent functions of four inputs or less can be implemented in one Arria GX ALM. In addition, a five-input function and an independent three-input function can be implemented without sharing inputs.

Arithmetic Mode

Arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. An ALM in arithmetic mode uses two sets of 2 four-input LUTs along with two dedicated full adders. The dedicated adders allow the LUTs to be available to perform pre-adder logic; therefore, each adder can add the output of two four-input functions. The four LUTs share the `dataa` and `datab` inputs. As shown in Figure 2–34, the carry-in signal feeds to `adder0`, and the carry-out from `adder0` feeds to carry-in of `adder1`. The carry-out from `adder1` drives to `adder0` of the next ALM in the LAB. ALMs in arithmetic mode can drive out registered and/or unregistered versions of the adder outputs.

Figure 2–34. ALM in Arithmetic Mode



While operating in arithmetic mode, the ALM can support simultaneous use of the adder's carry output along with combinational logic outputs. In this operation, adder output is ignored. This usage of the adder with the combinational logic output provides resource savings of up to 50% for functions that can use this ability. An example of such functionality is a conditional operation, such as the one shown in Figure 2–35. The equation for this example is:

Equation 2–1.

$$R = (X < Y) ? Y : X$$

To implement this function, the adder is used to subtract 'Y' from 'X.' If 'X' is less than 'Y,' the `carry_out` signal is '1.' The `carry_out` signal is fed to an adder where it drives out to the LAB local interconnect. It then feeds to the LAB-wide `syncload` signal. When asserted, `syncload` selects the `syncdata` input. In this case, the data 'Y' drives the `syncdata` inputs to the registers. If 'X' is greater than or equal to 'Y,' the `syncload` signal is deasserted and 'X' drives the data port of the registers.

Table 2–11. TriMatrix Memory Features (Part 2 of 2)

Memory Feature	M512 RAM Block (32 × 18 Bits)	M4K RAM Block (128 × 36 Bits)	M-RAM Block (4K × 144 Bits)
ROM	✓	✓	—
FIFO buffer	✓	✓	✓
Pack mode	—	✓	✓
Byte enable	✓	✓	✓
Address clock enable	—	✓	✓
Parity bits	✓	✓	✓
Mixed clock mode	✓	✓	✓
Memory initialization file (**.mif**)	✓	✓	—
Simple dual-port memory mixed width support	✓	✓	✓
True dual-port memory mixed width support	—	✓	✓
Power-up conditions	Outputs cleared	Outputs cleared	Outputs unknown
Register clears	Output registers	Output registers	Output registers
Mixed-port read-during-write	Unknown output/old data	Unknown output/old data	Unknown output
Configurations	512 × 1 256 × 2 128 × 4 64 × 8 64 × 9 32 × 16 32 × 18	4K × 1 2K × 2 1K × 4 512 × 8 512 × 9 256 × 16 256 × 18 128 × 32 128 × 36	64K × 8 64K × 9 32K × 16 32K × 18 16K × 32 16K × 36 8K × 64 8K × 72 4K × 128 4K × 144

TriMatrix memory provides three different memory sizes for efficient application support. The Quartus II software automatically partitions the user-defined memory into the embedded memory blocks using the most efficient size combinations. You can also manually assign the memory to a specific block size or a mixture of block sizes.

M512 RAM Block

The M512 RAM block is a simple dual-port memory block and is useful for implementing small FIFO buffers, DSP, and clock domain transfer applications. Each block contains 576 RAM bits (including parity bits). M512 RAM blocks can be configured in the following modes:

- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

Table 2–12. M-RAM Row Interface Unit Signals (Part 2 of 2)

Unit Interface Block	Input Signals	Output Signals
L4	datain_a[56..42] byteena_a[5..4]	dataout_a[59..48]
L5	datain_a[71..57] byteena_a[7..6]	dataout_a[71..60]
R0	datain_b[14..0] byteena_b[1..0]	dataout_b[11..0]
R1	datain_b[29..15] byteena_b[3..2]	dataout_b[23..12]
R2	datain_b[35..30] addressb[4..0] addr_ena_b clock_b clocken_b renwe_b aclr_b	dataout_b[35..24]
R3	addressb[15..5] datain_b[41..36]	dataout_b[47..36]
R4	datain_b[56..42] byteena_b[5..4]	dataout_b[59..48]
R5	datain_b[71..57] byteena_b[7..6]	dataout_b[71..60]

For more information about TriMatrix memory, refer to the *TriMatrix Embedded Memory Blocks in Arria GX Devices* chapter.

Digital Signal Processing Block

The most commonly used DSP functions are finite impulse response (FIR) filters, complex FIR filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, direct cosine transform (DCT) functions, and correlators. All of these use the multiplier as the fundamental building block. Additionally, some applications need specialized operations such as multiply-add and multiply-accumulate operations. Arria GX devices provide DSP blocks to meet the arithmetic requirements of these functions.

Each Arria GX device has two to four columns of DSP blocks to efficiently implement DSP functions faster than ALM-based implementations. Each DSP block can be configured to support up to:

- Eight 9 × 9-bit multipliers
- Four 18 × 18-bit multipliers
- One 36 × 36-bit multiplier

Table 2–15. DSP Block Signal Sources and Destinations

LAB Row at Interface	Control Signals Generated	Data Inputs	Data Outputs
0	clock0 aclr0 ena0 mult01_saturate addnsub1_round/ accum_round addnsub1 signa sourcea sourceb	A1[17..0] B1[17..0]	OA[17..0] OB[17..0]
1	clock1 aclr1 ena1 accum_saturate mult01_round accum_sload sourcea sourceb mode0	A2[17..0] B2[17..0]	OC[17..0] OD[17..0]
2	clock2 aclr2 ena2 mult23_saturate addnsub3_round/ accum_round addnsub3 sign_b sourcea sourceb	A3[17..0] B3[17..0]	OE[17..0] OF[17..0]
3	clock3 aclr3 ena3 accum_saturate mult23_round accum_sload sourcea sourceb mode1	A4[17..0] B4[17..0]	OG[17..0] OH[17..0]

Table 4–3. Arria GX Device Recommended Operating Conditions (Part 2 of 2) *(Note 1)* (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Units
T_J	Operating junction temperature	For commercial use	0	85	C
		For industrial use	–40	100	C

Notes to Table 4–3:

(1) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.

(2) During transitions, the inputs may overshoot to the voltage shown in Table 4–2 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

(3) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically from ground to V_{CC}.

(4) V_{CCPD} must ramp-up from 0 V to 3.3 V within 100 µs to 100 ms. If V_{CCPD} is not ramped up within this specified time, the Arria GX device will not configure successfully. If the system does not allow for a V_{CCPD} ramp-up time of 100 ms or less, hold nCONFIG low until all power supplies are reliable.

(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, can be driven before V_{CCINT}, V_{CCPD}, and V_{CCIO} are powered.

(6) V_{CCIO} maximum and minimum conditions for PCI and PCI-X are shown in parentheses.

Transceiver Block Characteristics

Table 4–4 through Table 4–6 on page 4–4 contain transceiver block specifications.

Table 4–4. Arria GX Transceiver Block Absolute Maximum Ratings *(Note 1)*

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCA}	Transceiver block supply voltage	Commercial and industrial	–0.5	4.6	V
V_{CCP}	Transceiver block supply voltage	Commercial and industrial	–0.5	1.8	V
V_{CCR}	Transceiver block supply voltage	Commercial and industrial	–0.5	1.8	V
V_{CCT_B}	Transceiver block supply voltage	Commercial and industrial	–0.5	1.8	V
V_{CCL_B}	Transceiver block supply voltage	Commercial and industrial	–0.5	1.8	V
V_{CCH_B}	Transceiver block supply voltage	Commercial and industrial	–0.5	2.4	V

Note to Table 4–4:

(1) The device can tolerate prolonged operation at this absolute maximum, as long as the maximum specification is not violated.

Table 4–5. Arria GX Transceiver Block Operating Conditions

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCA}	Transceiver block supply voltage	Commercial and industrial	3.135	3.3	3.465	V
V_{CCP}	Transceiver block supply voltage	Commercial and industrial	1.15	1.2	1.25	V
V_{CCR}	Transceiver block supply voltage	Commercial and industrial	1.15	1.2	1.25	V
V_{CCT_B}	Transceiver block supply voltage	Commercial and industrial	1.15	1.2	1.25	V
V_{CCL_B}	Transceiver block supply voltage	Commercial and industrial	1.15	1.2	1.25	V
V_{CCH_B}	Transceiver block supply voltage	Commercial and industrial	1.15	1.2	1.25	V
			1.425	1.5	1.575	V
R_{REFB} *(1)*	Reference resistor	Commercial and industrial	2K - 1%	2K	2K +1%	Ω

Note to Table 4–5:

(1) The DC signal on this pin must be as clean as possible. Ensure that no noise is coupled to this pin.

Table 4–7. Arria GX Transceiver Block AC Specification *(Note 1), (2), (3)* (Part 3 of 4)

Description	Condition	–6 Speed Grade Commercial & Industrial	Units
Serial RapidIO (1.25 Gbps, 2.5 Gbps, and 3.125 Gbps) Receiver Jitter Tolerance *(6)*			
Total Jitter Tolerance	CJPAT Compliance Pattern; DC Gain = 0 dB	> 0.65	UI p-p
Combined Deterministic and Random Jitter Tolerance (J_{DR})	CJPAT Compliance Pattern; DC Gain = 0 dB	> 0.55	UI p-p
Deterministic Jitter Tolerance (J_D)	CJPAT Compliance Pattern; DC Gain = 0 dB	> 0.37	UI p-p
Sinusoidal Jitter Tolerance	Jitter Frequency = 22.1 KHz	> 8.5	UI p-p
	Jitter Frequency = 200 KHz	> 1.0	UI p-p
	Jitter Frequency = 1.875 MHz	> 0.1	UI p-p
	Jitter Frequency = 20 MHz	> 0.1	UI p-p
SDI Transmitter Jitter Generation *(8)*			
Alignment Jitter (peak-to-peak)	Data Rate = 1.485 Gbps (HD) REFCLK = 74.25 MHz Pattern = Color Bar Vod = 800 mV No Pre-emphasis Low-Frequency Roll-Off = 100 KHz	0.2	UIv
	Data Rate = 2.97 Gbps (3G) REFCLK = 148.5 MHz Pattern = Color Bar Vod = 800 mV No Pre-emphasis Low-Frequency Roll-Off = 100 KHz	0.3	UI

Table 4–14. Arria GX Device DC Operating Conditions (Part 2 of 2) *(Note 1)*

Symbol	Parameter	Conditions	Device	Min	Typ	Max	Units
R_{CONF} *(4)*	Value of I/O pin pull-up resistor before and during configuration	V_i = 0, V_{CCIO} = 3.3 V	—	10	25	50	kΩ
		V_i = 0, V_{CCIO} = 2.5 V	—	15	35	70	kΩ
		V_i = 0, V_{CCIO} = 1.8 V	—	30	50	100	kΩ
		V_i = 0, V_{CCIO} = 1.5 V	—	40	75	150	kΩ
		V_i = 0, V_{CCIO} = 1.2 V	—	50	90	170	kΩ
	Recommended value of I/O pin external pull-down resistor before and during configuration	—	—	—	1	2	kΩ

Notes to Table 4–14:

(1) Typical values are for T_A = 25 °C, V_{CCINT} = 1.2 V, and V_{CCIO} = 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

(2) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, 1.5, and 1.2 V).

(3) Maximum values depend on the actual TJ and design utilization. For maximum values, refer to the Excel-based PowerPlay Early Power Estimator (available at PowerPlay Early Power Estimators (EPE) and Power Analyzer) or the Quartus® II PowerPlay Power Analyzer feature for maximum values. For more information, refer to "Power Consumption" on page 4–25.

(4) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.

I/O Standard Specifications

Table 4–15 through Table 4–38 show the Arria GX device family I/O standard specifications.

Table 4–15. LVTTL Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO} *(1)*	Output supply voltage	—	3.135	3.465	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.3	0.8	V
V_{OH}	High-level output voltage	I_{OH} = –4 mA *(2)*	2.4	—	V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA *(2)*	—	0.45	V

Notes to Table 4–15:

(1) Arria GX devices comply to the narrow range for the supply voltage as specified in the EIA/JEDEC Standard, JESD8-B.

(2) This specification is supported across all the programmable drive strength settings available for this I/O standard.

Table 4–16. LVCMOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO} *(1)*	Output supply voltage	—	3.135	3.465	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.3	0.8	V
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, I_{OH} = –0.1 mA *(2)*	V_{CCIO} – 0.2	—	V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, I_{OL} = 0.1 mA *(2)*	—	0.2	V

Notes to Table 4–16:

(1) Arria GX devices comply to the narrow range for the supply voltage as specified in the EIA/JEDEC Standard, JESD8-B.

(2) This specification is supported across all the programmable drive strength available for this I/O standard.

Bus Hold Specifications

Table 4–39 shows the Arria GX device family bus hold specifications.

Table 4–39. Bus Hold Parameters

Parameter	Conditions	V_{CCIO} Level										Units
		1.2 V		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	$V_{IN} > V_{IL}$ (maximum)	22.5	—	25	—	30	—	50	—	70	—	µA
High sustaining current	$V_{IN} < V_{IH}$ (minimum)	–22.5	—	–25	—	–30	—	–50	—	–70	—	µA
Low overdrive current	0 V $< V_{IN} < V_{CCIO}$	—	120	—	160	—	200	—	300	—	500	µA
High overdrive current	0 V < $V_{IN} < V_{CCIO}$	—	–120	—	–160	—	–200	—	–300	—	–500	µA
Bus-hold trip point	—	0.45	0.95	0.5	1.0	0.68	1.07	0.7	1.7	0.8	2.0	V

On-Chip Termination Specifications

Table 4–40 and Table 4–41 define the specification for internal termination resistance tolerance when using series or differential on-chip termination.

Table 4–40. Series On-Chip Termination Specification for Top and Bottom I/O Banks

Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	Industrial Max	Units
25-Ω R_S 3.3/2.5	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.3/2.5V	±30	±30	%
50-Ω R_S 3.3/2.5	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5V	±30	± 30	%
25-Ω R_S 1.8	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8V	±30	±30	%
50-Ω R_S 1.8	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8V	±30	±30	%
50-Ω R_S 1.5	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.5V	±36	±36	%
50-Ω R_S 1.2	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2V	±50	±50	%

Table 4–66. EP1AGX60 Row Pins Input Timing Parameters (Part 2 of 3)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
1.8 V	GCLK	t_{SU}	1.477	1.477	3.275	ns
		t_H	–1.372	–1.372	–2.998	ns
	GCLK PLL	t_{SU}	3.049	3.049	6.718	ns
		t_H	–2.944	–2.944	–6.441	ns
1.5 V	GCLK	t_{SU}	1.480	1.480	3.370	ns
		t_H	–1.375	–1.375	–3.093	ns
	GCLK PLL	t_{SU}	3.052	3.052	6.813	ns
		t_H	–2.947	–2.947	–6.536	ns
SSTL-2 CLASS I	GCLK	t_{SU}	1.237	1.237	2.566	ns
		t_H	–1.132	–1.132	–2.289	ns
	GCLK PLL	t_{SU}	2.800	2.800	5.990	ns
		t_H	–2.695	–2.695	–5.713	ns
SSTL-2 CLASS II	GCLK	t_{SU}	1.237	1.237	2.566	ns
		t_H	–1.132	–1.132	–2.289	ns
	GCLK PLL	t_{SU}	2.800	2.800	5.990	ns
		t_H	–2.695	–2.695	–5.713	ns
SSTL-18 CLASS I	GCLK	t_{SU}	1.255	1.255	2.649	ns
		t_H	–1.150	–1.150	–2.372	ns
	GCLK PLL	t_{SU}	2.827	2.827	6.092	ns
		t_H	–2.722	–2.722	–5.815	ns
SSTL-18 CLASS II	GCLK	t_{SU}	1.255	1.255	2.649	ns
		t_H	–1.150	–1.150	–2.372	ns
	GCLK PLL	t_{SU}	2.827	2.827	6.092	ns
		t_H	–2.722	–2.722	–5.815	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	1.255	1.255	2.649	ns
		t_H	–1.150	–1.150	–2.372	ns
	GCLK PLL	t_{SU}	2.827	2.827	6.092	ns
		t_H	–2.722	–2.722	–5.815	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	1.255	1.255	2.649	ns
		t_H	–1.150	–1.150	–2.372	ns
	GCLK PLL	t_{SU}	2.827	2.827	6.092	ns
		t_H	–2.722	–2.722	–5.815	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.281	1.281	2.777	ns
		t_H	–1.176	–1.176	–2.500	ns
	GCLK PLL	t_{SU}	2.853	2.853	6.220	ns
		t_H	–2.748	–2.748	–5.943	ns

Table 4–96 lists clock timing specifications.

Table 4–96. EP1AGX90 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.904	1.904	4.376	ns
t_{COUT}	1.904	1.904	4.376	ns
t_{PLLCIN}	–0.153	–0.153	0.254	ns
$t_{PLLCOUT}$	–0.153	–0.153	0.254	ns

Table 4–97 through Table 4–98 list the RCLK clock timing parameters for EP1AGX90 devices.

Table 4–97 lists clock timing specifications.

Table 4–97. EP1AGX90 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.462	1.462	3.407	ns
t_{COUT}	1.467	1.467	3.401	ns
t_{PLLCIN}	–0.430	–0.430	–0.322	ns
$t_{PLLCOUT}$	–0.425	–0.425	–0.328	ns

Table 4–98 lists clock timing specifications.

Table 4–98. EP1AGX90 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.760	1.760	4.011	ns
t_{COUT}	1.760	1.760	4.011	ns
t_{PLLCIN}	–0.118	–0.118	0.303	ns
$t_{PLLCOUT}$	–0.118	–0.118	0.303	ns

Block Performance

Table 4–99 shows the Arria GX performance for some common designs. All performance values were obtained with the Quartus II software compilation of library of parameterized modules (LPM) or MegaCore functions for finite impulse response (FIR) and fast Fourier transform (FFT) designs.

Table 4–107. Arria GX Maximum Output Clock Rate for Dedicated Clock Pins (Part 3 of 4)

I/O Standards	Drive Strength	–6 Speed Grade	Units
DIFFERENTIAL 1.8-V SSTL CLASS I	4 mA	140	MHz
	6 mA	186	MHz
	8 mA	280	MHz
	10 mA	373	MHz
	12 mA	373	MHz
DIFFERENTIAL 1.8-V SSTL CLASS II	8 mA	140	MHz
	16 mA	327	MHz
	18 mA	373	MHz
	20 mA	420	MHz
DIFFERENTIAL 1.8-V HSTL CLASS I	4 mA	280	MHz
	6 mA	420	MHz
	8 mA	561	MHz
	10 mA	561	MHz
	12 mA	607	MHz
DIFFERENTIAL 1.8-V HSTL CLASS II	16 mA	420	MHz
	18 mA	467	MHz
	20 mA	514	MHz
DIFFERENTIAL 1.5-V HSTL CLASS I	4 mA	280	MHz
	6 mA	420	MHz
	8 mA	561	MHz
	10 mA	607	MHz
	12 mA	654	MHz
DIFFERENTIAL 1.5-V HSTL CLASS II	16 mA	514	MHz
	18 mA	561	MHz
	20 mA	561	MHz
	24 mA	278	MHz
3.3-V PCI	—	626	MHz
3.3-V PCI-X	—	626	MHz
LVDS	—	280	MHz
HYPERTRANSPORT	—	116	MHz
LVPECL	—	280	MHz
3.3-V LVTTL	SERIES_25_OHMS	327	MHz
	SERIES_50_OHMS	327	MHz
3.3-V LVCMOS	SERIES_25_OHMS	280	MHz
	SERIES_50_OHMS	280	MHz
2.5 V	SERIES_25_OHMS	280	MHz
	SERIES_50_OHMS	280	MHz
1.8 V	SERIES_25_OHMS	420	MHz
	SERIES_50_OHMS	420	MHz

Table 4–110. Maximum DCD for DDIO Output on Row I/O Pins Without PLL in the Clock Path *Note (1)*

Maximum DCD (ps) for Row DDIO Output I/O Standard	Input I/O Standard (No PLL in the Clock Path)					Units
	TTL/CMOS		SSTL-2	SSTL/HSTL	LVDS	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	3.3V	
LVDS	180	180	180	180	180	ps

Note to Table 4–110:

(1) Table 4–110 assumes the input clock has zero DCD.

Table 4–111. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path *(Note 1)*

Maximum DCD (ps) for DDIO Column Output I/O Standard	Input IO Standard (No PLL in the Clock Path)				Units
	TTL/CMOS		SSTL-2	SSTL/HSTL	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	
3.3-V LVTTL	440	495	170	160	ps
3.3-V LVCMOS	390	450	120	110	ps
2.5 V	375	430	105	95	ps
1.8 V	325	385	90	100	ps
1.5-V LVCMOS	430	490	160	155	ps
SSTL-2 Class I	355	410	85	75	ps
SSTL-2 Class II	350	405	80	70	ps
SSTL-18 Class I	335	390	65	65	ps
SSTL-18 Class II	320	375	70	80	ps
1.8-V HSTL Class I	330	385	60	70	ps
1.8-V HSTL Class II	330	385	60	70	ps
1.5-V HSTL Class I	330	390	60	70	ps
1.5-V HSTL Class II	330	360	90	100	ps
LVPECL	180	180	180	180	ps

Note to Table 4–111:

(1) Table 4–111 assumes the input clock has zero DCD.

Table 4–112. Maximum DCD for DDIO Output on Row I/O Pins With PLL in the Clock Path

Maximum DCD (ps) for Row DDIO Output I/O Standard	Arria GX Devices (PLL Output Feeding DDIO)	Units
	–6 Speed Grade	
3.3-V LVTTL	105	ps
3.3-V LVCMOS	75	ps
2.5V	90	ps
1.8V	100	ps
1.5-V LVCMOS	100	ps
SSTL-2 Class I	75	ps
SSTL-2 Class II	70	ps

Table 4–112. Maximum DCD for DDIO Output on Row I/O Pins With PLL in the Clock Path

Maximum DCD (ps) for Row DDIO Output I/O Standard	Arria GX Devices (PLL Output Feeding DDIO)	Units
	–6 Speed Grade	
SSTL-18 Class I	65	ps
1.8-V HSTL Class I	70	ps
1.5-V HSTL Class I	70	ps
LVDS	180	ps

Table 4–113. Maximum DCD for DDIO Output on Column I/O Pins With PLL in the Clock Path

Maximum DCD (ps) for Column DDIO Output I/O Standard	Arria GX Devices (PLL Output Feeding DDIO)	Units
	–6 Speed Grade	
3.3-V LVTTL	160	ps
3.3-V LVCMOS	110	ps
2.5V	95	ps
1.8V	100	ps
1.5-V LVCMOS	155	ps
SSTL-2 Class I	75	ps
SSTL-2 Class II	70	ps
SSTL-18 Class I	65	ps
SSTL-18 Class II	80	ps
1.8-V HSTL Class I	70	ps
1.8-V HSTL Class II	70	ps
1.5-V HSTL Class I	70	ps
1.5-V HSTL Class II	100	ps
1.2-V HSTL	155	ps
LVPECL	180	ps

High-Speed I/O Specifications

Table 4–114 lists high-speed timing specifications definitions.

Table 4–114. High-Speed Timing Specifications and Definitions (Part 1 of 2)

High-Speed Timing Specifications	Definitions
t_C	High-speed receiver/transmitter input and output clock period.
f_{HSCLK}	High-speed receiver/transmitter input and output clock frequency.
J	Deserialization factor (width of parallel data bus).
W	PLL multiplication factor.
t_{RISE}	Low-to-high transmission time.
t_{FALL}	High-to-low transmission time.

Table 4–114. High-Speed Timing Specifications and Definitions (Part 2 of 2)

High-Speed Timing Specifications	Definitions
Timing unit interval (TUI)	The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency × Multiplication Factor) = t_C/w).
f_{HSDR}	Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
$f_{HSDRDPA}$	Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
Channel-to-channel skew (TCCS)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
Sampling window (SW)	The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window.
Input jitter	Peak-to-peak input jitter on high-speed PLLs.
Output jitter	Peak-to-peak output jitter on high-speed PLLs.
t_{DUTY}	Duty cycle on high-speed transmitter output clock.
t_{LOCK}	Lock time for high-speed transmitter and receiver PLLs.

Table 4–115 shows the high-speed I/O timing specifications.

Table 4–115. High-Speed I/O Specifications (Part 1 of 2) *Note (1), (2)*

Symbol	Conditions	–6 Speed Grade			Units
		Min	Typ	Max	
f_{HSCLK} (clock frequency) $f_{HSCLK} = f_{HSDR} / W$	W = 2 to 32 (LVDS, HyperTransport technology) *(3)*	16	—	420	MHz
	W = 1 (SERDES bypass, LVDS only)	16	—	500	MHz
	W = 1 (SERDES used, LVDS only)	150	—	640	MHz
f_{HSDR} (data rate)	J = 4 to 10 (LVDS, HyperTransport technology)	150	—	840	Mbps
	J = 2 (LVDS, HyperTransport technology)	*(4)*	—	700	Mbps
	J = 1 (LVDS only)	*(4)*	—	500	Mbps
$f_{HSDRDPA}$ (DPA data rate)	J = 4 to 10 (LVDS, HyperTransport technology)	150	—	840	Mbps
TCCS	All differential I/O standards	—	—	200	ps
SW	All differential I/O standards	440	—	—	ps
Output jitter	—	—	—	190	ps
Output t_{RISE}	All differential I/O standards	—	—	290	ps
Output t_{FALL}	All differential I/O standards	—	—	290	ps
t_{DUTY}	—	45	50	55	%
DPA run length	—	—	—	6,400	UI
DPA jitter tolerance	Data channel peak-to-peak jitter	0.44	—	—	UI

5. Reference and Ordering Information

AGX51005-2.0

Software

Arria® GX devices are supported by the Altera® Quartus® II design software, which provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap® II logic analyzer, and device configuration.

For more information about the Quartus II software features, refer to the *Quartus II Development Software Handbook* .

The Quartus II software supports the Windows XP/2000/NT, Sun Solaris 8/9, Linux Red Hat v7.3, Linux Red Hat Enterprise 3, and HP-UX operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink interface.

Device Pin-Outs

Arria GX device pin-outs are available on the Altera web site at www.altera.com.

Ordering Information

Figure 5–1 describes the ordering codes for Arria GX devices.

For more information on a specific package, refer to the *Package Information for Arria GX Devices* chapter.