Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	2508
Number of Logic Elements/Cells	50160
Total RAM Bits	2475072
Number of I/O	350
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep1agx50df780i6

- Main device features:
  - TriMatrix memory consisting of three RAM block sizes to implement true dual-port memory and first-in first-out (FIFO) buffers with performance up to 380 MHz
  - Up to 16 global clock networks with up to 32 regional clock networks per device
  - High-speed DSP blocks provide dedicated implementation of multipliers, multiply-accumulate functions, and finite impulse response (FIR) filters
  - Up to four enhanced phase-locked loops (PLLs) per device provide spread spectrum, programmable bandwidth, clock switch-over, and advanced multiplication and phase shifting
  - Support for numerous single-ended and differential I/O standards
  - High-speed source-synchronous differential I/O support on up to 47 channels
  - Support for source-synchronous bus standards, including SPI-4 Phase 2 (POS-PHY Level 4), SFI-4.1, XSBI, UTOPIA IV, NPSI, and CSIX-L1
  - Support for high-speed external memory including DDR and DDR2 SDRAM, and SDR SDRAM
  - Support for multiple intellectual property megafunctions from Altera® MegaCore® functions and Altera Megafunction Partners Program (AMPP^{SM})
  - Support for remote configuration updates

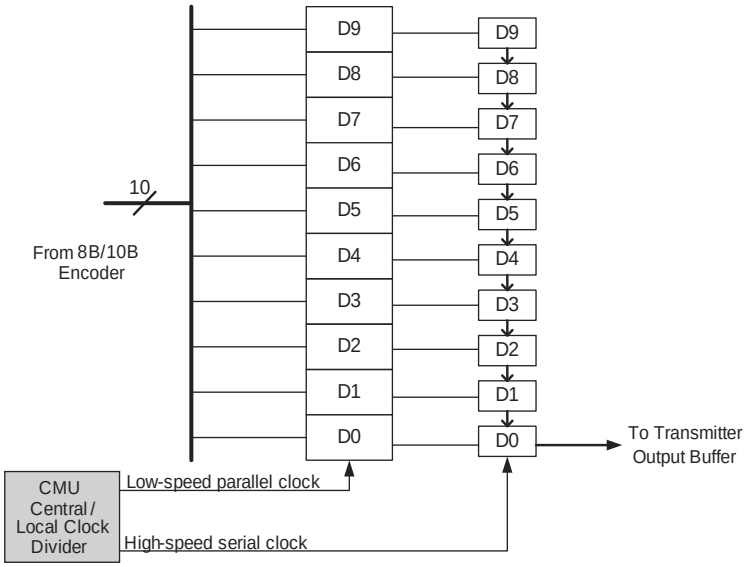
Table 1–1 lists Arria GX device features for FineLine BGA (FBGA) with flip chip packages.

Table 1–1. Arria GX Device Features (Part 1 of 2)

Feature	EP1AGX20C	EP1AGX35C/D		EP1AGX50C/D		EP1AGX60C/D/E			EP1AGX90E
	C	C	D	C	D	C	D	E	E
Package	484-pin, 780-pin (Flip chip)	484-pin (Flip chip)	780-pin (Flip chip)	484-pin (Flip chip)	780-pin, 1152-pin (Flip chip)	484-pin (Flip chip)	780-pin (Flip chip)	1152-pin (Flip chip)	1152-pin (Flip chip)
ALMs	8,632	13,408		20,064		24,040			36,088
Equivalent logic elements (LEs)	21,580	33,520		50,160		60,100			90,220
Transceiver channels	4	4	8	4	8	4	8	12	12
Transceiver data rate	600 Mbps to 3.125 Gbps	600 Mbps to 3.125 Gbps		600 Mbps to 3.125 Gbps		600 Mbps to 3.125 Gbps			600 Mbps to 3.125 Gbps
Source-synchronous receive channels	31	31	31	31	31, 42	31	31	42	47

Figure 2–7 shows the serializer block diagram.

Figure 2–7. Serializer



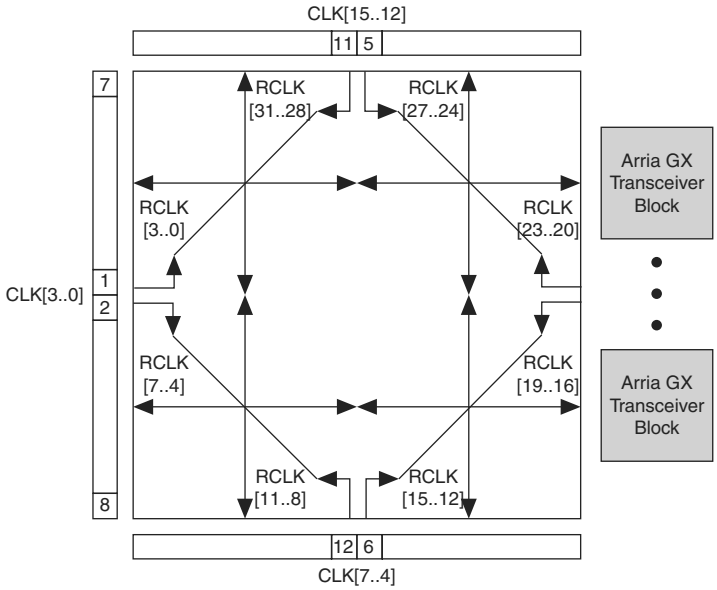
Transmitter Buffer

The Arria GX transceiver buffers support the 1.2- and 1.5-V PCML I/O standard at rates up to 3.125 Gbps. The common mode voltage (V_{CM}) of the output driver may be set to 600 or 700 mV.

For more information about the Arria GX transceiver buffers, refer to the *Arria GX Transceiver Architecture* chapter.

The output buffer, as shown in Figure 2–8, is directly driven by the high-speed data serializer and consists of a programmable output driver, a programmable pre-emphasis circuit, and OCT circuitry.

Figure 2–24. Regional Clock Resources in Arria GX Devices



For the RCLK or GCLK network to route into the transceiver, a local route input output (LRIO) channel is required. Each LRIO clock region has up to eight clock paths and each transceiver block has a maximum of eight clock paths for connecting with LRIO clocks. These resources are limited and determine the number of clocks that can be used between the PLD and transceiver blocks. Table 2–7 and Table 2–8 list the number of LRIO resources available for Arria GX devices with different numbers of transceiver blocks.

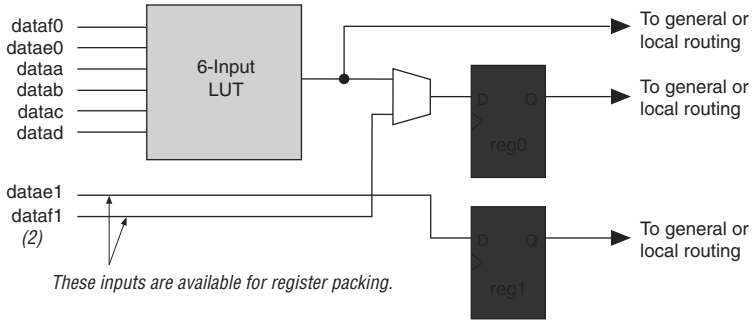
Table 2–7. Available Clocking Connections for Transceivers in EP1AGX35D, EP1AGX50D, and EP1AGX60D

Source	Clock Resource		Transceiver	
	Global Clock	Regional Clock	Bank13 8 Clock I/O	Bank14 8 Clock I/O
Region0 8 LRIO clock	✓	RCLK 20-27	✓	—
Region1 8 LRIO clock	✓	RCLK 12-19	—	✓

Table 2–8. Available Clocking Connections for Transceivers in EP1AGX60E and EP1AGX90E

Source	Clock Resource		Transceiver		
	Global Clock	Regional Clock	Bank13 8 Clock I/O	Bank14 8 Clock I/O	Bank15 8 Clock I/O
Region0 8 LRIO clock	✓	RCLK 20-27	✓	—	—
Region1 8 LRIO clock	✓	RCLK 20-27	✓	✓	—
Region2 8 LRIO clock	✓	RCLK 12-19	—	✓	✓
Region3 8 LRIO clock	✓	RCLK 12-19	—	—	✓

Figure 2–32. Six-Input Function in Normal Mode *Note (1), (2)*



Notes to Figure 2–32:

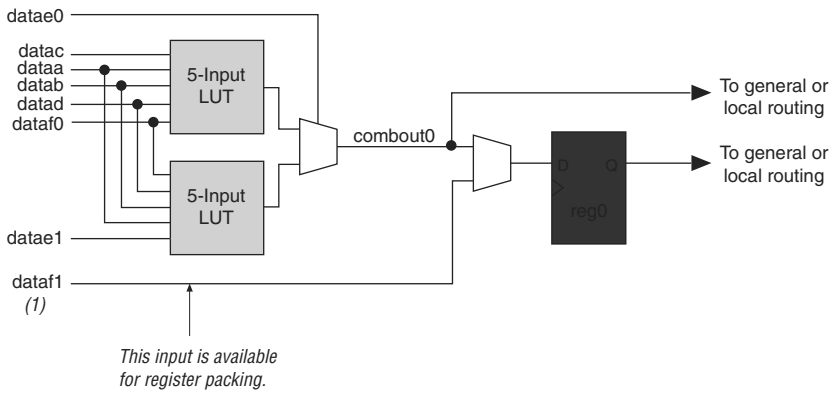
(1) If `datae1` and `dataf1` are used as inputs to the six-input function, `datae0` and `dataf0` are available for register packing.

(2) The `dataf1` input is available for register packing only if the six-input function is un-registered.

Extended LUT Mode

Extended LUT mode is used to implement a specific set of seven-input functions. The set must be a 2-to-1 multiplexer fed by two arbitrary five-input functions sharing four inputs. Figure 2–33 shows the template of supported seven-input functions utilizing extended LUT mode. In this mode, if the seven-input function is unregistered, the unused eighth input is available for register packing. Functions that fit into the template shown in Figure 2–33 occur naturally in designs. These functions often appear in designs as "if-else" statements in Verilog HDL or VHDL code.

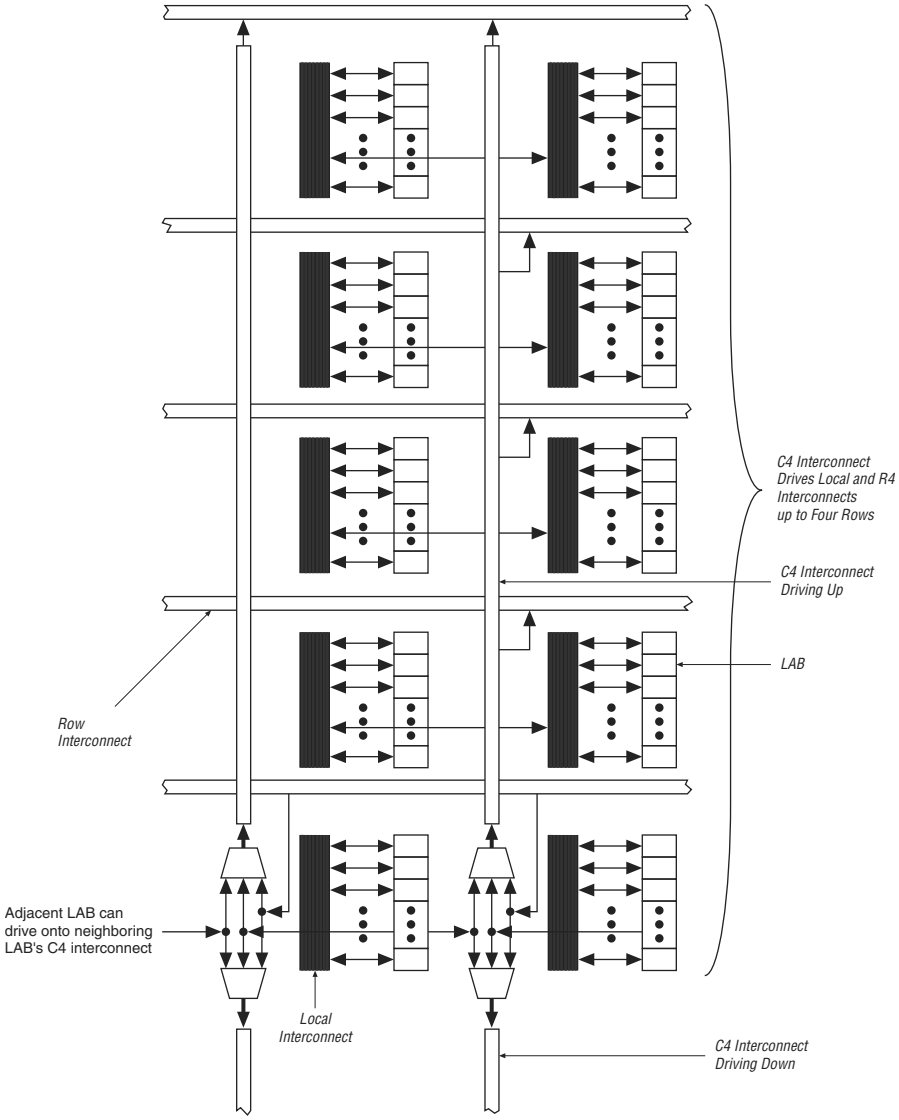
Figure 2–33. Template for Supported Seven-Input Functions in Extended LUT Mode



Note to Figure 2–33:

(1) If the seven-input function is unregistered, the unused eighth input is available for register packing. The second register, `reg1`, is not available.

Figure 2–41. C4 Interconnect Connections *(Note 1)*



Note to Figure 2–41:

(1) Each C4 interconnect can drive either up or down four rows.

C16 column interconnects span a length of 16 LABs and provide the fastest resource for long column connections between LABs, TriMatrix memory blocks, DSP blocks, and IOEs. C16 interconnects can cross M-RAM blocks and also drive to row and column interconnects at every fourth LAB. C16 interconnects drive LAB local interconnects via C4 and R4 interconnects and do not drive LAB local interconnects directly. All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (that is, TriMatrix memory and DSP blocks) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB. All blocks are fed by the row LAB clocks, `labclk[5..0]`.

Figure 2–49. M-RAM Row Unit Interface to Interconnect

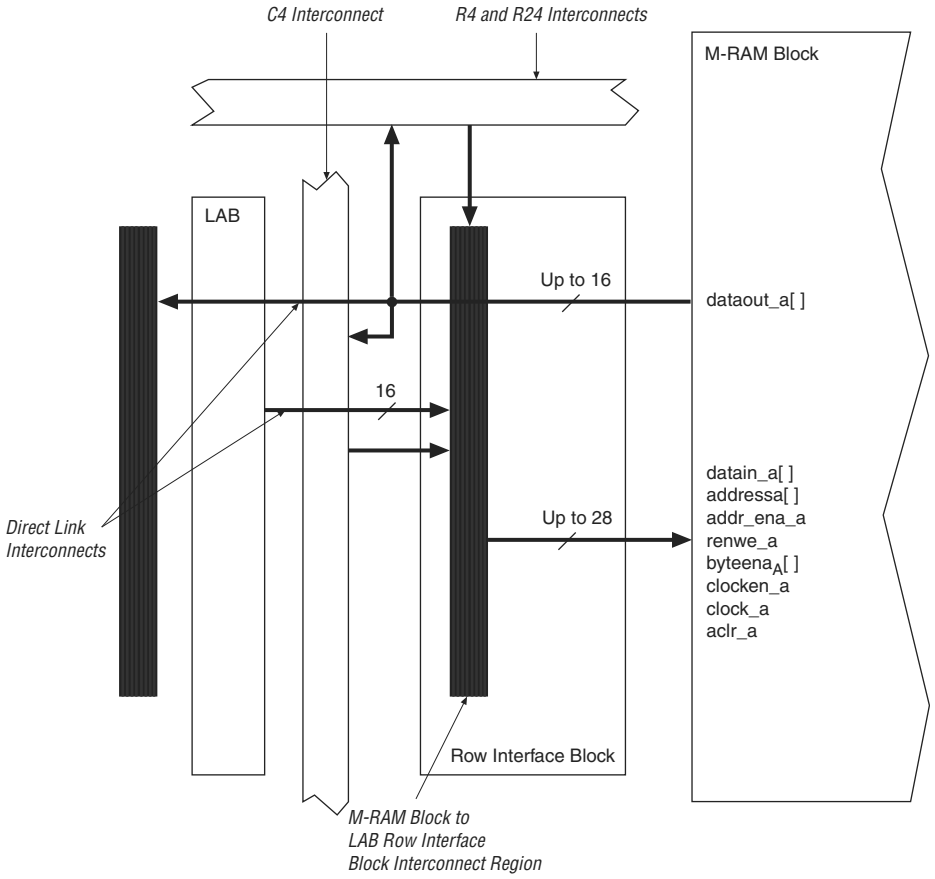


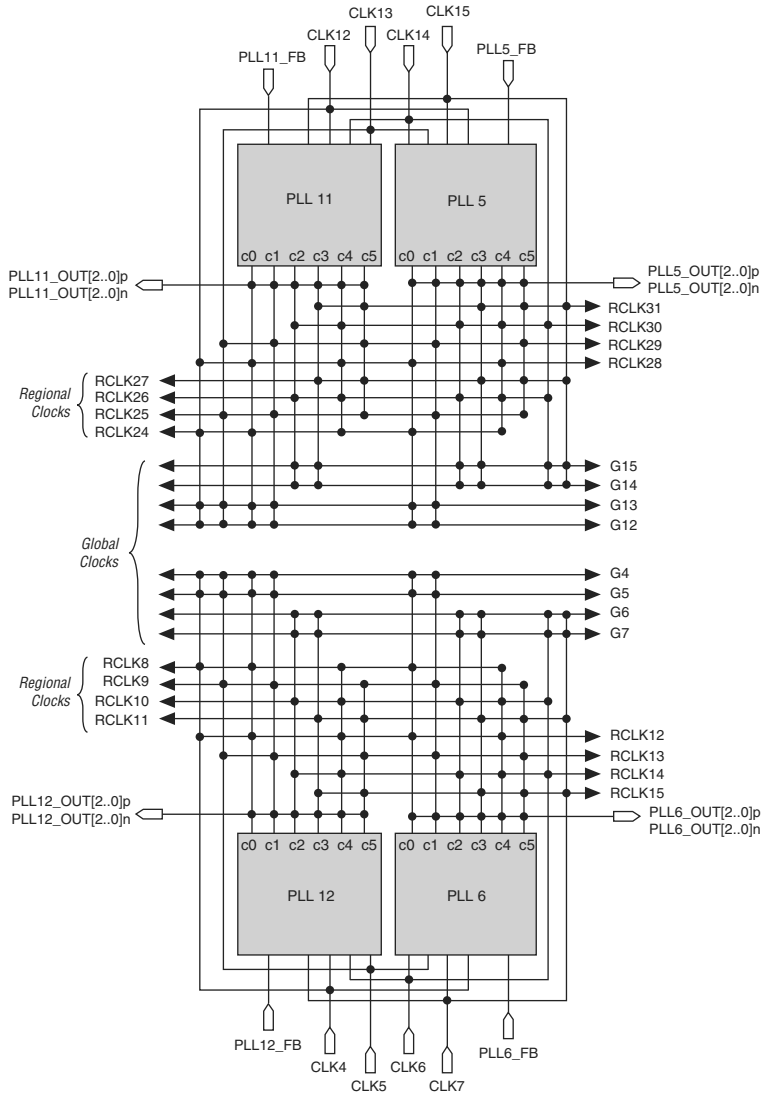
Table 2–12 lists the input and output data signal connections along with the address and control signal input connections to the row unit interfaces (L0 to L5 and R0 to R5).

Table 2–12. M-RAM Row Interface Unit Signals (Part 1 of 2)

Unit Interface Block	Input Signals	Output Signals
L0	datain_a[14..0] byteena_a[1..0]	dataout_a[11..0]
L1	datain_a[29..15] byteena_a[3..2]	dataout_a[23..12]
L2	datain_a[35..30] addressa[4..0] addr_ena_a clock_a clocken_a renwe_a aclr_a	dataout_a[35..24]
L3	addressa[15..5] datain_a[41..36]	dataout_a[47..36]

Figure 2–64 shows the global and regional clocking from enhanced PLL outputs and top and bottom CLK pins.

Figure 2–64. Global and Regional Clock Connections from Top and Bottom Clock Pins and Enhanced PLL Outputs *(Note 1)*



Note to Figure 2–64:

(1) If the design uses the feedback input, you might lose one (or two if FBIN is differential) external clock output pin.

The connections to the global and regional clocks from the top clock pins and enhanced PLL outputs are shown in Table 2–20. The connections to the clocks from the bottom clock pins are shown in Table 2–21.

Configuring Arria GX FPGAs with JRunner

The JRunner software driver configures Altera FPGAs, including Arria GX FPGAs, through the ByteBlaster™ II or ByteBlasterMV cables in JTAG mode. The programming input file supported is in Raw Binary File (**.rbf**) format. JRunner also requires a Chain Description File (**.cdf**) generated by the Quartus II software. JRunner is targeted for embedded JTAG configuration. The source code is developed for the Windows NT operating system (OS), but can be customized to run on other platforms.

For more information about the JRunner software driver, refer to the *AN414: JRunner Software Driver: An Embedded Solution for PLD JTAG Configuration* and the source files on the Altera website.

Programming Serial Configuration Devices with SRunner

You can program a serial configuration device in-system by an external microprocessor using SRunner™. SRunner is a software driver developed for embedded serial configuration device programming that can be easily customized to fit into different embedded systems. SRunner software driver reads a raw programming data file (**.rpd**) and writes to serial configuration devices. The serial configuration device programming time using SRunner software driver is comparable to the programming time when using the Quartus II software.

For more information about SRunner, refer to the *AN418: SRunner: An Embedded Solution for Serial Configuration Device Programming* and the source code on the Altera website.

For more information about programming serial configuration devices, refer to the *Serial Configuration Devices (EPCS1, EPCS4, EPCS64, and EPCS128) Data Sheet* in the *Configuration Handbook*.

Configuring Arria GX FPGAs with the MicroBlaster Driver

The MicroBlaster™ software driver supports a raw binary file (RBF) programming input file and is ideal for embedded FPP or PS configuration. The source code is developed for the Windows NT operating system, although it can be customized to run on other operating systems.

For more information about the MicroBlaster software driver, refer to the *Configuring the MicroBlaster Fast Passive Parallel Software Driver White Paper* or the *AN423: Configuring the MicroBlaster Passive Serial Software Driver*.

PLL Reconfiguration

The phase-locked loops (PLLs) in the Arria GX device family support reconfiguration of their multiply, divide, VCO-phase selection, and bandwidth selection settings without reconfiguring the entire device. You can use either serial data from the logic array or regular I/O pins to program the PLL's counter settings in a serial chain. This option provides considerable flexibility for frequency synthesis, allowing real-time variation of the PLL frequency and delay. The rest of the device is functional while reconfiguring the PLL.

Table 4–6. Arria GX Transceiver Block AC Specification (Part 2 of 3)

Symbol / Description	Conditions	–6 Speed Grade Commercial and Industrial			Units
		Min	Typ	Max	
Bandwidth at 2.5 Gbps	BW = Low	—	35	—	MHz
	BW = Med	—	50	—	
	BW = High	—	60	—	
Return loss differential mode	50 MHz to 1.25 GHz (PCI Express)	–10			dB
	100 MHz to 2.5 GHz (XAUI)				
Return loss common mode	50 MHz to 1.25 GHz (PCI Express)	–6			dB
	100 MHz to 2.5 GHz (XAUI)				
Programmable PPM detector *(5)*	—	± 62.5, 100, 125, 200, 250, 300, 500, 1000			PPM
Run length *(6)*	—	80			UI
Programmable equalization	—	—	—	5	dB
Signal detect/loss threshold *(7)*	—	65	—	175	mV
CDR LTR TIme *(8)*, *(9)*	—	—	—	75	us
CDR Minimum T1b *(9)*, *(10)*	—	15	—	—	us
LTD lock time *(9)*, *(11)*	—	0	100	4000	ns
Data lock time from `rx_freqlocked` *(9)*, *(12)*	—	—	—	4	us
Programmable DC gain	—	0, 3, 6			dB
Transmitter Buffer					
Output Common Mode voltage (V_{ocm})	—	580 ± 10%			mV
On-chip termination resistors	—	108±10%			Ω
Return loss differential mode	50 MHz to 1.25 GHz (PCI Express)	–10			dB
	312 MHz to 625 MHz (XAUI)				
	625 MHz to 3.125GHz (XAUI)	–10			$\frac{dB}{decade\ slope}$
Return loss common mode	50 MHz to 1.25 GHz (PCI Express)	–6			dB
Rise time	—	35	—	65	ps
Fall time	—	35	—	65	ps
Intra differential pair skew	V_{OD} = 800 mV	—	—	15	ps
Intra-transceiver block skew (×4) *(13)*	—	—	—	100	ps

Table 4–7. Arria GX Transceiver Block AC Specification *(Note 1), (2), (3)* (Part 2 of 4)

Description	Condition	–6 Speed Grade Commercial & Industrial	Units
Deterministic jitter at 3.125 Gbps	REFCLK = 156.25 MHz Pattern = CJPAT V_{OD} = 1200 mV No Pre-emphasis	0.17	UI
XAUI Receiver Jitter Tolerance *(4)*			
Total jitter	Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.65	UI
Deterministic jitter	Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.37	UI
Peak-to-peak jitter	Jitter frequency = 22.1 KHz	> 8.5	UI
Peak-to-peak jitter	Jitter frequency = 1.875 MHz	> 0.1	UI
Peak-to-peak jitter	Jitter frequency = 20 MHz	> 0.1	UI
PCI Express (PIPE) Transmitter Jitter Generation *(5)*			
Total Transmitter Jitter Generation	Compliance Pattern; V_{OD} = 800 mV; Pre-emphasis = 49%	< 0.25	UI p-p
PCI Express (PIPE) Receiver Jitter Tolerance *(5)*			
Total Receiver Jitter Tolerance	Compliance Pattern; DC Gain = 3 db	> 0.6	UI p-p
Gigabit Ethernet (GIGE) Transmitter Jitter Generation *(7)*			
Total Transmitter Jitter Generation (TJ)	CRPAT: V_{OD} = 800 mV; Pre-emphasis = 0%	< 0.279	UI p-p
Deterministic Transmitter Jitter Generation (DJ)	CRPAT; V_{OD} = 800 mV; Pre-emphasis = 0%	< 0.14	UI p-p
Gigabit Ethernet (GIGE) Receiver Jitter Tolerance			
Total Jitter Tolerance	CJPAT Compliance Pattern; DC Gain = 0 dB	> 0.66	UI p-p
Deterministic Jitter Tolerance	CJPAT Compliance Pattern; DC Gain = 0 dB	> 0.4	UI p-p
Serial RapidIO (1.25 Gbps, 2.5 Gbps, and 3.125 Gbps) Transmitter Jitter Generation *(6)*			
Total Transmitter Jitter Generation (TJ)	CJPAT Compliance Pattern; V_{OD} = 800 mV; Pre-emphasis = 0%	< 0.35	UI p-p
Deterministic Transmitter Jitter Generation (DJ)	CJPAT Compliance Pattern; V_{OD} = 800 mV; Pre-emphasis = 0%	< 0.17	UI p-p

Table 4–8 and Table 4–9 list the transmitter and receiver PCS latency for each mode, respectively.

Table 4–8. PCS Latency *(Note 1)*

Functional Mode	Configuration	Transmitter PCS Latency					
		TX PIPE	TX Phase Comp FIFO	Byte Serializer	TX State Machine	8B/10B Encoder	Sum *(2)*
XAUI	—	—	2–3	1	0.5	0.5	4–5
PIPE	×1, ×4, ×8 8-bit channel width	1	3–4	1	—	1	6–7
	×1, ×4, ×8 16-bit channel width	1	3–4	1	—	0.5	6–7
GIGE	—	—	2–3	1	—	1	4–5
Serial RapidIO	1.25 Gbps, 2.5 Gbps, 3.125 Gbps	—	2–3	1	—	0.5	4–5
SDI	HD10-bit channel width	—	2–3	1	—	1	4–5
	HD, 3G 20-bit channel width	—	2–3	1	—	0.5	4–5
BASIC Single Width	8-bit/10-bit channel width	—	2–3	1	—	1	4–5
	16-bit/20-bit channel width	—	2–3	1	—	0.5	4–5

Notes to Table 4–8:

(1) The latency numbers are with respect to the PLD-transceiver interface clock cycles.

(2) The total latency number is rounded off in the Sum column.

Table 4–9. PCS Latency (Part 1 of 2) (Part 1 of 2)

Functional Mode	Configuration	Receiver PCS Latency									
		Word Aligner	Deskew FIFO	Rate Matcher *(3)*	8B/10B Decoder	Receiver State Machine	Byte Deserializer	Byte Order	Receiver Phase Comp FIFO	Receiver PIPE	Sum *(2)*
XAUI	—	2–2.5	2–2.5	5.5–6.5	0.5	1	1	1	1–2	—	14–17
PIPE	×1, ×4 8-bit channel width	4–5	—	11–13	1	—	1	1	2–3	1	21–25
	×1, ×4 16-bit channel width	2–2.5	—	5.5–6.5	0.5	—	1	1	2–3	1	13–16
GIGE	—	4–5	—	11–13	1	—	1	1	1–2	—	19–23
Serial RapidIO	1.25 Gbps, 2.5 Gbps, 3.125 Gbps	2–2.5	—	—	0.5	—	1	1	1–2	—	6–7
SDI	HD 10-bit channel width	5	—	—	1	—	1	1	1–2	—	9–10
	HD, 3G 20-bit channel width	2.5	—	—	0.5	—	1	1	1–2	—	6–7

Table 4–17. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO} *(1)*	Output supply voltage	—	2.375	2.625	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.3	0.7	V
V_{OH}	High-level output voltage	I_{OH} = –1 mA *(2)*	2.0	—	V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA *(2)*	—	0.4	V

Notes to Table 4–17:

(1) The Arria GX device V_{CCIO} voltage level support of 2.5 to 5% is narrower than defined in the normal range of the EIA/JEDEC standard.

(2) This specification is supported across all the programmable drive settings available for this I/O standard.

Table 4–18. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO} *(1)*	Output supply voltage	—	1.71	1.89	V
V_{IH}	High-level input voltage	—	0.65 × V_{CCIO}	2.25	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(2)*	V_{CCIO} – 0.45	—	V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(2)*	—	0.45	V

Notes to Table 4–18:

(1) The Arria GX device V_{CCIO} voltage level support of 1.8 to 5% is narrower than defined in the normal range of the EIA/JEDEC standard.

(2) This specification is supported across all the programmable drive settings available for this I/O standard, as shown in *Arria GX Architecture* chapter.

Table 4–19. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO} *(1)*	Output supply voltage	—	1.425	1.575	V
V_{IH}	High-level input voltage	—	0.65 V_{CCIO}	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(2)*	0.75 V_{CCIO}	—	V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(2)*	—	0.25 V_{CCIO}	V

Notes to Table 4–19:

(1) The Arria GX device V_{CCIO} voltage level support of 1.5 to 5% is narrower than defined in the normal range of the EIA/JEDEC standard.

(2) This specification is supported across all the programmable drive settings available for this I/O standard, as shown in the *Arria GX Architecture* chapter.

Figure 4–5 and Figure 4–6 show receiver input and transmitter output waveforms, respectively, for all differential I/O standards (LVDS and LVPECL).

Figure 4–9. Measurement Setup for t_{zx}

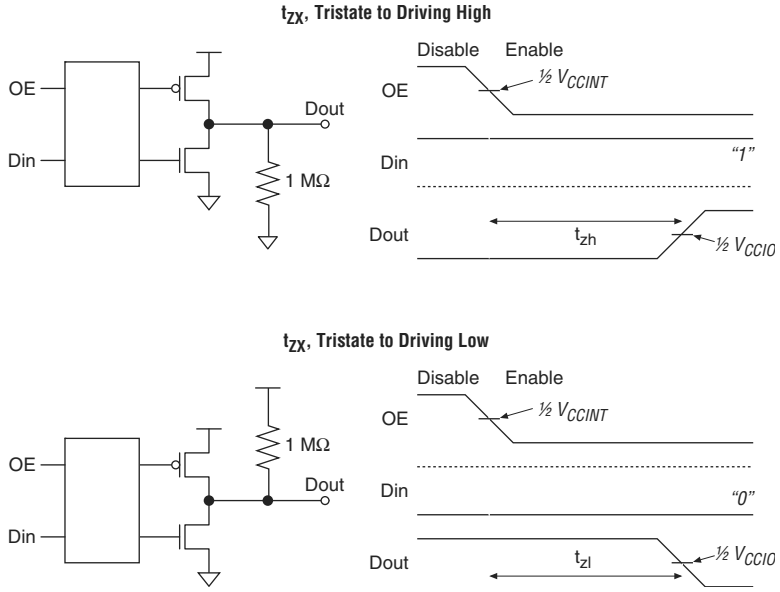


Table 4–45 specifies the input timing measurement setup.

Table 4–45. Timing Measurement Methodology for Input Pins *(Note 1)*, *(2)*, *(3)*, *(4)* (Part 1 of 2)

I/O Standard	Measurement Conditions			Measurement Point
	V_{CCIO} (V)	V_{REF} (V)	Edge Rate (ns)	VMEAS (V)
LVTTL *(5)*	3.135	—	3.135	1.5675
LVCMOS *(5)*	3.135	—	3.135	1.5675
2.5 V *(5)*	2.375	—	2.375	1.1875
1.8 V *(5)*	1.710	—	1.710	0.855
1.5 V *(5)*	1.425	—	1.425	0.7125
PCI *(6)*	2.970	—	2.970	1.485
PCI-X *(6)*	2.970	—	2.970	1.485
SSTL-2 Class I	2.325	1.163	2.325	1.1625
SSTL-2 Class II	2.325	1.163	2.325	1.1625
SSTL-18 Class I	1.660	0.830	1.660	0.83
SSTL-18 Class II	1.660	0.830	1.660	0.83
1.8-V HSTL Class I	1.660	0.830	1.660	0.83
1.8-V HSTL Class II	1.660	0.830	1.660	0.83
1.5-V HSTL Class I	1.375	0.688	1.375	0.6875
1.5-V HSTL Class II	1.375	0.688	1.375	0.6875
1.2-V HSTL with OCT	1.140	0.570	1.140	0.570
Differential SSTL-2 Class I	2.325	1.163	2.325	1.1625
Differential SSTL-2 Class II	2.325	1.163	2.325	1.1625
Differential SSTL-18 Class I	1.660	0.830	1.660	0.83

Table 4–50. EP1AGX20 Row Pins output Timing Parameters (Part 2 of 2)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.626	2.626	5.614	ns
		GCLK PLL	t_{CO}	1.207	1.207	2.542	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.602	2.602	5.538	ns
		GCLK PLL	t_{CO}	1.183	1.183	2.466	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.568	2.568	5.407	ns
		GCLK PLL	t_{CO}	1.149	1.149	2.335	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.614	2.614	5.556	ns
		GCLK PLL	t_{CO}	1.195	1.195	2.484	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.618	2.618	5.485	ns
		GCLK PLL	t_{CO}	1.199	1.199	2.413	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.594	2.594	5.468	ns
		GCLK PLL	t_{CO}	1.175	1.175	2.396	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.597	2.597	5.447	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.375	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.595	2.595	5.466	ns
		GCLK PLL	t_{CO}	1.176	1.176	2.394	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.598	2.598	5.430	ns
		GCLK PLL	t_{CO}	1.179	1.179	2.358	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.580	2.580	5.426	ns
		GCLK PLL	t_{CO}	1.161	1.161	2.354	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.584	2.584	5.415	ns
		GCLK PLL	t_{CO}	1.165	1.165	2.343	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.575	2.575	5.414	ns
		GCLK PLL	t_{CO}	1.156	1.156	2.342	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.594	2.594	5.443	ns
		GCLK PLL	t_{CO}	1.175	1.175	2.371	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.597	2.597	5.429	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.357	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.582	2.582	5.421	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.349	ns
LVDS	—	GCLK	t_{CO}	2.654	2.654	5.613	ns
		GCLK PLL	t_{CO}	1.226	1.226	2.530	ns

Table 4–55. EP1AGX35 Column Pins Input Timing Parameters (Part 2 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
2.5 V	GCLK	t_{SU}	1.261	1.261	2.897	ns
		t_H	–1.156	–1.156	–2.620	ns
	GCLK PLL	t_{SU}	2.703	2.703	6.003	ns
		t_H	–2.598	–2.598	–5.726	ns
1.8 V	GCLK	t_{SU}	1.327	1.327	3.107	ns
		t_H	–1.222	–1.222	–2.830	ns
	GCLK PLL	t_{SU}	2.769	2.769	6.213	ns
		t_H	–2.664	–2.664	–5.936	ns
1.5 V	GCLK	t_{SU}	1.330	1.330	3.200	ns
		t_H	–1.225	–1.225	–2.923	ns
	GCLK PLL	t_{SU}	2.772	2.772	6.306	ns
		t_H	–2.667	–2.667	–6.029	ns
SSTL-2 CLASS I	GCLK	t_{SU}	1.075	1.075	2.372	ns
		t_H	–0.970	–0.970	–2.095	ns
	GCLK PLL	t_{SU}	2.517	2.517	5.480	ns
		t_H	–2.412	–2.412	–5.203	ns
SSTL-2 CLASS II	GCLK	t_{SU}	1.075	1.075	2.372	ns
		t_H	–0.970	–0.970	–2.095	ns
	GCLK PLL	t_{SU}	2.517	2.517	5.480	ns
		t_H	–2.412	–2.412	–5.203	ns
SSTL-18 CLASS I	GCLK	t_{SU}	1.113	1.113	2.479	ns
		t_H	–1.008	–1.008	–2.202	ns
	GCLK PLL	t_{SU}	2.555	2.555	5.585	ns
		t_H	–2.450	–2.450	–5.308	ns
SSTL-18 CLASS II	GCLK	t_{SU}	1.114	1.114	2.479	ns
		t_H	–1.009	–1.009	–2.202	ns
	GCLK PLL	t_{SU}	2.556	2.556	5.587	ns
		t_H	–2.451	–2.451	–5.310	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	1.113	1.113	2.479	ns
		t_H	–1.008	–1.008	–2.202	ns
	GCLK PLL	t_{SU}	2.555	2.555	5.585	ns
		t_H	–2.450	–2.450	–5.308	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	1.114	1.114	2.479	ns
		t_H	–1.009	–1.009	–2.202	ns
	GCLK PLL	t_{SU}	2.556	2.556	5.587	ns
		t_H	–2.451	–2.451	–5.310	ns

Table 4–62. EP1AGX50 Row Pins Output Timing Parameters (Part 3 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.606	2.606	5.480	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.396	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.608	2.608	5.442	ns
		GCLK PLL	t_{CO}	1.181	1.181	2.360	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.590	2.590	5.438	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.356	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.594	2.594	5.427	ns
		GCLK PLL	t_{CO}	1.167	1.167	2.345	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.585	2.585	5.426	ns
		GCLK PLL	t_{CO}	1.158	1.158	2.344	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.605	2.605	5.457	ns
		GCLK PLL	t_{CO}	1.177	1.177	2.373	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.607	2.607	5.441	ns
		GCLK PLL	t_{CO}	1.180	1.180	2.359	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.592	2.592	5.433	ns
		GCLK PLL	t_{CO}	1.165	1.165	2.351	ns
LVDS	—	GCLK	t_{CO}	2.654	2.654	5.613	ns
		GCLK PLL	t_{CO}	1.226	1.226	2.530	ns

Table 4–63 lists I/O timing specifications.

Table 4–63. EP1AGX50 Column Pins Output Timing Parameters (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	2.948	2.948	6.608	ns
		GCLK PLL	t_{CO}	1.476	1.476	3.447	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.797	2.797	6.203	ns
		GCLK PLL	t_{CO}	1.331	1.331	3.075	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.722	2.722	6.204	ns
		GCLK PLL	t_{CO}	1.264	1.264	3.075	ns
3.3-V LVTTL	16 mA	GCLK	t_{CO}	2.694	2.694	6.024	ns
		GCLK PLL	t_{CO}	1.238	1.238	2.906	ns
3.3-V LVTTL	20 mA	GCLK	t_{CO}	2.670	2.670	5.896	ns
		GCLK PLL	t_{CO}	1.216	1.216	2.781	ns
3.3-V LVTTL	24 mA	GCLK	t_{CO}	2.660	2.660	5.895	ns
		GCLK PLL	t_{CO}	1.209	1.209	2.783	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.797	2.797	6.203	ns
		GCLK PLL	t_{CO}	1.331	1.331	3.075	ns

Table 4–99 lists performance notes.

Table 4–99. Arria GX Performance Notes

Applications		Resources Used			Performance
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	–6 Speed Grade
LE	16-to-1 multiplexer	5	0	0	168.41
	32-to-1 multiplexer	11	0	0	334.11
	16-bit counter	16	0	0	374.0
	64-bit counter	64	0	0	168.41
TriMatrix Memory M512 block	Simple dual-port RAM 32 x 18 bit	0	1	0	348.0
	FIFO 32 x 18 bit	0	1	0	333.22
TriMatrix Memory M4K block	Simple dual-port RAM 128 x 36 bit	0	1	0	344.71
	True dual-port RAM 128 x 18 bit	0	1	0	348.0
TriMatrix Memory MegaRAM block	Single port RAM 4K x 144 bit	0	2	0	244.0
	Simple dual-port RAM 4K x 144 bit	0	1	0	292.0
	True dual-port RAM 4K x 144 bit	0	2	0	244.0
	Single port RAM 8K x 72 bit	0	1	0	247.0
	Simple dual-port RAM 8K x 72 bit	0	1	0	292.0
	Single port RAM 16K x 36 bit	0	1	0	254.0
	Simple dual-port RAM 16K x 36 bit	0	1	0	292.0
	True dual-port RAM 16K x 36 bit	0	1	0	251.0
	Single port RAM 32K x 18 bit	0	1	0	317.36
	Simple dual-port RAM 32K x 18 bit	0	1	0	292.0
	True dual-port RAM 32K x 18 bit	0	1	0	251.0
	Single port RAM 64K x 9 bit	0	1	0	254.0
	Simple dual-port RAM 64K x 9 bit	0	1	0	292.0
	True dual-port RAM 64K x 9 bit	0	1	0	251.0

Table 4–102. Arria GX Maximum Input Toggle Rate for Column I/O Pins

I/O Standards	–6 Speed Grade	Units
SSTL-18 CLASS II	467	MHz
1.8-V HSTL CLASS I	467	MHz
1.8-V HSTL CLASS II	467	MHz
1.5-V HSTL CLASS I	467	MHz
1.5-V HSTL CLASS II	467	MHz
3.3-V PCI	420	MHz
3.3-V PCI-X	420	MHz

Table 4–103 shows the maximum input clock toggle rates for Arria GX device row I/O pins.

Table 4–103. Arria GX Maximum Input Toggle Rate for Row I/O Pins

I/O Standards	–6 Speed Grade	Units
3.3-V LVTTL	420	MHz
3.3-V LVCMOS	420	MHz
2.5 V	420	MHz
1.8 V	420	MHz
1.5 V	420	MHz
SSTL-2 CLASS I	467	MHz
SSTL-2 CLASS II	467	MHz
SSTL-18 CLASS I	467	MHz
SSTL-18 CLASS II	467	MHz
1.8-V HSTL CLASS I	467	MHz
1.8-V HSTL CLASS II	467	MHz
1.5-V HSTL CLASS I	467	MHz
1.5-V HSTL CLASS II	467	MHz
LVDS	392	MHz

Table 4–104 shows the maximum input clock toggle rates for Arria GX device dedicated clock pins.

Table 4–104. Arria GX Maximum Input Clock Rate for Dedicated Clock Pins (Part 1 of 2)

I/O Standards	–6 Speed Grade	Units
3.3-V LVTTL	373	MHz
3.3-V LVCMOS	373	MHz
2.5 V	373	MHz
1.8 V	373	MHz
1.5 V	373	MHz
SSTL-2 CLASS I	467	MHz
SSTL-2 CLASS II	467	MHz
3.3-V PCI	373	MHz

Table 4–104. Arria GX Maximum Input Clock Rate for Dedicated Clock Pins (Part 2 of 2)

I/O Standards	–6 Speed Grade	Units
3.3-V PCI-X	373	MHz
SSTL-18 CLASS I	467	MHz
SSTL-18 CLASS II	467	MHz
1.8-V HSTL CLASS I	467	MHz
1.8-V HSTL CLASS II	467	MHz
1.5-V HSTL CLASS I	467	MHz
1.5-V HSTL CLASS II	467	MHz
1.2-V HSTL	233	MHz
DIFFERENTAL SSTL-2	467	MHz
DIFFERENTIAL 2.5-V SSTL CLASS II	467	MHz
DIFFERENTIAL 1.8-V SSTL CLASS I	467	MHz
DIFFERENTIAL 1.8-V SSTL CLASS II	467	MHz
DIFFERENTIAL 1.8-V HSTL CLASS I	467	MHz
DIFFERENTIAL 1.8-V HSTL CLASS II	467	MHz
DIFFERENTIAL 1.5-V HSTL CLASS I	467	MHz
DIFFERENTIAL 1.5-V HSTL CLASS II	467	MHz
DIFFERENTIAL 1.2-V HSTL	233	MHz
LVDS	640	MHz
LVDS *(1)*	373	MHz

Note to Table 4–104:

(1) This set of numbers refers to the VIO dedicated input clock pins.

Table 4–105 shows the maximum output clock toggle rates for Arria GX device column I/O pins.

Table 4–105. Arria GX Maximum Output Toggle Rate for Column I/O Pins (Part 1 of 3)

I/O Standards	Drive Strength	–6 Speed Grade	Units
3.3-V LVTTL	4 mA	196	MHz
	8 mA	303	MHz
	12 mA	393	MHz
	16 mA	486	MHz
	20 mA	570	MHz
	24 mA	626	MHz

Table 4–112. Maximum DCD for DDIO Output on Row I/O Pins With PLL in the Clock Path

Maximum DCD (ps) for Row DDIO Output I/O Standard	Arria GX Devices (PLL Output Feeding DDIO)	Units
	–6 Speed Grade	
SSTL-18 Class I	65	ps
1.8-V HSTL Class I	70	ps
1.5-V HSTL Class I	70	ps
LVDS	180	ps

Table 4–113. Maximum DCD for DDIO Output on Column I/O Pins With PLL in the Clock Path

Maximum DCD (ps) for Column DDIO Output I/O Standard	Arria GX Devices (PLL Output Feeding DDIO)	Units
	–6 Speed Grade	
3.3-V LVTTL	160	ps
3.3-V LVCMOS	110	ps
2.5V	95	ps
1.8V	100	ps
1.5-V LVCMOS	155	ps
SSTL-2 Class I	75	ps
SSTL-2 Class II	70	ps
SSTL-18 Class I	65	ps
SSTL-18 Class II	80	ps
1.8-V HSTL Class I	70	ps
1.8-V HSTL Class II	70	ps
1.5-V HSTL Class I	70	ps
1.5-V HSTL Class II	100	ps
1.2-V HSTL	155	ps
LVPECL	180	ps

High-Speed I/O Specifications

Table 4–114 lists high-speed timing specifications definitions.

Table 4–114. High-Speed Timing Specifications and Definitions (Part 1 of 2)

High-Speed Timing Specifications	Definitions
t_C	High-speed receiver/transmitter input and output clock period.
f_{HSCLK}	High-speed receiver/transmitter input and output clock frequency.
J	Deserialization factor (width of parallel data bus).
W	PLL multiplication factor.
t_{RISE}	Low-to-high transmission time.
t_{FALL}	High-to-low transmission time.