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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	2508
Number of Logic Elements/Cells	50160
Total RAM Bits	2475072
Number of I/O	350
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep1agx50df780i6n

Table 1–1. Arria GX Device Features (Part 2 of 2)

Feature	EP1AGX20C	EP1AGX35C/D		EP1AGX50C/D		EP1AGX60C/D/E			EP1AGX90E
	C	C	D	C	D	C	D	E	E
Source-synchronous transmit channels	29	29	29	29	29, 42	29	29	42	45
M512 RAM blocks (32 × 18 bits)	166	197		313		326			478
M4K RAM blocks (128 × 36 bits)	118	140		242		252			400
M-RAM blocks (4096 × 144 bits)	1	1		2		2			4
Total RAM bits	1,229,184	1,348,416		2,475,072		2,528,640			4,477,824
Embedded multipliers (18 × 18)	40	56		104		128			176
DSP blocks	10	14		26		32			44
PLLs	4	4		4	4, 8	4		8	8
Maximum user I/O pins	230, 341	230	341	229	350, 514	229	350	514	538

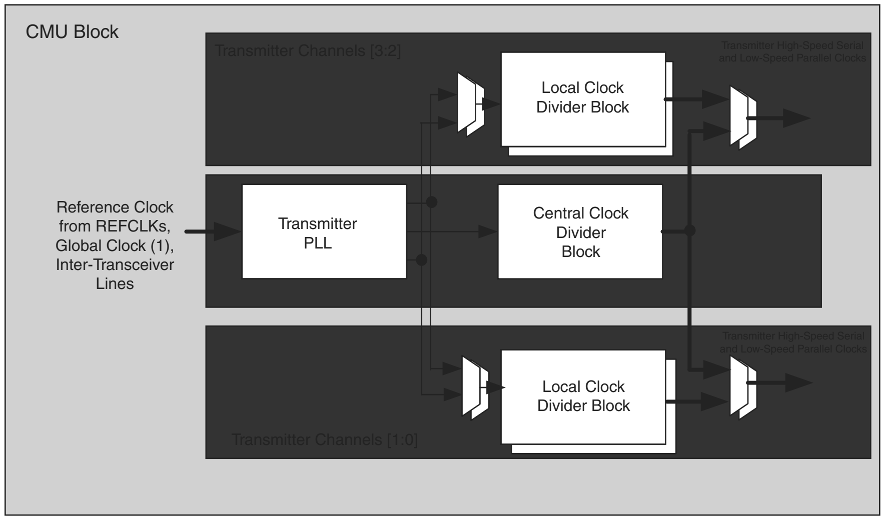
Arria GX devices are available in space-saving FBGA packages (refer to Table 1–2). All Arria GX devices support vertical migration within the same package. With vertical migration support, designers can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities. For I/O pin migration across densities, the designer must cross-reference the available I/O pins with the device pin-outs for all planned densities of a given package type to identify which I/O pins are migratable.

Table 1–2. Arria GX Package Options (Pin Counts and Transceiver Channels) (Part 1 of 2)

Device	Transceiver Channels	Source-Synchronous Channels		Maximum User I/O Pin Count		
		Receive	Transmit	484-Pin FBGA (23 mm)	780-Pin FBGA (29 mm)	1152-Pin FBGA (35 mm)
EP1AGX20C	4	31	29	230	341	—
EP1AGX35C	4	31	29	230	—	—
EP1AGX50C	4	31	29	229	—	—
EP1AGX60C	4	31	29	229	—	—
EP1AGX35D	8	31	29	—	341	—
EP1AGX50D	8	31, 42	29, 42	—	350	514

Figure 2–3 shows the block diagram of the clock multiplier unit.

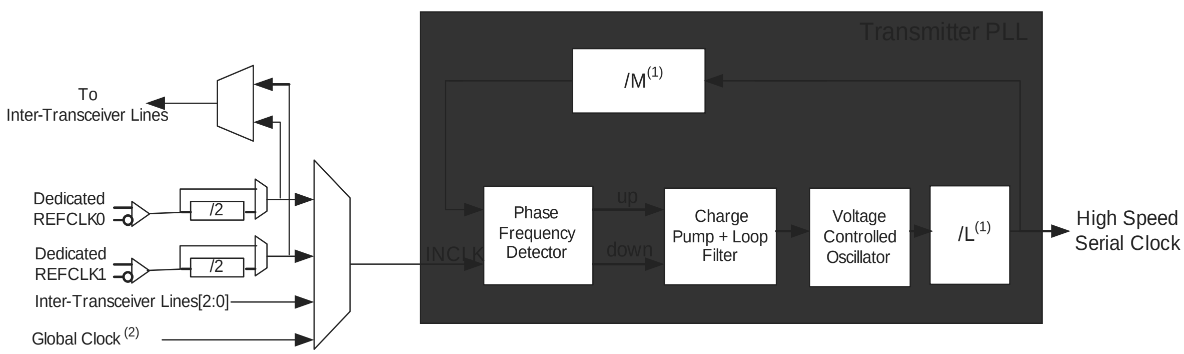
Figure 2–3. Clock Multiplier Unit



The transmitter PLL multiplies the input reference clock to generate the high-speed serial clock required to support the intended protocol. It implements a half-rate voltage controlled oscillator (VCO) that generates a clock at half the frequency of the serial data rate for which it is configured.

Figure 2–4 shows the block diagram of the transmitter PLL.

Figure 2–4. Transmitter PLL



Notes to Figure 2–4:

(1) You only need to select the protocol and the available input reference clock frequency in the ALTGXB MegaWizard Plug-In Manager. Based on your selections, the MegaWizard Plug-In Manager automatically selects the necessary /M and /L dividers (clock multiplication factors).

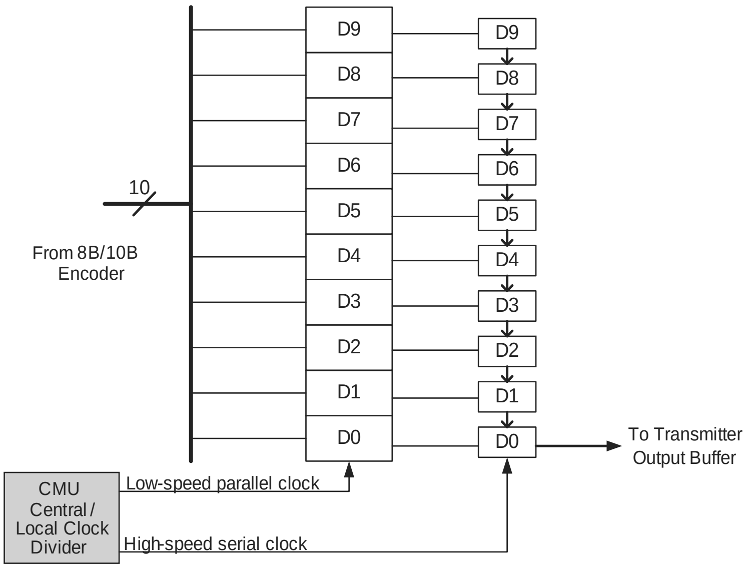
(2) The global clock line must be driven from an input pin only.

The reference clock input to the transmitter PLL can be derived from:

- One of two available dedicated reference clock input pins (`REFCLK0` or `REFCLK1`) of the associated transceiver block
- PLD global clock network (must be driven directly from an input clock pin and cannot be driven by user logic or enhanced PLL)

Figure 2–7 shows the serializer block diagram.

Figure 2–7. Serializer



Transmitter Buffer

The Arria GX transceiver buffers support the 1.2- and 1.5-V PCML I/O standard at rates up to 3.125 Gbps. The common mode voltage (V_{CM}) of the output driver may be set to 600 or 700 mV.

For more information about the Arria GX transceiver buffers, refer to the *Arria GX Transceiver Architecture* chapter.

The output buffer, as shown in Figure 2–8, is directly driven by the high-speed data serializer and consists of a programmable output driver, a programmable pre-emphasis circuit, and OCT circuitry.

XAUI Mode

In XAUI mode, the rate matcher adheres to clause 48 of the IEEE 802.3ae specification for clock rate compensation. The rate matcher performs clock compensation on columns of /R/ (/K28.0/), denoted by //R//. An //R// is added or deleted automatically based on the number of words in the FIFO buffer.

PCI Express (PIPE) Mode Rate Matcher

In PCI Express (PIPE) mode, the rate matcher can compensate up to ± 300 PPM (600 PPM total) frequency difference between the upstream transmitter and the receiver. The rate matcher logic looks for skip ordered sets (SOS), which contains a /K28.5/ comma followed by three /K28.0/ skip characters. The rate matcher logic deletes or inserts /K28.0/ skip characters as necessary from/to the rate matcher FIFO.

The rate matcher in PCI Express (PIPE) mode has a FIFO buffer overflow and underflow protection. In the event of a FIFO buffer overflow, the rate matcher deletes any data after detecting the overflow condition to prevent FIFO pointer corruption until the rate matcher is not full. In an underflow condition, the rate matcher inserts 9'h1FE (/K30.7/) until the FIFO buffer is not empty. These measures ensure that the FIFO buffer can gracefully exit the overflow and underflow condition without requiring a FIFO reset. The rate matcher FIFO overflow and underflow condition is indicated on the `pipestatus` port.

You can bypass the rate matcher in PCI Express (PIPE) mode if you have a synchronous system where the upstream transmitter and local receiver derive their reference clocks from the same source.

GIGE Mode Rate Matcher

In GIGE mode, the rate matcher can compensate up to ± 100 PPM (200 PPM total) frequency difference between the upstream transmitter and the receiver. The rate matcher logic inserts or deletes /I2/ idle ordered sets to/from the rate matcher FIFO during the inter-frame or inter-packet gap (IFG or IPG). /I2/ is selected as the rate matching ordered set because it maintains the running disparity, unlike /I1/ that alters the running disparity. Because the /I2/ ordered-set contains two 10-bit code groups (/K28.5/, /D16.2/), 20 bits are inserted or deleted at a time for rate matching.

☞ The rate matcher logic has the capability to insert or delete /C1/ or /C2/ configuration ordered sets when 'GIGE Enhanced' mode is chosen as the sub-protocol in the MegaWizard Plug-In Manager.

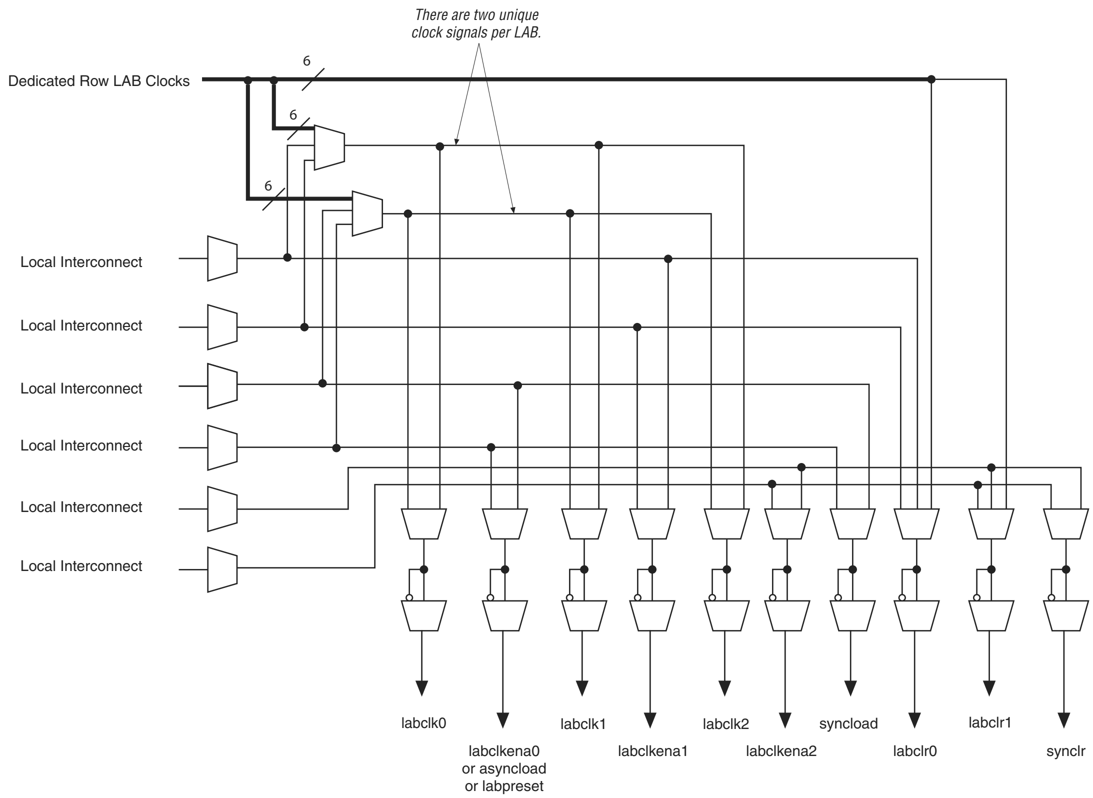
If the frequency PPM difference between the upstream transmitter and the local receiver is high, or if the packet size is too large, the rate matcher FIFO buffer can face an overflow or underflow situation.

Basic Mode

In basic mode, you can program the skip and control pattern for rate matching. There is no restriction on the deletion of a skip character in a cluster. The rate matcher deletes the skip characters as long as they are available. For insertion, the rate matcher inserts skip characters such that the number of skip characters at the output of rate matcher does not exceed five.

Figure 2–27 shows the LAB control signal generation circuit.

Figure 2–27. LAB-Wide Control Signals



Adaptive Logic Modules

The basic building block of logic in the Arria GX architecture is the ALM. The ALM provides advanced features with efficient logic utilization. Each ALM contains a variety of look-up table (LUT)-based resources that can be divided between two adaptive LUTs (ALUTs). With up to eight inputs to the two ALUTs, one ALM can implement various combinations of two functions. This adaptability allows the ALM to be completely backward-compatible with four-input LUT architectures. One ALM can also implement any function of up to six inputs and certain seven-input functions.

In addition to the adaptive LUT-based resources, each ALM contains two programmable registers, two dedicated full adders, a carry chain, a shared arithmetic chain, and a register chain. Through these dedicated resources, the ALM can efficiently implement various arithmetic functions and shift registers. Each ALM drives all types of interconnects: local, row, column, carry chain, shared arithmetic chain, register chain, and direct link interconnects. Figure 2–28 shows a high-level block diagram of the Arria GX ALM while Figure 2–29 shows a detailed view of all the connections in the ALM.

Table 2–11. TriMatrix Memory Features (Part 2 of 2)

Memory Feature	M512 RAM Block (32 × 18 Bits)	M4K RAM Block (128 × 36 Bits)	M-RAM Block (4K × 144 Bits)
ROM	✓	✓	—
FIFO buffer	✓	✓	✓
Pack mode	—	✓	✓
Byte enable	✓	✓	✓
Address clock enable	—	✓	✓
Parity bits	✓	✓	✓
Mixed clock mode	✓	✓	✓
Memory initialization file (**.mif**)	✓	✓	—
Simple dual-port memory mixed width support	✓	✓	✓
True dual-port memory mixed width support	—	✓	✓
Power-up conditions	Outputs cleared	Outputs cleared	Outputs unknown
Register clears	Output registers	Output registers	Output registers
Mixed-port read-during-write	Unknown output/old data	Unknown output/old data	Unknown output
Configurations	512 × 1 256 × 2 128 × 4 64 × 8 64 × 9 32 × 16 32 × 18	4K × 1 2K × 2 1K × 4 512 × 8 512 × 9 256 × 16 256 × 18 128 × 32 128 × 36	64K × 8 64K × 9 32K × 16 32K × 18 16K × 32 16K × 36 8K × 64 8K × 72 4K × 128 4K × 144

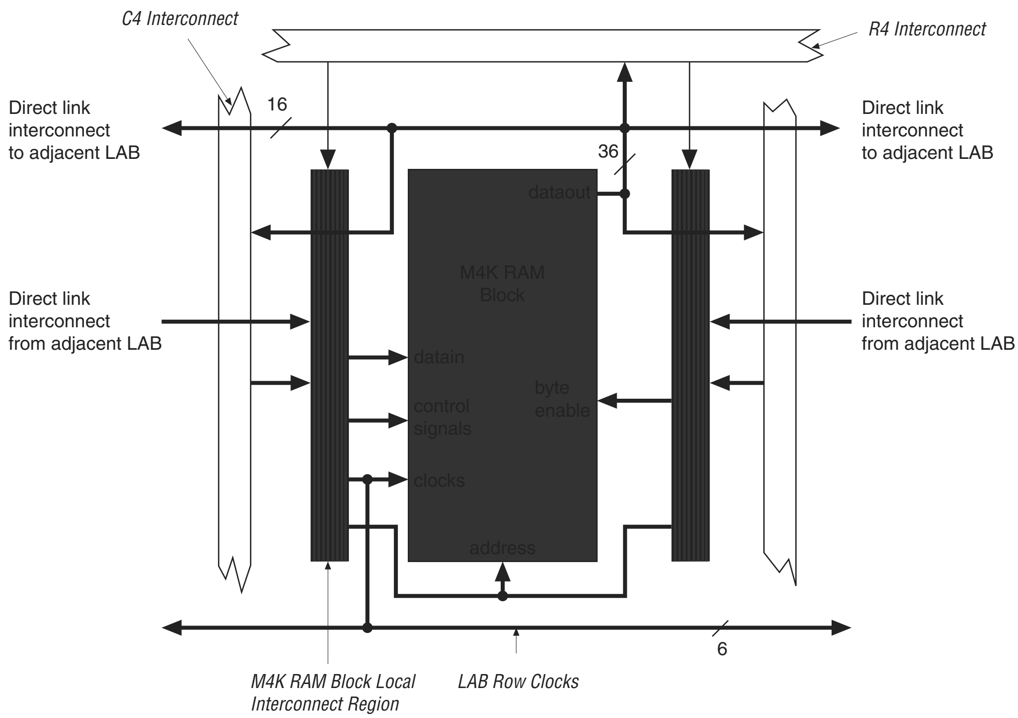
TriMatrix memory provides three different memory sizes for efficient application support. The Quartus II software automatically partitions the user-defined memory into the embedded memory blocks using the most efficient size combinations. You can also manually assign the memory to a specific block size or a mixture of block sizes.

M512 RAM Block

The M512 RAM block is a simple dual-port memory block and is useful for implementing small FIFO buffers, DSP, and clock domain transfer applications. Each block contains 576 RAM bits (including parity bits). M512 RAM blocks can be configured in the following modes:

- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

Figure 2–43. M512 RAM Block LAB Row Interface



M4K RAM Blocks

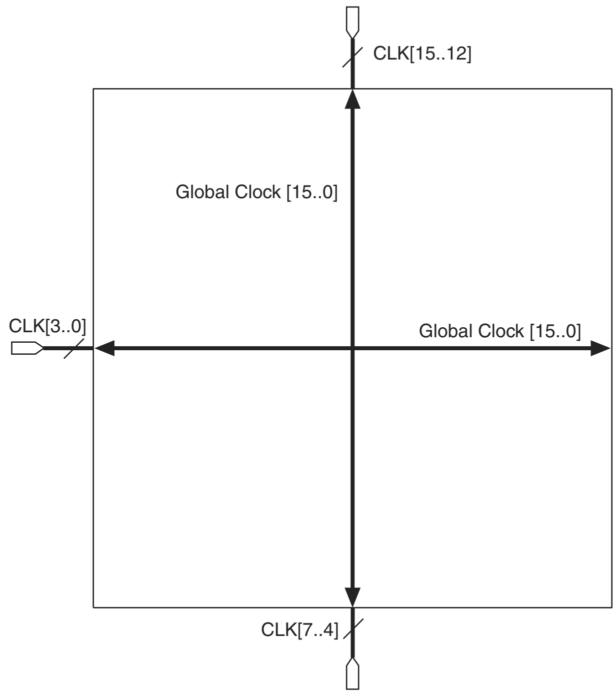
The M4K RAM block includes support for true dual-port RAM. The M4K RAM block is used to implement buffers for a wide variety of applications such as storing processor code, implementing lookup schemes, and implementing larger memory applications. Each block contains 4,608 RAM bits (including parity bits). M4K RAM blocks can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

When configured as RAM or ROM, you can use an initialization file to pre-load the memory contents.

M4K RAM blocks allow for different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M4K RAM block registers (`renwe`, `address`, `byte enable`, `datain`, and `output` registers). Only the `output` register can be bypassed. The six `labclk` signals or local interconnects can drive the control signals for the A and B ports of the M4K RAM block. ALMs can also control the `clock_a`, `clock_b`, `renwe_a, renwe_b`, `clr_a, clr_b`, `clocken_a`, and `clocken_b` signals, as shown in Figure 2–44.

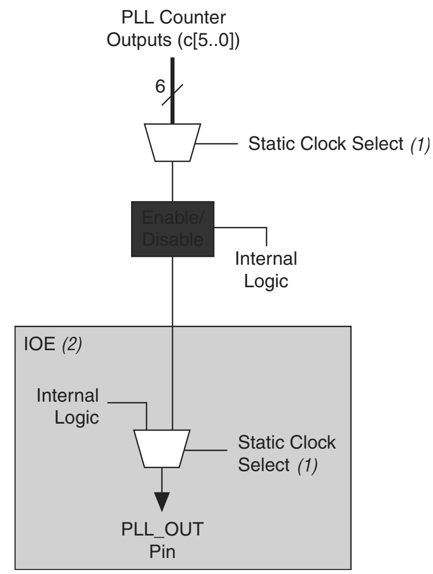
Figure 2–54. Global Clocking



Regional Clock Network

There are eight RCLK networks (`RCLK[7..0]`) in each quadrant of the Arria GX device that are driven by the dedicated `CLK[15..12]` and `CLK[7..0]` input pins, by PLL outputs, or by internal logic. The regional clock networks provide the lowest clock delay and skew for logic contained in a single quadrant. The `CLK` pins symmetrically drive the `RCLK` networks in a particular quadrant, as shown in Figure 2–55.

Figure 2–60. External PLL Output Clock Control Blocks



Notes to Figure 2–60:

(1) These clock select signals can only be set through a configuration file (**.sof** or **.pof**) and cannot be dynamically controlled during user mode operation.

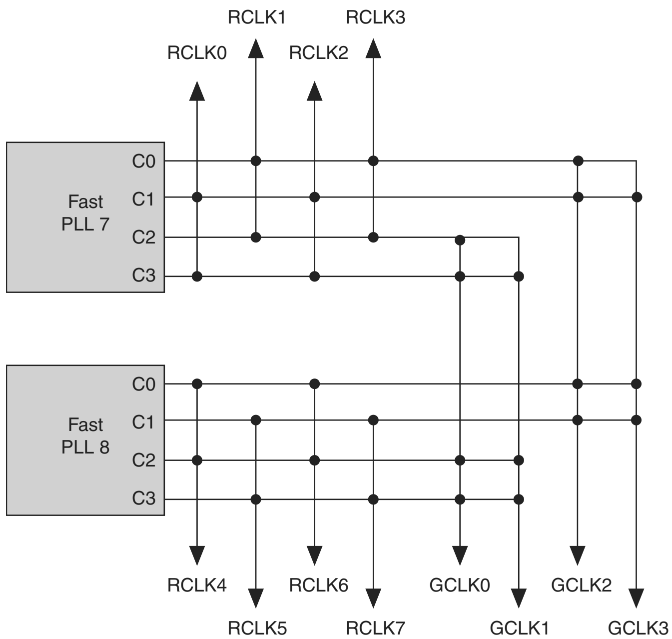
(2) The clock control block feeds to a multiplexer within the `PLL_OUT` pin's IOE. The `PLL_OUT` pin is a dual-purpose pin. Therefore, this multiplexer selects either an internal signal or the output of the clock control block.

For the global clock control block, clock source selection can be controlled either statically or dynamically. You have the option of statically selecting the clock source by using the Quartus II software to set specific configuration bits in the configuration file (**.sof** or **.pof**) or controlling the selection dynamically by using internal logic to drive the multiplexer select inputs. When selecting statically, the clock source can be set to any of the inputs to the select multiplexer. When selecting the clock source dynamically, you can either select between two PLL outputs (such as the `C0` or `C1` outputs from one PLL), between two PLLs (such as the `C0/C1` clock output of one PLL or the `C0/C1` clock output of the other PLL), between two clock pins (such as `CLK0` or `CLK1`), or between a combination of clock pins or PLL outputs.

For the regional and `PLL_OUT` clock control block, clock source selection can only be controlled statically using configuration bits. Any of the inputs to the clock select multiplexer can be set as the clock source.

Arria GX clock networks can be disabled (powered down) by both static and dynamic approaches. When a clock net is powered down, all logic fed by the clock net is in an off-state thereby reducing the overall power consumption of the device. GCLK and RCLK networks can be powered down statically through a setting in the configuration file (**.sof** or **.pof**). Clock networks that are not used are automatically powered down through configuration bit settings in the configuration file generated by the Quartus II software. The dynamic clock enable or disable feature allows the internal logic to control power up/down synchronously on `GCLK` and `RCLK` nets and `PLL_OUT` pins. This function is independent of the PLL and is applied directly on the clock network or `PLL_OUT` pin, as shown in Figure 2–58 through Figure 2–60.

Figure 2–63. Global and Regional Clock Connections from Corner Clock Pins and Fast PLL Outputs *(Note 1)*



Note to Figure 2–63:

(1) The GCLK or RCLK in a fast PLL's quadrant can drive the fast PLL input. A dedicated clock input pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

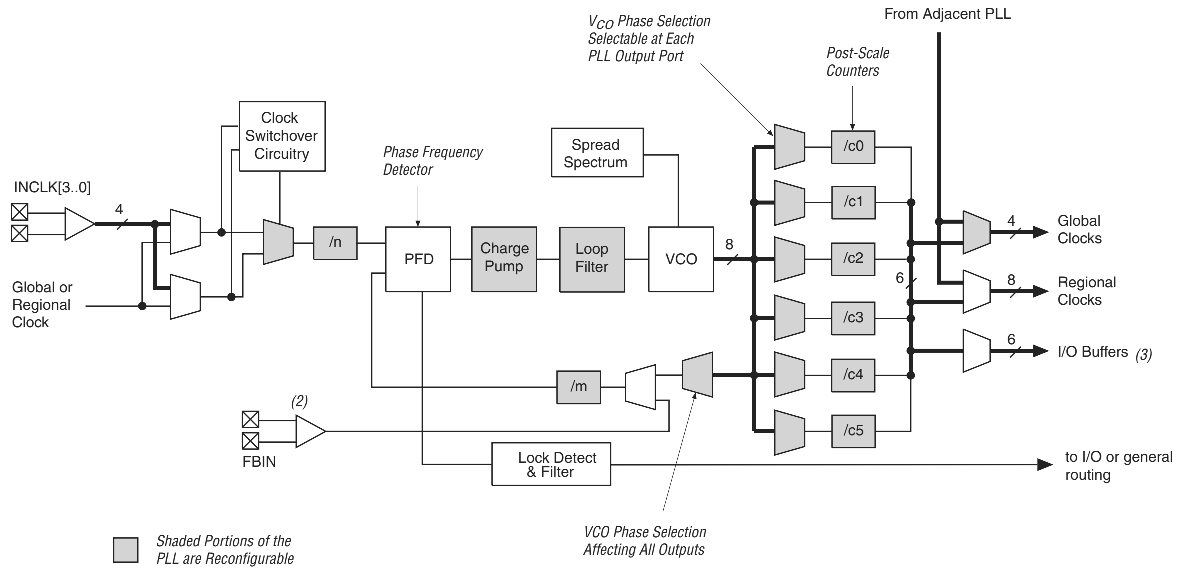
Table 2–19. Global and Regional Clock Connections from Left Side Clock Pins and Fast PLL Outputs (Part 1 of 2)

Left Side Global & Regional Clock Network Connectivity	CLK0	CLK1	CLK2	CLK3	RCLK0	RCLK1	RCLK2	RCLK3	RCLK4	RCLK5	RCLK6	RCLK7
Clock Pins												
CLK0p	✓	✓	—	—	✓	—	—	—	✓	—	—	—
CLK1p	✓	✓	—	—	—	✓	—	—	—	✓	—	—
CLK2p	—	—	✓	✓	—	—	✓	—	—	—	✓	—
CLK3p	—	—	✓	✓	—	—	—	✓	—	—	—	✓
Drivers from Internal Logic												
GCLKDRV0	✓	✓	—	—	—	—	—	—	—	—	—	—
GCLKDRV1	✓	✓	—	—	—	—	—	—	—	—	—	—
GCLKDRV2	—	—	✓	✓	—	—	—	—	—	—	—	—
GCLKDRV3	—	—	✓	✓	—	—	—	—	—	—	—	—
RCLKDRV0	—	—	—	—	✓	—	—	—	✓	—	—	—
RCLKDRV1	—	—	—	—	—	✓	—	—	—	✓	—	—
RCLKDRV2	—	—	—	—	—	—	✓	—	—	—	✓	—
RCLKDRV3	—	—	—	—	—	—	—	✓	—	—	—	✓
RCLKDRV4	—	—	—	—	✓	—	—	—	✓	—	—	—
RCLKDRV5	—	—	—	—	—	✓	—	—	—	✓	—	—
RCLKDRV6	—	—	—	—	—	—	✓	—	—	—	✓	—

Enhanced PLLs

Arria GX devices contain up to four enhanced PLLs with advanced clock management features. These features include support for external clock feedback mode, spread-spectrum clocking, and counter cascading. Figure 2–65 shows a diagram of the enhanced PLL.

Figure 2–65. Arria GX Enhanced PLL *(Note 1)*



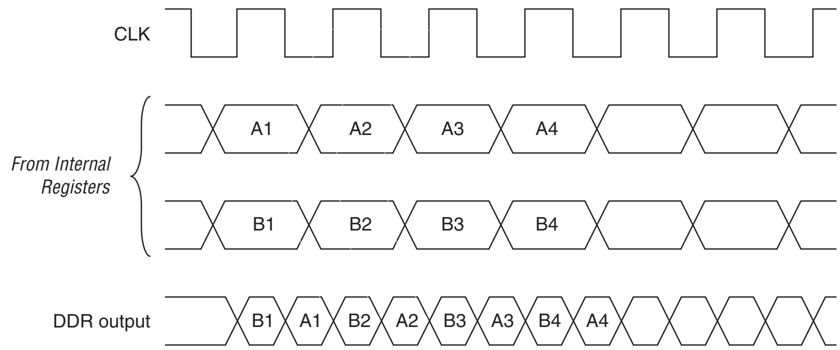
Notes to Figure 2–65:

(1) Each clock source can come from any of the four clock pins that are physically located on the same side of the device as the PLL.
(2) If the feedback input is used, you will lose one (or two, if FBIN is differential) external clock output pin.
(3) Each enhanced PLL has three differential external clock outputs or six single-ended external clock outputs.
(4) The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal cannot drive the PLL.

Fast PLLs

Arria GX devices contain up to four fast PLLs with high-speed serial interfacing ability. Fast PLLs offer high-speed outputs to manage the high-speed differential I/O interfaces. Figure 2–66 shows a diagram of the fast PLL.

Figure 2–76. Output Timing Diagram in DDR Mode



The Arria GX IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations. The negative-edge-clocked OE register holds the `OE` signal inactive until the falling edge of the clock to meet DDR SDRAM timing requirements.

External RAM Interfacing

In addition to the six I/O registers in each IOE, Arria GX devices also have dedicated phase-shift circuitry for interfacing with external memory interfaces, including DDR, DDR2 SDRAM, and SDR SDRAM. In every Arria GX device, the I/O banks at the top (Banks 3 and 4) and bottom (Banks 7 and 8) of the device support DQ and DQS signals with DQ bus modes of ×4, ×8/×9, ×16/×18, or ×32/×36. Table 2–23 shows the number of DQ and DQS buses that are supported per device.

Table 2–23. DQS and DQ Bus Mode Support *(Note 1)*

Device	Package	Number of ×4 Groups	Number of ×8/×9 Groups	Number of ×16/×18 Groups	Number of ×32/×36 Groups
EP1AGX20	484-pin FineLine BGA	2	0	0	0
EP1AGX35	484-pin FineLine BGA	2	0	0	0
	780-pin FineLine BGA	18	8	4	0
EP1AGX50/60	484-pin FineLine BGA	2	0	0	0
	780-pin FineLine BGA	18	8	4	0
	1,152-pin FineLine BGA	36	18	8	4
EP1AGX90	1,152-pin FineLine BGA	36	18	8	4

Note to Table 2–23:

(1) Numbers are preliminary until devices are available.

A compensated delay element on each DQS pin automatically aligns input DQS synchronization signals with the data window of their corresponding DQ data signals. The DQS signals drive a local DQS bus in the top and bottom I/O banks. This DQS bus is an additional resource to the I/O clocks and is used to clock DQ input registers with the DQS signal.

Arria GX devices provide two types of termination:

- On-chip differential termination (R_D OCT)
- On-chip series termination (R_S OCT)

Table 2–26 lists the Arria GX OCT support per I/O bank.

Table 2–26. On-Chip Termination Support by I/O Banks

On-Chip Termination Support	I/O Standard Support	Top and Bottom Banks (3, 4, 7, 8)	Left Bank (1, 2)
Series termination	3.3-V LVTTL	✓	✓
	3.3-V LVCMOS	✓	✓
	2.5-V LVTTL	✓	✓
	2.5-V LVCMOS	✓	✓
	1.8-V LVTTL	✓	✓
	1.8-V LVCMOS	✓	✓
	1.5-V LVTTL	✓	✓
	1.5-V LVCMOS	✓	✓
	SSTL-2 class I and II	✓	✓
	SSTL-18 class I	✓	✓
	SSTL-18 class II	✓	—
	1.8-V HSTL class I	✓	✓
	1.8-V HSTL class II	✓	—
	1.5-V HSTL class I	✓	✓
	1.2-V HSTL	✓	—
Differential termination *(1)*	LVDS	—	✓
	HyperTransport technology	—	✓

Note to Table 2–26:

(1) Clock pins `CLK1` and `CLK3`, and pins `FPLL[7..8]CLK` do not support differential on-chip termination. Clock pins `CLK0` and `CLK2`, do support differential on-chip termination. Clock pins in the top and bottom banks (`CLK[4..7, 12..15]`) do not support differential on-chip termination.

On-Chip Differential Termination (R_D OCT)

Arria GX devices support internal differential termination with a nominal resistance value of 100 Ω for LVDS input receiver buffers. LVPECL input signals (supported on clock pins only) require an external termination resistor. R_D OCT is supported across the full range of supported differential data rates as shown in the *High-Speed I/O Specifications* section of the *DC & Switching Characteristics* chapter.

For more information about R_D OCT, refer to the *High-Speed Differential I/O Interfaces with DPA in Arria GX Devices* chapter.

For more information about tolerance specifications for R_D OCT, refer to the *DC & Switching Characteristics* chapter.

Table 4–6. Arria GX Transceiver Block AC Specification (Part 3 of 3)

Symbol / Description	Conditions	–6 Speed Grade Commercial and Industrial			Units
		Min	Typ	Max	
Transmitter PLL					
VCO frequency range	—	500	—	1562.5	MHz
Bandwidth at 3.125 Gbps	BW = Low	—	3	—	MHz
	BW = Med	—	5	—	
	BW = High	—	9	—	
Bandwidth at 2.5 Gbps	BW = Low	—	1	—	MHz
	BW = Med	—	2	—	
	BW = High	—	4	—	
TX PLL lock time from `gxb_powerdown` de-assertion *(9)*, *(14)*	—	—	—	100	us
PCS					
Interface speed per mode	—	25	—	156.25	MHz
Digital Reset Pulse Width	—	Minimum is 2 parallel clock cycles			—

Notes to Table 4–6:

(1) Spread spectrum clocking is allowed only in PCI Express (PIPE) mode if the upstream transmitter and the receiver share the same clock source.
(2) The reference clock DC coupling option is only available in PCI Express (PIPE) mode for the HCSL I/O standard.
(3) The `fixedclk` is used in PIPE mode receiver detect circuitry.
(4) The device cannot tolerate prolonged operation at this absolute maximum.
(5) The rate matcher supports only up to ± 300 PPM for PIPE mode and ± 100 PPM for GIGE mode.
(6) This parameter is measured by embedding the run length data in a PRBS sequence.
(7) Signal detect threshold detector circuitry is available only in PCI Express (PIPE mode).
(8) Time taken for `rx_pll_locked` to go high from `rx_analogreset` deassertion. Refer to Figure 4–1.
(9) For lock times specific to the protocols, refer to protocol characterization documents.
(10) Time for which the CDR needs to stay in LTR mode after `rx_pll_locked` is asserted and before `rx_locktodata` is asserted in manual mode. Refer to Figure 4–1.
(11) Time taken to recover valid data from GXB after the `rx_locktodata` signal is asserted in manual mode. Measurement results are based on PRBS31, for native data rates only. Refer to Figure 4–1.
(12) Time taken to recover valid data from GXB after the `rx_freqlocked` signal goes high in automatic mode. Measurement results are based on PRBS31, for native data rates only. Refer to Figure 4–2.
(13) This is applicable only to PCI Express (PIPE) ×4 and XAUI ×4 mode.
(14) Time taken to lock `TX PLL` from `gxb_powerdown` deassertion.
(15) The 1.2 V RX VICM settings is intended for DC-coupled LVDS links.

Figure 4–1 shows the lock time parameters in manual mode. Figure 4–2 shows the lock time parameters in automatic mode.

☞ LTD = Lock to data
LTR = Lock to reference clock

Figure 4–3 and Figure 4–4 show differential receiver input and transmitter output waveforms, respectively.

Figure 4–3. Receiver Input Waveform

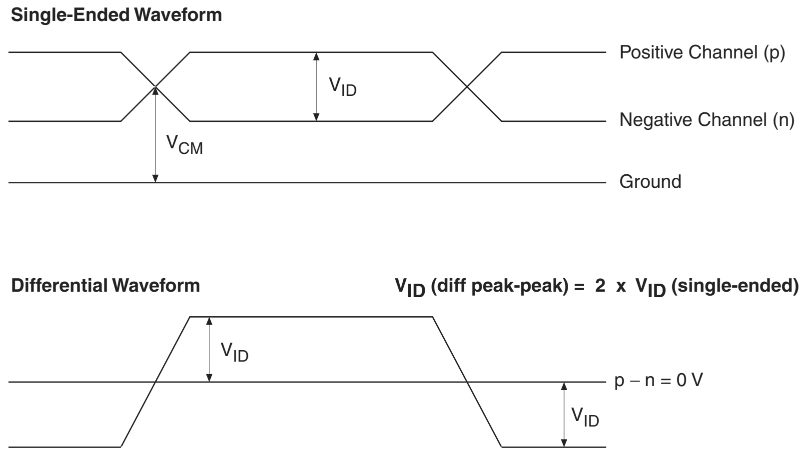


Figure 4–4. Transmitter Output Waveform

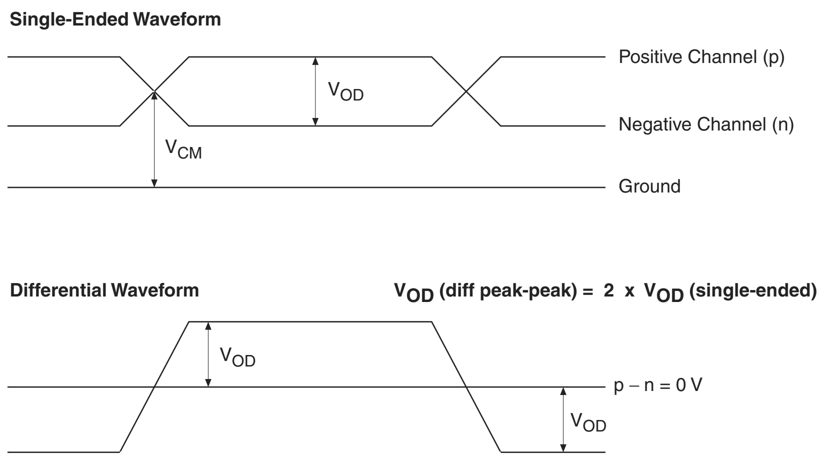


Table 4–7 lists the Arria GX transceiver block AC specification.

Table 4–7. Arria GX Transceiver Block AC Specification *(Note 1)*, *(2)*, *(3)* (Part 1 of 4)

Description	Condition	–6 Speed Grade Commercial & Industrial	Units
XAUI Transmit Jitter Generation *(4)*			
Total jitter at 3.125 Gbps	`REFCLK` = 156.25 MHz Pattern = CJPAT V_{OD} = 1200 mV No Pre-emphasis	0.3	UI

Table 4–50. EP1AGX20 Row Pins output Timing Parameters (Part 2 of 2)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.626	2.626	5.614	ns
		GCLK PLL	t_{CO}	1.207	1.207	2.542	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.602	2.602	5.538	ns
		GCLK PLL	t_{CO}	1.183	1.183	2.466	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.568	2.568	5.407	ns
		GCLK PLL	t_{CO}	1.149	1.149	2.335	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.614	2.614	5.556	ns
		GCLK PLL	t_{CO}	1.195	1.195	2.484	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.618	2.618	5.485	ns
		GCLK PLL	t_{CO}	1.199	1.199	2.413	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.594	2.594	5.468	ns
		GCLK PLL	t_{CO}	1.175	1.175	2.396	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.597	2.597	5.447	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.375	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.595	2.595	5.466	ns
		GCLK PLL	t_{CO}	1.176	1.176	2.394	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.598	2.598	5.430	ns
		GCLK PLL	t_{CO}	1.179	1.179	2.358	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.580	2.580	5.426	ns
		GCLK PLL	t_{CO}	1.161	1.161	2.354	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.584	2.584	5.415	ns
		GCLK PLL	t_{CO}	1.165	1.165	2.343	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.575	2.575	5.414	ns
		GCLK PLL	t_{CO}	1.156	1.156	2.342	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.594	2.594	5.443	ns
		GCLK PLL	t_{CO}	1.175	1.175	2.371	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.597	2.597	5.429	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.357	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.582	2.582	5.421	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.349	ns
LVDS	—	GCLK	t_{CO}	2.654	2.654	5.613	ns
		GCLK PLL	t_{CO}	1.226	1.226	2.530	ns

Table 4–55. EP1AGX35 Column Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.131	1.131	2.607	ns
		t_H	–1.026	–1.026	–2.330	ns
	GCLK PLL	t_{SU}	2.573	2.573	5.713	ns
		t_H	–2.468	–2.468	–5.436	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.132	1.132	2.607	ns
		t_H	–1.027	–1.027	–2.330	ns
	GCLK PLL	t_{SU}	2.574	2.574	5.715	ns
		t_H	–2.469	–2.469	–5.438	ns
3.3-V PCI	GCLK	t_{SU}	1.256	1.256	2.903	ns
		t_H	–1.151	–1.151	–2.626	ns
	GCLK PLL	t_{SU}	2.698	2.698	6.009	ns
		t_H	–2.593	–2.593	–5.732	ns
3.3-V PCI-X	GCLK	t_{SU}	1.256	1.256	2.903	ns
		t_H	–1.151	–1.151	–2.626	ns
	GCLK PLL	t_{SU}	2.698	2.698	6.009	ns
		t_H	–2.593	–2.593	–5.732	ns
LVDS	GCLK	t_{SU}	1.106	1.106	2.489	ns
		t_H	–1.001	–1.001	–2.212	ns
	GCLK PLL	t_{SU}	2.530	2.530	5.564	ns
		t_H	–2.425	–2.425	–5.287	ns

Table 4–56 lists I/O timing specifications.

Table 4–56. EP1AGX35 Row Pins Output Timing Parameters (Part 1 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	2.904	2.904	6.699	ns
		GCLK PLL	t_{CO}	1.485	1.485	3.627	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.776	2.776	6.059	ns
		GCLK PLL	t_{CO}	1.357	1.357	2.987	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.720	2.720	6.022	ns
		GCLK PLL	t_{CO}	1.301	1.301	2.950	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.776	2.776	6.059	ns
		GCLK PLL	t_{CO}	1.357	1.357	2.987	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.670	2.670	5.753	ns
		GCLK PLL	t_{CO}	1.251	1.251	2.681	ns
2.5 V	4 mA	GCLK	t_{CO}	2.759	2.759	6.033	ns
		GCLK PLL	t_{CO}	1.340	1.340	2.961	ns

Table 4–72 lists I/O timing specifications.

Table 4–72. EP1AGX90 Row Pins Input Timing Parameters (Part 1 of 2)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.295	1.295	2.873	ns
		t_H	–1.190	–1.190	–2.596	ns
	GCLK PLL	t_{SU}	3.366	3.366	7.017	ns
		t_H	–3.261	–3.261	–6.740	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.295	1.295	2.873	ns
		t_H	–1.190	–1.190	–2.596	ns
	GCLK PLL	t_{SU}	3.366	3.366	7.017	ns
		t_H	–3.261	–3.261	–6.740	ns
2.5 V	GCLK	t_{SU}	1.307	1.307	2.854	ns
		t_H	–1.202	–1.202	–2.577	ns
	GCLK PLL	t_{SU}	3.378	3.378	6.998	ns
		t_H	–3.273	–3.273	–6.721	ns
1.8 V	GCLK	t_{SU}	1.381	1.381	3.073	ns
		t_H	–1.276	–1.276	–2.796	ns
	GCLK PLL	t_{SU}	3.434	3.434	7.191	ns
		t_H	–3.329	–3.329	–6.914	ns
1.5 V	GCLK	t_{SU}	1.384	1.384	3.168	ns
		t_H	–1.279	–1.279	–2.891	ns
	GCLK PLL	t_{SU}	3.437	3.437	7.286	ns
		t_H	–3.332	–3.332	–7.009	ns
SSTL-2 CLASS I	GCLK	t_{SU}	1.121	1.121	2.329	ns
		t_H	–1.016	–1.016	–2.052	ns
	GCLK PLL	t_{SU}	3.187	3.187	6.466	ns
		t_H	–3.082	–3.082	–6.189	ns
SSTL-2 CLASS II	GCLK	t_{SU}	1.121	1.121	2.329	ns
		t_H	–1.016	–1.016	–2.052	ns
	GCLK PLL	t_{SU}	3.187	3.187	6.466	ns
		t_H	–3.082	–3.082	–6.189	ns
SSTL-18 CLASS I	GCLK	t_{SU}	1.159	1.159	2.447	ns
		t_H	–1.054	–1.054	–2.170	ns
	GCLK PLL	t_{SU}	3.212	3.212	6.565	ns
		t_H	–3.107	–3.107	–6.288	ns
SSTL-18 CLASS II	GCLK	t_{SU}	1.157	1.157	2.441	ns
		t_H	–1.052	–1.052	–2.164	ns
	GCLK PLL	t_{SU}	3.235	3.235	6.597	ns
		t_H	–3.130	–3.130	–6.320	ns

Table 4–102. Arria GX Maximum Input Toggle Rate for Column I/O Pins

I/O Standards	–6 Speed Grade	Units
SSTL-18 CLASS II	467	MHz
1.8-V HSTL CLASS I	467	MHz
1.8-V HSTL CLASS II	467	MHz
1.5-V HSTL CLASS I	467	MHz
1.5-V HSTL CLASS II	467	MHz
3.3-V PCI	420	MHz
3.3-V PCI-X	420	MHz

Table 4–103 shows the maximum input clock toggle rates for Arria GX device row I/O pins.

Table 4–103. Arria GX Maximum Input Toggle Rate for Row I/O Pins

I/O Standards	–6 Speed Grade	Units
3.3-V LVTTL	420	MHz
3.3-V LVCMOS	420	MHz
2.5 V	420	MHz
1.8 V	420	MHz
1.5 V	420	MHz
SSTL-2 CLASS I	467	MHz
SSTL-2 CLASS II	467	MHz
SSTL-18 CLASS I	467	MHz
SSTL-18 CLASS II	467	MHz
1.8-V HSTL CLASS I	467	MHz
1.8-V HSTL CLASS II	467	MHz
1.5-V HSTL CLASS I	467	MHz
1.5-V HSTL CLASS II	467	MHz
LVDS	392	MHz

Table 4–104 shows the maximum input clock toggle rates for Arria GX device dedicated clock pins.

Table 4–104. Arria GX Maximum Input Clock Rate for Dedicated Clock Pins (Part 1 of 2)

I/O Standards	–6 Speed Grade	Units
3.3-V LVTTL	373	MHz
3.3-V LVCMOS	373	MHz
2.5 V	373	MHz
1.8 V	373	MHz
1.5 V	373	MHz
SSTL-2 CLASS I	467	MHz
SSTL-2 CLASS II	467	MHz
3.3-V PCI	373	MHz

Table 4–105. Arria GX Maximum Output Toggle Rate for Column I/O Pins (Part 2 of 3)

I/O Standards	Drive Strength	–6 Speed Grade	Units
3.3-V LVCMOS	4 mA	215	MHz
	8 mA	411	MHz
	12 mA	626	MHz
	16 mA	819	MHz
	20 mA	874	MHz
	24 mA	934	MHz
2.5 V	4 mA	168	MHz
	8 mA	355	MHz
	12 mA	514	MHz
	16 mA	766	MHz
1.8 V	2 mA	97	MHz
	4 mA	215	MHz
	6 mA	336	MHz
	8 mA	486	MHz
	10 mA	706	MHz
	12 mA	925	MHz
1.5 V	2 mA	168	MHz
	4 mA	303	MHz
	6 mA	350	MHz
	8 mA	392	MHz
SSTL-2 CLASS I	8 mA	280	MHz
	12 mA	327	MHz
SSTL-2 CLASS II	16 mA	280	MHz
	20 mA	327	MHz
	24 mA	327	MHz
SSTL-18 CLASS I	4 mA	140	MHz
	6 mA	186	MHz
	8 mA	280	MHz
	10 mA	373	MHz
	12 mA	373	MHz
SSTL-18 CLASS II	8 mA	140	MHz
	16 mA	327	MHz
	18 mA	373	MHz
	20 mA	420	MHz
1.8-V HSTL CLASS I	4 mA	280	MHz
	6 mA	420	MHz
	8 mA	561	MHz
	10 mA	561	MHz
	12 mA	607	MHz

