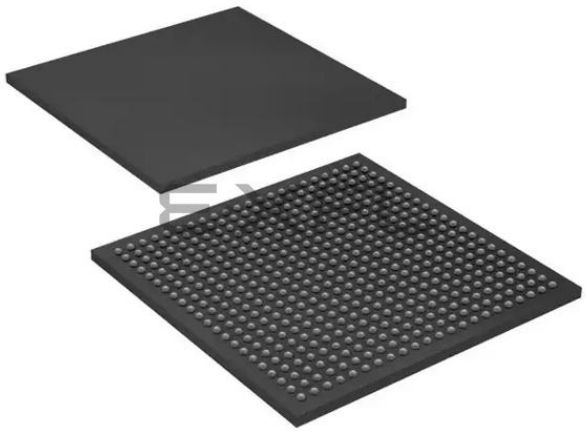

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3005
Number of Logic Elements/Cells	60100
Total RAM Bits	2528640
Number of I/O	229
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1agx60cf484c6n

1. Arria GX Device Family Overview

AGX51001-2.0

Introduction

The Arria® GX family of devices combines 3.125 Gbps serial transceivers with reliable packaging technology and a proven logic array. Arria GX devices include 4 to 12 high-speed transceiver channels, each incorporating clock data recovery (CDR) technology and embedded SERDES circuitry designed to support PCI-Express, Gigabit Ethernet, SDI, SerialLite II, XAUI, and Serial RapidIO protocols, along with the ability to develop proprietary, serial-based IP using its Basic mode. The transceivers build upon the success of the Stratix® II GX family. The Arria GX FPGA technology offers a 1.2-V logic array with the right level of performance and dependability needed to support these mainstream protocols.

Features

The key features of Arria GX devices include:

- Transceiver block features
  - High-speed serial transceiver channels with CDR support up to 3.125 Gbps.
  - Devices available with 4, 8, or 12 high-speed full-duplex serial transceiver channels
  - Support for the following CDR-based bus standards—PCI Express, Gigabit Ethernet, SDI, SerialLite II, XAUI, and Serial RapidIO, along with the ability to develop proprietary, serial-based IP using its Basic mode
  - Individual transmitter and receiver channel power-down capability for reduced power consumption during non-operation
  - 1.2- and 1.5-V pseudo current mode logic (PCML) support on transmitter output buffers
  - Receiver indicator for loss of signal (available only in PCI Express [PIPE] mode)
  - Hot socketing feature for hot plug-in or hot swap and power sequencing support without the use of external devices
  - Dedicated circuitry that is compliant with PIPE, XAUI, Gigabit Ethernet, Serial Digital Interface (SDI), and Serial RapidIO
  - 8B/10B encoder/decoder performs 8-bit to 10-bit encoding and 10-bit to 8-bit decoding
  - Phase compensation FIFO buffer performs clock domain translation between the transceiver block and the logic array
  - Channel aligner compliant with XAUI

In GIGE and Serial RapidIO modes, you can dynamically put each transceiver channel individually in serial loopback by controlling the `rx_seriallpbken` port. A high on the `rx_seriallpbken` port puts the transceiver into serial loopback and a low takes the transceiver out of serial loopback.

As seen in Figure 2–18, the serial data output from the transmitter serializer is looped back to the receiver CRU in serial loopback. The transmitter data path from the PLD interface to the serializer in serial loopback is the same as in non-loopback mode. The receiver data path from the clock recovery unit to the PLD interface in serial loopback is the same as in non-loopback mode. Because the entire transceiver data path is available in serial loopback, this option is often used to diagnose the data path as a probable cause of link errors.

☞ When serial loopback is enabled, the transmitter output buffer is still active and drives the serial data out on the `tx_dataout` port.

Reverse Serial Loopback

Reverse serial loopback mode uses the analog portion of the transceiver. An external source (pattern generator or transceiver) generates the source data. The high-speed serial source data arrives at the high-speed differential receiver input buffer, passes through the CRU unit and the retimed serial data is looped back, and is transmitted though the high-speed differential transmitter output buffer.

Figure 2–19 shows the data path in reverse serial loopback mode.

Figure 2–19. Arria GX Block in Reverse Serial Loopback Mode

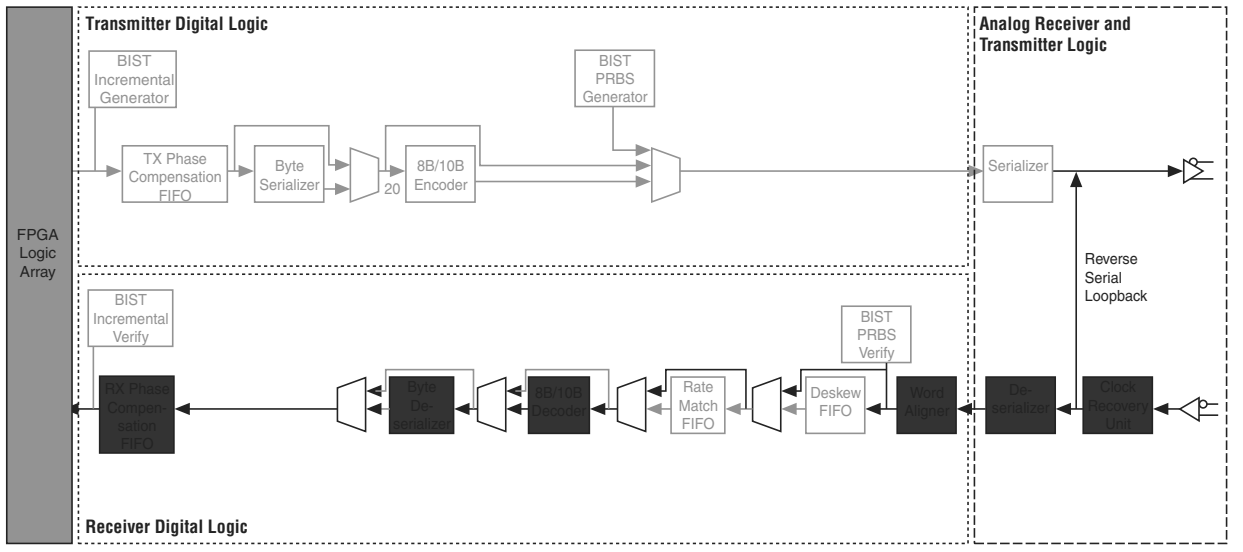
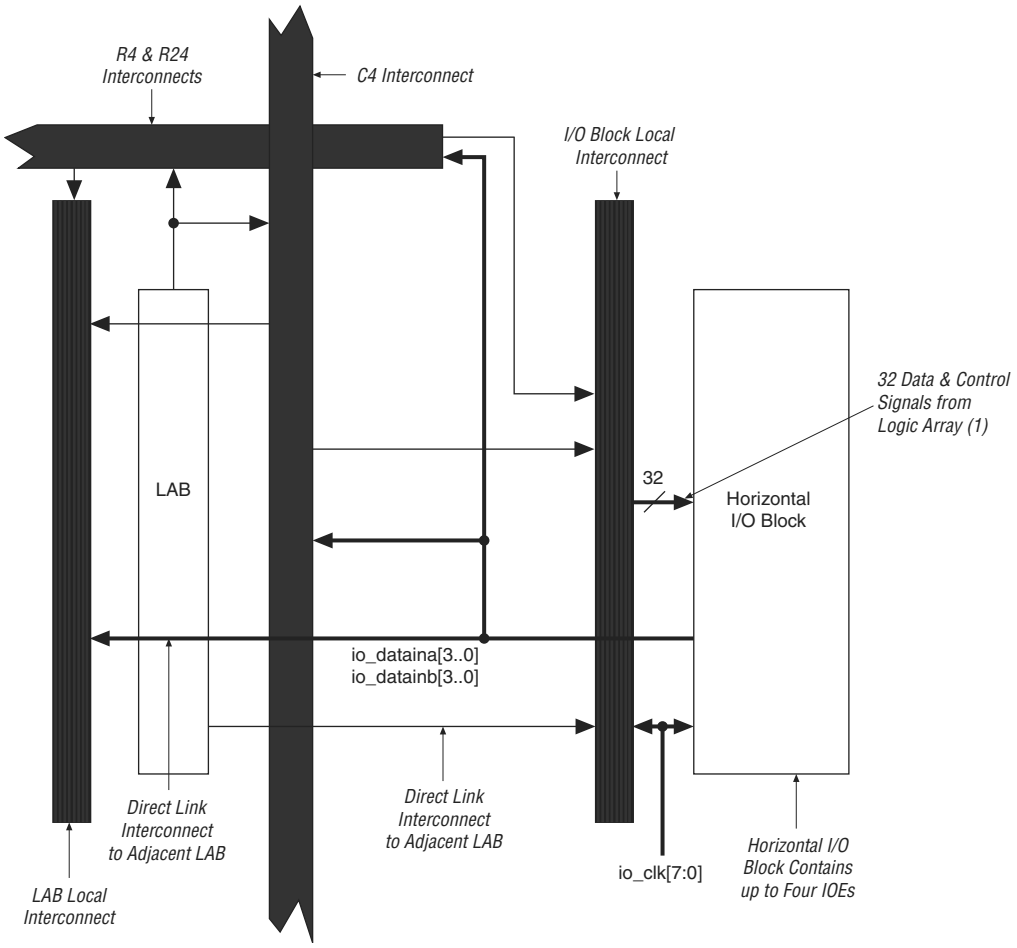


Figure 2–68 shows how a row I/O block connects to the logic array.

Figure 2–68. Row I/O Block Connection to the Interconnect



Note to Figure 2–68:

(1) The 32 data and control signals consist of eight data out lines: four lines each for DDR applications `io_dataouta[3..0]` and `io_dataoutb[3..0]`, four output enables `io_oe[3..0]`, four input clock enables `io_ce_in[3..0]`, four output clock enables `io_ce_out[3..0]`, four clocks `io_clk[3..0]`, four asynchronous clear and preset signals `io_aclr/apreset[3..0]`, and four synchronous clear and preset signals `io_sclr/spreset[3..0]`.

A path in which a pin directly drives a register can require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinational logic may not require the delay. Programmable delays exist for decreasing input-pin-to-logic-array and IOE input register delays. The Quartus II Compiler can program these delays to automatically minimize setup time while providing a zero hold time. Programmable delays can increase the register-to-pin delays for output and/or output enable registers. Programmable delays are no longer required to ensure zero hold times for logic array register-to-IOE register transfers. The Quartus II Compiler can create zero hold time for these transfers. Table 2–22 shows the programmable delays for Arria GX devices.

Table 2–22. Arria GX Devices Programmable Delay Chain

Programmable Delays	Quartus II Logic Option
Input pin to logic array delay	Input delay from pin to internal cells
Input pin to input register delay	Input delay from pin to input register
Output pin delay	Delay from output register to output pin
Output enable register t_{CO} delay	Delay to output enable pin

IOE registers in Arria GX devices share the same source for clear or preset. You can program preset or clear for each individual IOE. You can also program the registers to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power-up. If one register in an IOE uses a preset or clear signal, all registers in the IOE must use that same signal if they require preset or clear. Additionally, a synchronous reset signal is available for the IOE registers.

Double Data Rate I/O Pins

Arria GX devices have six registers in the IOE, which support DDR interfacing by clocking data on both positive and negative clock edges. The IOEs in Arria GX devices support DDR inputs, DDR outputs, and bidirectional DDR modes. When using the IOE for DDR inputs, the two input registers clock double rate input data on alternating edges. An input latch is also used in the IOE for DDR input acquisition. The latch holds the data that is present during the clock high times, allowing both bits of data to be synchronous with the same clock edge (either rising or falling). Figure 2–73 shows an IOE configured for DDR input. Figure 2–74 shows the DDR input timing diagram.

On-Chip Series Termination (R_S OCT)

Arria GX devices support driver impedance matching to provide the I/O driver with controlled output impedance that closely matches the impedance of the transmission line. As a result, reflections can be significantly reduced. Arria GX devices support R_S OCT for single-ended I/O standards with typical R_S values of 25 and 50 Ω. Once matching impedance is selected, current drive strength is no longer selectable. Table 2–26 shows the list of output standards that support R_S OCT.

For more information about R_S OCT supported by Arria GX devices, refer to the *Selectable I/O Standards in Arria GX Devices* chapter.

For more information about tolerance specifications for OCT without calibration, refer to the *DC & Switching Characteristics* chapter.

MultiVolt I/O Interface

The Arria GX architecture supports the MultiVolt I/O interface feature that allows Arria GX devices in all packages to interface with systems of different supply voltages. Arria GX VCCINT pins must always be connected to a 1.2-V power supply. With a 1.2-V V_{CCINT} level, input pins are 1.2-, 1.5-, 1.8-, 2.5-, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.2-, 1.5-, 1.8-, 2.5-, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (for example, when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). Arria GX VCCPD power pins must be connected to a 3.3-V power supply. These power pins are used to supply the pre-driver power to the output buffers, which increases the performance of the output pins. The VCCPD pins also power configuration input pins and JTAG input pins.

Table 2–27 lists Arria GX MultiVolt I/O support.

Table 2–27. Arria GX MultiVolt I/O Support *(Note 1)*

V_{CCIO} (V)	Input Signal (V)					Output Signal (V)					
	1.2	1.5	1.8	2.5	3.3	1.2	1.5	1.8	2.5	3.3	5.0
1.2	*(4)*	✓ *(2)*	✓ *(2)*	✓ *(2)*	✓ *(2)*	✓ *(4)*	—	—	—	—	—
1.5	*(4)*	✓	✓	✓ *(2)*	✓ *(2)*	✓ *(3)*	✓	—	—	—	—
1.8	*(4)*	✓	✓	✓ *(2)*	✓ *(2)*	✓ *(3)*	✓ *(3)*	✓	—	—	—
2.5	*(4)*	—	—	✓	✓	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓	—	—
3.3	*(4)*	—	—	✓	✓	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓	✓

Notes to Table 2–27:

(1) To drive inputs higher than V_{CCIO} but less than 4.0 V, disable the PCI clamping diode and select the **Allow LVTTL and LVCMOS input levels to overdrive input buffer** option in the Quartus II software.

(2) The pin current may be slightly higher than the default value. You must verify that the driving device's V_{OL} maximum and V_{OH} minimum voltages do not violate the applicable Arria GX V_{IL} maximum and V_{IH} minimum voltage specifications.

(3) Although V_{CCIO} specifies the voltage necessary for the Arria GX device to drive out, a receiving device powered at a different level can still interface with the Arria GX device if it has inputs that tolerate the V_{CCIO} value.

(4) Arria GX devices support 1.2-V HSTL. They do not support 1.2-V LVTTL and 1.2-V LVCMOS.

The TDO and nCEO pins are powered by V_{CCIO} of the bank that they reside. TDO is in I/O bank 4 and nCEO is in I/O Bank 7. Ideally, the V_{CC} supplies for the I/O buffers of any two connected pins are at the same voltage level. This may not always be possible depending on the V_{CCIO} level of TDO and nCEO pins on master devices and the configuration voltage level chosen by V_{CCSEL} on slave devices. Master and slave devices can be in any position in the chain. The master device indicates that it is driving out TDO or nCEO to a slave device. For multi-device passive configuration schemes, the nCEO pin of the master device drives the nCE pin of the slave device. The VCCSEL pin on the slave device selects which input buffer is used for nCE. When V_{CCSEL} is logic high, it selects the 1.8-V/1.5-V buffer powered by V_{CCIO}. When V_{CCSEL} is logic low, it selects the 3.3-V/2.5-V input buffer powered by V_{CCPD}. The ideal case is to have the V_{CCIO} of the nCEO bank in a master device match the V_{CCSEL} settings for the nCE input buffer of the slave device it is connected to, but that may not be possible depending on the application.

Table 2–28 contains board design recommendations to ensure that nCEO can successfully drive nCE for all power supply combinations.

Table 2–28. Board Design Recommendations for nCEO and nCE Input Buffer Power

nCE Input Buffer Power in I/O Bank 3	Arria GX nCEO V_{CCIO} Voltage Level in I/O Bank 7				
	V_{CCIO} = 3.3 V	V_{CCIO} = 2.5 V	V_{CCIO} = 1.8 V	V_{CCIO} = 1.5 V	V_{CCIO} = 1.2 V
VCCSEL high (V_{CCIO} Bank 3 = 1.5 V)	✓ *(1), (2)*	✓ *(3), (4)*	✓ *(5)*	✓	✓
VCCSEL high (V_{CCIO} Bank 3 = 1.8 V)	✓ *(1), (2)*	✓ *(3), (4)*	✓	✓	Level shifter required
VCCSEL low (nCE powered by V_{CCPD} = 3.3 V)	✓	✓ *(4)*	✓ *(6)*	Level shifter required	Level shifter required

Notes to Table 2–28:

(1) Input buffer is 3.3-V tolerant.
(2) The nCEO output buffer meets V_{OH} (MIN) = 2.4 V.
(3) Input buffer is 2.5-V tolerant.
(4) The nCEO output buffer meets V_{OH} (MIN) = 2.0 V.
(5) Input buffer is 1.8-V tolerant.
(6) An external 250-Ω pull-up resistor is not required, but recommended if signal levels on the board are not optimal.

For JTAG chains, the TDO pin of the first device drives the TDI pin of the second device in the chain. The V_{CCSEL} input on JTAG input I/O cells (TCK, TMS, TDI, and TRST) is internally hardwired to GND selecting the 3.3-V/2.5-V input buffer powered by V_{CCPD}. The ideal case is to have the V_{CCIO} of the TDO bank from the first device to match the V_{CCSEL} settings for TDI on the second device, but that may not be possible depending on the application. Table 2–29 contains board design recommendations to ensure proper JTAG chain operation.

Configuring Arria GX FPGAs with JRunner

The JRunner software driver configures Altera FPGAs, including Arria GX FPGAs, through the ByteBlaster™ II or ByteBlasterMV cables in JTAG mode. The programming input file supported is in Raw Binary File (**.rbf**) format. JRunner also requires a Chain Description File (**.cdf**) generated by the Quartus II software. JRunner is targeted for embedded JTAG configuration. The source code is developed for the Windows NT operating system (OS), but can be customized to run on other platforms.

For more information about the JRunner software driver, refer to the *AN414: JRunner Software Driver: An Embedded Solution for PLD JTAG Configuration* and the source files on the Altera website.

Programming Serial Configuration Devices with SRunner

You can program a serial configuration device in-system by an external microprocessor using SRunner™. SRunner is a software driver developed for embedded serial configuration device programming that can be easily customized to fit into different embedded systems. SRunner software driver reads a raw programming data file (**.rpd**) and writes to serial configuration devices. The serial configuration device programming time using SRunner software driver is comparable to the programming time when using the Quartus II software.

For more information about SRunner, refer to the *AN418: SRunner: An Embedded Solution for Serial Configuration Device Programming* and the source code on the Altera website.

For more information about programming serial configuration devices, refer to the *Serial Configuration Devices (EPCS1, EPCS4, EPCS64, and EPCS128) Data Sheet* in the *Configuration Handbook*.

Configuring Arria GX FPGAs with the MicroBlaster Driver

The MicroBlaster™ software driver supports a raw binary file (RBF) programming input file and is ideal for embedded FPP or PS configuration. The source code is developed for the Windows NT operating system, although it can be customized to run on other operating systems.

For more information about the MicroBlaster software driver, refer to the *Configuring the MicroBlaster Fast Passive Parallel Software Driver White Paper* or the *AN423: Configuring the MicroBlaster Passive Serial Software Driver*.

PLL Reconfiguration

The phase-locked loops (PLLs) in the Arria GX device family support reconfiguration of their multiply, divide, VCO-phase selection, and bandwidth selection settings without reconfiguring the entire device. You can use either serial data from the logic array or regular I/O pins to program the PLL's counter settings in a serial chain. This option provides considerable flexibility for frequency synthesis, allowing real-time variation of the PLL frequency and delay. The rest of the device is functional while reconfiguring the PLL.

Table 4–17. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO} *(1)*	Output supply voltage	—	2.375	2.625	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.3	0.7	V
V_{OH}	High-level output voltage	I_{OH} = –1 mA *(2)*	2.0	—	V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA *(2)*	—	0.4	V

Notes to Table 4–17:

(1) The Arria GX device V_{CCIO} voltage level support of 2.5 to 5% is narrower than defined in the normal range of the EIA/JEDEC standard.

(2) This specification is supported across all the programmable drive settings available for this I/O standard.

Table 4–18. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO} *(1)*	Output supply voltage	—	1.71	1.89	V
V_{IH}	High-level input voltage	—	0.65 × V_{CCIO}	2.25	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(2)*	V_{CCIO} – 0.45	—	V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(2)*	—	0.45	V

Notes to Table 4–18:

(1) The Arria GX device V_{CCIO} voltage level support of 1.8 to 5% is narrower than defined in the normal range of the EIA/JEDEC standard.

(2) This specification is supported across all the programmable drive settings available for this I/O standard, as shown in *Arria GX Architecture* chapter.

Table 4–19. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO} *(1)*	Output supply voltage	—	1.425	1.575	V
V_{IH}	High-level input voltage	—	0.65 V_{CCIO}	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(2)*	0.75 V_{CCIO}	—	V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(2)*	—	0.25 V_{CCIO}	V

Notes to Table 4–19:

(1) The Arria GX device V_{CCIO} voltage level support of 1.5 to 5% is narrower than defined in the normal range of the EIA/JEDEC standard.

(2) This specification is supported across all the programmable drive settings available for this I/O standard, as shown in the *Arria GX Architecture* chapter.

Figure 4–5 and Figure 4–6 show receiver input and transmitter output waveforms, respectively, for all differential I/O standards (LVDS and LVPECL).

Table 4–33. 1.5-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	1.425	1.5	1.575	V
V_{REF}	Input reference voltage	—	0.713	0.75	0.788	V
V_{TT}	Termination voltage	—	0.713	0.75	0.788	V
V_{IH} (DC)	DC high-level input voltage	—	V_{REF} + 0.1	—	—	V
V_{IL} (DC)	DC low-level input voltage	—	–0.3	—	V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage	—	V_{REF} + 0.2	—	—	V
V_{IL} (AC)	AC low-level input voltage	—	—	—	V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(1)*	V_{CCIO} – 0.4	—	—	V
V_{OL}	Low-level output voltage	I_{OH} = –8 mA *(1)*	—	—	0.4	V

Note to Table 4–33:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Arria GX Architecture* chapter.

Table 4–34. 1.5-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	1.425	1.50	1.575	V
V_{REF}	Input reference voltage	—	0.713	0.75	0.788	V
V_{TT}	Termination voltage	—	0.713	0.75	0.788	V
V_{IH} (DC)	DC high-level input voltage	—	V_{REF} + 0.1	—	—	V
V_{IL} (DC)	DC low-level input voltage	—	–0.3	—	V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage	—	V_{REF} + 0.2	—	—	V
V_{IL} (AC)	AC low-level input voltage	—	—	—	V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(1)*	V_{CCIO} – 0.4	—	—	V
V_{OL}	Low-level output voltage	I_{OH} = –16 mA *(1)*	—	—	0.4	V

Note to Table 4–34:

(1) This specification is supported across all the programmable drive settings available for this I/O standard, as shown in the *Arria GX Architecture* chapter.

Table 4–35. 1.5-V HSTL Class I & II Differential Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage	1.425	1.5	1.575	V
V_{DIF} (DC)	DC input differential voltage	0.2	—	—	V
V_{CM} (DC)	DC common mode input voltage	0.68	—	0.9	V
V_{DIF} (AC)	AC differential input voltage	0.4	—	—	V
V_{OX} (AC)	AC differential cross point voltage	0.68	—	0.9	V

Table 4–49. EP1AGX20 Column Pins Input Timing Parameters (Part 2 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
SSTL-2 CLASS II	GCLK	t_{SU}	1.075	1.075	2.372	ns
		t_H	–0.970	–0.970	–2.095	ns
	GCLK PLL	t_{SU}	2.517	2.517	5.480	ns
		t_H	–2.412	–2.412	–5.203	ns
SSTL-18 CLASS I	GCLK	t_{SU}	1.113	1.113	2.479	ns
		t_H	–1.008	–1.008	–2.202	ns
	GCLK PLL	t_{SU}	2.555	2.555	5.585	ns
		t_H	–2.450	–2.450	–5.308	ns
SSTL-18 CLASS II	GCLK	t_{SU}	1.114	1.114	2.479	ns
		t_H	–1.009	–1.009	–2.202	ns
	GCLK PLL	t_{SU}	2.556	2.556	5.587	ns
		t_H	–2.451	–2.451	–5.310	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	1.113	1.113	2.479	ns
		t_H	–1.008	–1.008	–2.202	ns
	GCLK PLL	t_{SU}	2.555	2.555	5.585	ns
		t_H	–2.450	–2.450	–5.308	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	1.114	1.114	2.479	ns
		t_H	–1.009	–1.009	–2.202	ns
	GCLK PLL	t_{SU}	2.556	2.556	5.587	ns
		t_H	–2.451	–2.451	–5.310	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.131	1.131	2.607	ns
		t_H	–1.026	–1.026	–2.330	ns
	GCLK PLL	t_{SU}	2.573	2.573	5.713	ns
		t_H	–2.468	–2.468	–5.436	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.132	1.132	2.607	ns
		t_H	–1.027	–1.027	–2.330	ns
	GCLK PLL	t_{SU}	2.574	2.574	5.715	ns
		t_H	–2.469	–2.469	–5.438	ns
3.3-V PCI	GCLK	t_{SU}	1.256	1.256	2.903	ns
		t_H	–1.151	–1.151	–2.626	ns
	GCLK PLL	t_{SU}	2.698	2.698	6.009	ns
		t_H	–2.593	–2.593	–5.732	ns
3.3-V PCI-X	GCLK	t_{SU}	1.256	1.256	2.903	ns
		t_H	–1.151	–1.151	–2.626	ns
	GCLK PLL	t_{SU}	2.698	2.698	6.009	ns
		t_H	–2.593	–2.593	–5.732	ns

Table 4–50. EP1AGX20 Row Pins output Timing Parameters (Part 2 of 2)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.626	2.626	5.614	ns
		GCLK PLL	t_{CO}	1.207	1.207	2.542	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.602	2.602	5.538	ns
		GCLK PLL	t_{CO}	1.183	1.183	2.466	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.568	2.568	5.407	ns
		GCLK PLL	t_{CO}	1.149	1.149	2.335	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.614	2.614	5.556	ns
		GCLK PLL	t_{CO}	1.195	1.195	2.484	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.618	2.618	5.485	ns
		GCLK PLL	t_{CO}	1.199	1.199	2.413	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.594	2.594	5.468	ns
		GCLK PLL	t_{CO}	1.175	1.175	2.396	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.597	2.597	5.447	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.375	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.595	2.595	5.466	ns
		GCLK PLL	t_{CO}	1.176	1.176	2.394	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.598	2.598	5.430	ns
		GCLK PLL	t_{CO}	1.179	1.179	2.358	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.580	2.580	5.426	ns
		GCLK PLL	t_{CO}	1.161	1.161	2.354	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.584	2.584	5.415	ns
		GCLK PLL	t_{CO}	1.165	1.165	2.343	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.575	2.575	5.414	ns
		GCLK PLL	t_{CO}	1.156	1.156	2.342	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.594	2.594	5.443	ns
		GCLK PLL	t_{CO}	1.175	1.175	2.371	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.597	2.597	5.429	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.357	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.582	2.582	5.421	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.349	ns
LVDS	—	GCLK	t_{CO}	2.654	2.654	5.613	ns
		GCLK PLL	t_{CO}	1.226	1.226	2.530	ns

Table 4–51. EP1AGX20 Column Pins Output Timing Parameters (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
1.8 V	6 mA	GCLK	t_{CO}	2.695	2.695	6.155	ns
		GCLK PLL	t_{CO}	1.253	1.253	3.049	ns
1.8 V	8 mA	GCLK	t_{CO}	2.697	2.697	6.064	ns
		GCLK PLL	t_{CO}	1.255	1.255	2.958	ns
1.8 V	10 mA	GCLK	t_{CO}	2.651	2.651	5.987	ns
		GCLK PLL	t_{CO}	1.209	1.209	2.881	ns
1.8 V	12 mA	GCLK	t_{CO}	2.652	2.652	5.930	ns
		GCLK PLL	t_{CO}	1.210	1.210	2.824	ns
1.5 V	2 mA	GCLK	t_{CO}	2.746	2.746	6.723	ns
		GCLK PLL	t_{CO}	1.304	1.304	3.617	ns
1.5 V	4 mA	GCLK	t_{CO}	2.682	2.682	6.154	ns
		GCLK PLL	t_{CO}	1.240	1.240	3.048	ns
1.5 V	6 mA	GCLK	t_{CO}	2.685	2.685	6.036	ns
		GCLK PLL	t_{CO}	1.243	1.243	2.930	ns
1.5 V	8 mA	GCLK	t_{CO}	2.644	2.644	5.983	ns
		GCLK PLL	t_{CO}	1.202	1.202	2.877	ns
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.629	2.629	5.762	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.650	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.612	2.612	5.712	ns
		GCLK PLL	t_{CO}	1.167	1.167	2.600	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.590	2.590	5.639	ns
		GCLK PLL	t_{CO}	1.145	1.145	2.527	ns
SSTL-2 CLASS II	20 mA	GCLK	t_{CO}	2.591	2.591	5.626	ns
		GCLK PLL	t_{CO}	1.146	1.146	2.514	ns
SSTL-2 CLASS II	24 mA	GCLK	t_{CO}	2.587	2.587	5.624	ns
		GCLK PLL	t_{CO}	1.142	1.142	2.512	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.626	2.626	5.733	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.627	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.630	2.630	5.694	ns
		GCLK PLL	t_{CO}	1.185	1.185	2.582	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.609	2.609	5.675	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.563	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.614	2.614	5.673	ns
		GCLK PLL	t_{CO}	1.169	1.169	2.561	ns
SSTL-18 CLASS I	12 mA	GCLK	t_{CO}	2.608	2.608	5.659	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.547	ns
SSTL-18 CLASS II	8 mA	GCLK	t_{CO}	2.597	2.597	5.625	ns
		GCLK PLL	t_{CO}	1.152	1.152	2.513	ns

Table 4–63. EP1AGX50 Column Pins Output Timing Parameters (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.695	2.695	5.893	ns
		GCLK PLL	t_{CO}	1.239	1.239	2.780	ns
3.3-V LVCMOS	12 mA	GCLK	t_{CO}	2.663	2.663	5.809	ns
		GCLK PLL	t_{CO}	1.211	1.211	2.702	ns
3.3-V LVCMOS	16 mA	GCLK	t_{CO}	2.666	2.666	5.776	ns
		GCLK PLL	t_{CO}	1.218	1.218	2.670	ns
3.3-V LVCMOS	20 mA	GCLK	t_{CO}	2.651	2.651	5.758	ns
		GCLK PLL	t_{CO}	1.205	1.205	2.652	ns
3.3-V LVCMOS	24 mA	GCLK	t_{CO}	2.638	2.638	5.736	ns
		GCLK PLL	t_{CO}	1.194	1.194	2.630	ns
2.5 V	4 mA	GCLK	t_{CO}	2.754	2.754	6.240	ns
		GCLK PLL	t_{CO}	1.293	1.293	3.107	ns
2.5 V	8 mA	GCLK	t_{CO}	2.697	2.697	5.963	ns
		GCLK PLL	t_{CO}	1.241	1.241	2.845	ns
2.5 V	12 mA	GCLK	t_{CO}	2.672	2.672	5.837	ns
		GCLK PLL	t_{CO}	1.220	1.220	2.728	ns
2.5 V	16 mA	GCLK	t_{CO}	2.654	2.654	5.760	ns
		GCLK PLL	t_{CO}	1.202	1.202	2.654	ns
1.8 V	2 mA	GCLK	t_{CO}	2.804	2.804	7.295	ns
		GCLK PLL	t_{CO}	1.333	1.333	4.099	ns
1.8 V	4 mA	GCLK	t_{CO}	2.808	2.808	6.479	ns
		GCLK PLL	t_{CO}	1.338	1.338	3.325	ns
1.8 V	6 mA	GCLK	t_{CO}	2.717	2.717	6.195	ns
		GCLK PLL	t_{CO}	1.262	1.262	3.061	ns
1.8 V	8 mA	GCLK	t_{CO}	2.719	2.719	6.098	ns
		GCLK PLL	t_{CO}	1.264	1.264	2.970	ns
1.8 V	10 mA	GCLK	t_{CO}	2.671	2.671	6.012	ns
		GCLK PLL	t_{CO}	1.218	1.218	2.893	ns
1.8 V	12 mA	GCLK	t_{CO}	2.671	2.671	5.953	ns
		GCLK PLL	t_{CO}	1.219	1.219	2.836	ns
1.5 V	2 mA	GCLK	t_{CO}	2.779	2.779	6.815	ns
		GCLK PLL	t_{CO}	1.313	1.313	3.629	ns
1.5 V	4 mA	GCLK	t_{CO}	2.703	2.703	6.210	ns
		GCLK PLL	t_{CO}	1.249	1.249	3.060	ns
1.5 V	6 mA	GCLK	t_{CO}	2.705	2.705	6.118	ns
		GCLK PLL	t_{CO}	1.252	1.252	2.942	ns
1.5 V	8 mA	GCLK	t_{CO}	2.660	2.660	6.014	ns
		GCLK PLL	t_{CO}	1.211	1.211	2.889	ns

Table 4–75. EP1AGX90 Column Pins Output Timing Parameters (Part 4 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
1.5-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.845	2.845	6.264	ns
		GCLK PLL	t_{CO}	0.783	0.783	2.133	ns
1.5-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.839	2.839	6.262	ns
		GCLK PLL	t_{CO}	0.777	0.777	2.131	ns
1.5-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.826	2.826	6.074	ns
		GCLK PLL	t_{CO}	0.764	0.764	1.943	ns
1.5-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.829	2.829	6.084	ns
		GCLK PLL	t_{CO}	0.767	0.767	1.953	ns
1.5-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.831	2.831	6.097	ns
		GCLK PLL	t_{CO}	0.769	0.769	1.966	ns
3.3-V PCI	—	GCLK	t_{CO}	2.987	2.987	6.414	ns
		GCLK PLL	t_{CO}	0.923	0.923	2.279	ns
3.3-V PCI-X	—	GCLK	t_{CO}	2.987	2.987	6.414	ns
		GCLK PLL	t_{CO}	0.923	0.923	2.279	ns
LVDS	—	GCLK	t_{CO}	3.835	3.835	7.541	ns
		GCLK PLL	t_{CO}	1.769	1.769	3.404	ns

Table 4–76 through Table 4–77 list the EP1AGX90 regional clock (RCLK) adder values that should be added to the GCLK values. These adder values are used to determine I/O timing when the I/O pin is driven using the regional clock. This applies for all I/O standards supported by Arria GX with general purpose I/O pins.

Table 4–76 lists row pin delay adders when using the regional clock in Arria GX devices.

Table 4–76. EP1AGX90 Row Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.175	0.175	0.418	ns
RCLK PLL input adder	0.007	0.007	0.015	ns
RCLK output adder	–0.175	–0.175	–0.418	ns
RCLK PLL output adder	–0.007	–0.007	–0.015	ns

Table 4–80 lists clock timing specifications.

Table 4–80. EP1AGX20 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.655	1.655	3.726	ns
t_{COUT}	1.655	1.655	3.726	ns
t_{PLLCIN}	0.236	0.236	0.655	ns
$t_{PLLCOUT}$	0.236	0.236	0.655	ns

Table 4–81 through Table 4–82 list the RCLK clock timing parameters for EP1AGX20 devices.

Table 4–81 lists clock timing specifications.

Table 4–81. EP1AGX20 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.283	1.283	2.901	ns
t_{COUT}	1.288	1.288	2.895	ns
t_{PLLCIN}	–0.034	–0.034	0.077	ns
$t_{PLLCOUT}$	–0.029	–0.029	0.071	ns

Table 4–82 lists clock timing specifications.

Table 4–82. EP1AGX20 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.569	1.569	3.487	ns
t_{COUT}	1.569	1.569	3.487	ns
t_{PLLCIN}	0.278	0.278	0.706	ns
$t_{PLLCOUT}$	0.278	0.278	0.706	ns

EP1AGX35 Clock Timing Parameters

Table 4–83 through Table 4–84 list the GCLK clock timing parameters for EP1AGX35 devices.

Table 4–83 lists clock timing specifications.

Table 4–83. EP1AGX35 Row Pins Global Clock Timing Parameters (Part 1 of 2)

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.394	1.394	3.161	ns
t_{COUT}	1.399	1.399	3.155	ns

EP1AGX50 Clock Timing Parameters

Table 4–87 through Table 4–88 list the GCLK clock timing parameters for EP1AGX50 devices.

Table 4–87 lists clock timing specifications.

Table 4–87. EP1AGX50 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.529	1.529	3.587	ns
t_{COUT}	1.534	1.534	3.581	ns
t_{PLLCIN}	–0.024	–0.024	0.181	ns
$t_{PLLCOUT}$	–0.019	–0.019	0.175	ns

Table 4–88 lists clock timing specifications.

Table 4–88. EP1AGX50 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.793	1.793	4.165	ns
t_{COUT}	1.793	1.793	4.165	ns
t_{PLLCIN}	0.238	0.238	0.758	ns
$t_{PLLCOUT}$	0.238	0.238	0.758	ns

Table 4–89 through Table 4–90 list the RCLK clock timing parameters for EP1AGX50 devices.

Table 4–89 lists clock timing specifications.

Table 4–89. EP1AGX50 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.396	1.396	3.287	ns
t_{COUT}	1.401	1.401	3.281	ns
t_{PLLCIN}	–0.017	–0.017	0.195	ns
$t_{PLLCOUT}$	–0.012	–0.012	0.189	ns

Table 4–104. Arria GX Maximum Input Clock Rate for Dedicated Clock Pins (Part 2 of 2)

I/O Standards	–6 Speed Grade	Units
3.3-V PCI-X	373	MHz
SSTL-18 CLASS I	467	MHz
SSTL-18 CLASS II	467	MHz
1.8-V HSTL CLASS I	467	MHz
1.8-V HSTL CLASS II	467	MHz
1.5-V HSTL CLASS I	467	MHz
1.5-V HSTL CLASS II	467	MHz
1.2-V HSTL	233	MHz
DIFFERENTAL SSTL-2	467	MHz
DIFFERENTIAL 2.5-V SSTL CLASS II	467	MHz
DIFFERENTIAL 1.8-V SSTL CLASS I	467	MHz
DIFFERENTIAL 1.8-V SSTL CLASS II	467	MHz
DIFFERENTIAL 1.8-V HSTL CLASS I	467	MHz
DIFFERENTIAL 1.8-V HSTL CLASS II	467	MHz
DIFFERENTIAL 1.5-V HSTL CLASS I	467	MHz
DIFFERENTIAL 1.5-V HSTL CLASS II	467	MHz
DIFFERENTIAL 1.2-V HSTL	233	MHz
LVDS	640	MHz
LVDS *(1)*	373	MHz

Note to Table 4–104:

(1) This set of numbers refers to the VIO dedicated input clock pins.

Table 4–105 shows the maximum output clock toggle rates for Arria GX device column I/O pins.

Table 4–105. Arria GX Maximum Output Toggle Rate for Column I/O Pins (Part 1 of 3)

I/O Standards	Drive Strength	–6 Speed Grade	Units
3.3-V LVTTL	4 mA	196	MHz
	8 mA	303	MHz
	12 mA	393	MHz
	16 mA	486	MHz
	20 mA	570	MHz
	24 mA	626	MHz

Table 4–105. Arria GX Maximum Output Toggle Rate for Column I/O Pins (Part 2 of 3)

I/O Standards	Drive Strength	–6 Speed Grade	Units
3.3-V LVCMOS	4 mA	215	MHz
	8 mA	411	MHz
	12 mA	626	MHz
	16 mA	819	MHz
	20 mA	874	MHz
	24 mA	934	MHz
2.5 V	4 mA	168	MHz
	8 mA	355	MHz
	12 mA	514	MHz
	16 mA	766	MHz
1.8 V	2 mA	97	MHz
	4 mA	215	MHz
	6 mA	336	MHz
	8 mA	486	MHz
	10 mA	706	MHz
	12 mA	925	MHz
1.5 V	2 mA	168	MHz
	4 mA	303	MHz
	6 mA	350	MHz
	8 mA	392	MHz
SSTL-2 CLASS I	8 mA	280	MHz
	12 mA	327	MHz
SSTL-2 CLASS II	16 mA	280	MHz
	20 mA	327	MHz
	24 mA	327	MHz
SSTL-18 CLASS I	4 mA	140	MHz
	6 mA	186	MHz
	8 mA	280	MHz
	10 mA	373	MHz
	12 mA	373	MHz
SSTL-18 CLASS II	8 mA	140	MHz
	16 mA	327	MHz
	18 mA	373	MHz
	20 mA	420	MHz
1.8-V HSTL CLASS I	4 mA	280	MHz
	6 mA	420	MHz
	8 mA	561	MHz
	10 mA	561	MHz
	12 mA	607	MHz

To calculate the DCD as a percentage:

(T/2 – DCD) / T = (3,745 ps/2 – 125 ps) / 3,745 ps = 46.66% (for low boundary)

(T/2 + DCD) / T = (3,745 ps/2 + 125 ps) / 3,745 ps = 53.33% (for high boundary)

Therefore, the DCD percentage for the output clock at 267 MHz is from 46.66% to 53.33%.

Table 4–109. Maximum DCD for Non-DDIO Output on Column I/O Pins

Column I/O Output Standard I/O Standard	Maximum DCD (ps) for Non-DDIO Output	Units
	–6 Speed Grade	
3.3-V LVTTL	220	ps
3.3-V LVCMOS	175	ps
2.5 V	155	ps
1.8 V	110	ps
1.5-V LVCMOS	215	ps
SSTL-2 Class I	135	ps
SSTL-2 Class II	130	ps
SSTL-18 Class I	115	ps
SSTL-18 Class II	100	ps
1.8-V HSTL Class I	110	ps
1.8-V HSTL Class II	110	ps
1.5-V HSTL Class I	115	ps
1.5-V HSTL Class II	80	ps
1.2-V HSTL-12	200	ps
LVPECL	80	ps

Table 4–110. Maximum DCD for DDIO Output on Row I/O Pins Without PLL in the Clock Path *Note (1)*

Maximum DCD (ps) for Row DDIO Output I/O Standard	Input I/O Standard (No PLL in the Clock Path)					Units
	TTL/CMOS		SSTL-2	SSTL/HSTL	LVDS	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	3.3V	
3.3-V LVTTL	440	495	170	160	105	ps
3.3-V LVCMOS	390	450	120	110	75	ps
2.5 V	375	430	105	95	90	ps
1.8 V	325	385	90	100	135	ps
1.5-V LVCMOS	430	490	160	155	100	ps
SSTL-2 Class I	355	410	85	75	85	ps
SSTL-2 Class II	350	405	80	70	90	ps
SSTL-18 Class I	335	390	65	65	105	ps
1.8-V HSTL Class I	330	385	60	70	110	ps
1.5-V HSTL Class I	330	390	60	70	105	ps

Document Revision History

Table 4–124 lists the revision history for this chapter.

Table 4–124. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
December 2009, v2.0	■ Updated Table 4–104, Table 4–105, and Table 4–106. ■ Document template update. ■ Minor text edits.	—
April 2009 v1.4	■ Updated Table 4–6 and Table 4–7. ■ Updated "Maximum Input and Output Clock Toggle Rate" section.	—
May 2008 v1.3	Updated: ■ Table 4–5 ■ Table 4–7 ■ Table 4–8 ■ Table 4–9 ■ Table 4–10 ■ Table 4–11 ■ Table 4–12 ■ Table 4–13 ■ Table 4–14 ■ Table 4–15 ■ Table 4–16 ■ Table 4–17 ■ Table 4–43 ■ Table 4–116 ■ Table 4–117	—
	Updated: ■ Figure 4–4	—
	Minor text edits.	—
August 2007 v1.2	Removed "Preliminary" from each page.	—
	Removed "Preliminary" note from Tables 4–44, 4–45, and 4–47.	—
	Added "Referenced Documents" section.	—
June 2007 v1.1	Updated Table 4–99.	—
	Added GIGE information.	—
May 2007 v1.0	Initial release.	—