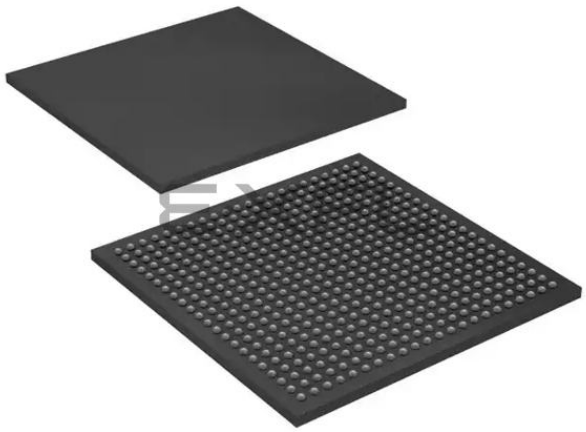

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

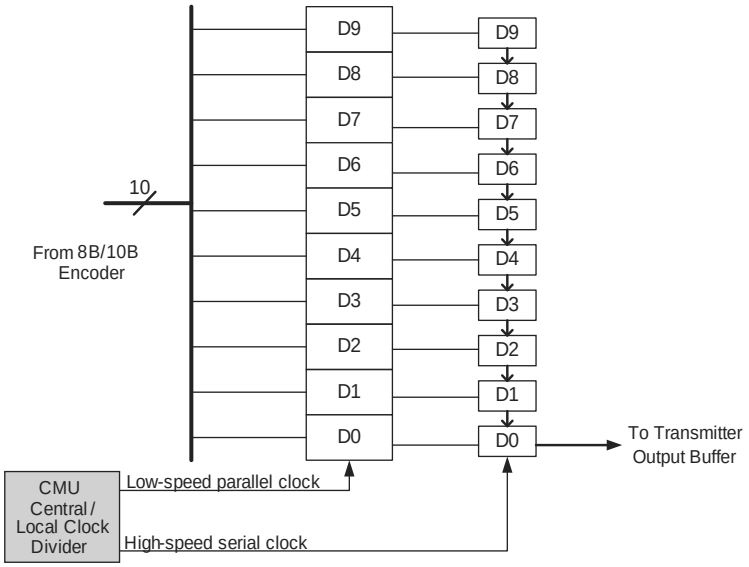
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3005
Number of Logic Elements/Cells	60100
Total RAM Bits	2528640
Number of I/O	229
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1agx60cf484i6n

Figure 2–7 shows the serializer block diagram.

Figure 2–7. Serializer



Transmitter Buffer

The Arria GX transceiver buffers support the 1.2- and 1.5-V PCML I/O standard at rates up to 3.125 Gbps. The common mode voltage (V_{CM}) of the output driver may be set to 600 or 700 mV.

For more information about the Arria GX transceiver buffers, refer to the *Arria GX Transceiver Architecture* chapter.

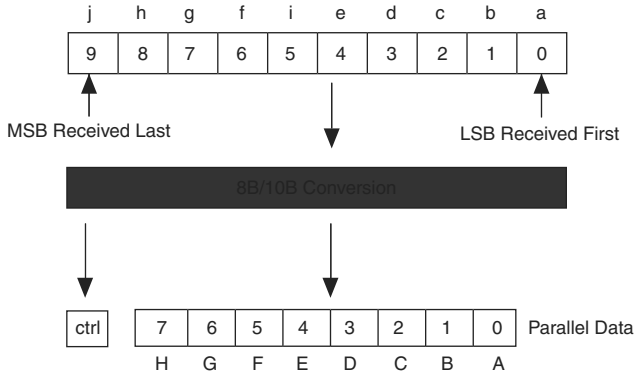
The output buffer, as shown in Figure 2–8, is directly driven by the high-speed data serializer and consists of a programmable output driver, a programmable pre-emphasis circuit, and OCT circuitry.

8B/10B Decoder

The 8B/10B decoder is used in all supported functional modes. The 8B/10B decoder takes in 10-bit data from the rate matcher and decodes it into 8-bit data + 1-bit control identifier, thereby restoring the original transmitted data at the receiver. The 8B/10B decoder indicates whether the received 10-bit character is a data or control code through the `rx_ctrldetect` port. If the received 10-bit code group is a control character (`Kx.y`), the `rx_ctrldetect` signal is driven high and if it is a data character (`Dx.y`), the `rx_ctrldetect` signal is driven low.

Figure 2–17 shows a 10-bit code group decoded to an 8-bit data and a 1-bit control indicator.

Figure 2–17. 10-Bit to 8-Bit Conversion



If the received 10-bit code is not a part of valid Dx.y or Kx.y code groups, the 8B/10B decoder block asserts an error flag on the `rx_errdetect` port. If the received 10-bit code is detected with incorrect running disparity, the 8B/10B decoder block asserts an error flag on the `rx_disperr` and `rx_errdetect` ports. The error flag signals (`rx_errdetect` and `rx_disperr`) have the same data path delay from the 8B/10B decoder to the PLD-transceiver interface as the bad code group.

Receiver State Machine

The receiver state machine operates in Basic, GIGE, PCI Express (PIPE), and XAUI modes. In GIGE mode, the receiver state machine replaces invalid code groups with K30.7. In XAUI mode, the receiver state machine translates the XAUI PCS code group to the XAUI XGMII code group.

For more information about transceiver clocking in all supported functional modes, refer to the *Arria GX Transceiver Architecture* chapter.

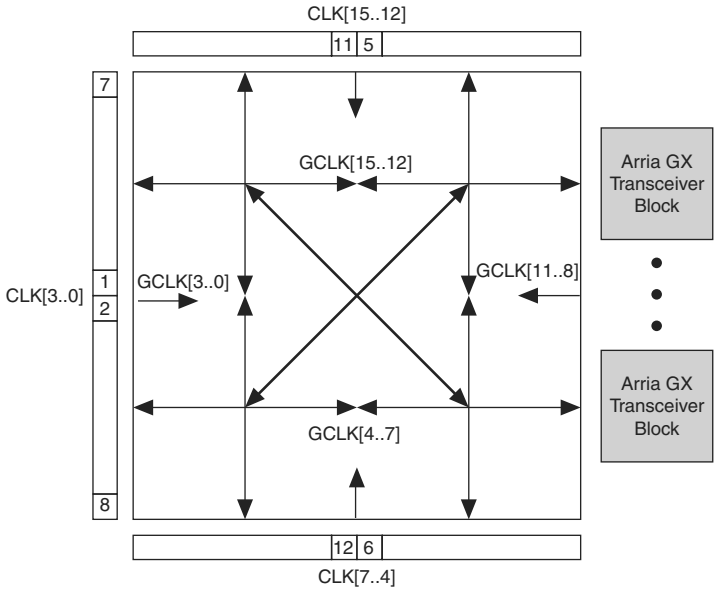
PLD Clock Utilization by Transceiver Blocks

Arria GX devices have up to 16 global clock (GCLK) lines and 16 regional clock (RCLK) lines that are used to route the transceiver clocks. The following transceiver clocks use the available global and regional clock resources:

- `pll_inclk` (if driven from an FPGA input pin)
- `rx_cruclk` (if driven from an FPGA input pin)
- `tx_clkout/coreclkout` (CMU low-speed parallel clock forwarded to the PLD)
- Recovered clock from each channel (`rx_clkout`) in non-rate matcher mode
- Calibration clock (`cal_blk_clk`)
- Fixed clock (`fixedclk` used for receiver detect circuitry in PCI Express [PIPE] mode only)

Figure 2–23 and Figure 2–24 show the available GCLK and RCLK resources in Arria GX devices.

Figure 2–23. Global Clock Resources in Arria GX Devices



One ALM contains two programmable registers. Each register has data, clock, clock enable, synchronous and asynchronous clear, asynchronous load data, and synchronous and asynchronous load/preset inputs.

Global signals, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable, preset, asynchronous load, and asynchronous load data. The asynchronous load data input comes from the `datae` or `dataf` input of the ALM, which are the same inputs that can be used for register packing. For combinational functions, the register is bypassed and the output of the LUT drives directly to the outputs of the ALM.

Each ALM has two sets of outputs that drive the local, row, and column routing resources. The LUT, adder, or register output can drive these output drivers independently (refer to Figure 2–29). For each set of output drivers, two ALM outputs can drive column, row, or direct link routing connections. One of these ALM outputs can also drive local interconnect resources. This allows the LUT or adder to drive one output while the register drives another output. This feature, called register packing, improves device utilization because the device can use the register and combinational logic for unrelated functions. Another special packing mode allows the register output to feed back into the LUT of the same ALM so that the register is packed with its own fan-out LUT. This feature provides another mechanism for improved fitting. The ALM can also drive out registered and unregistered versions of the LUT or adder output.

ALM Operating Modes

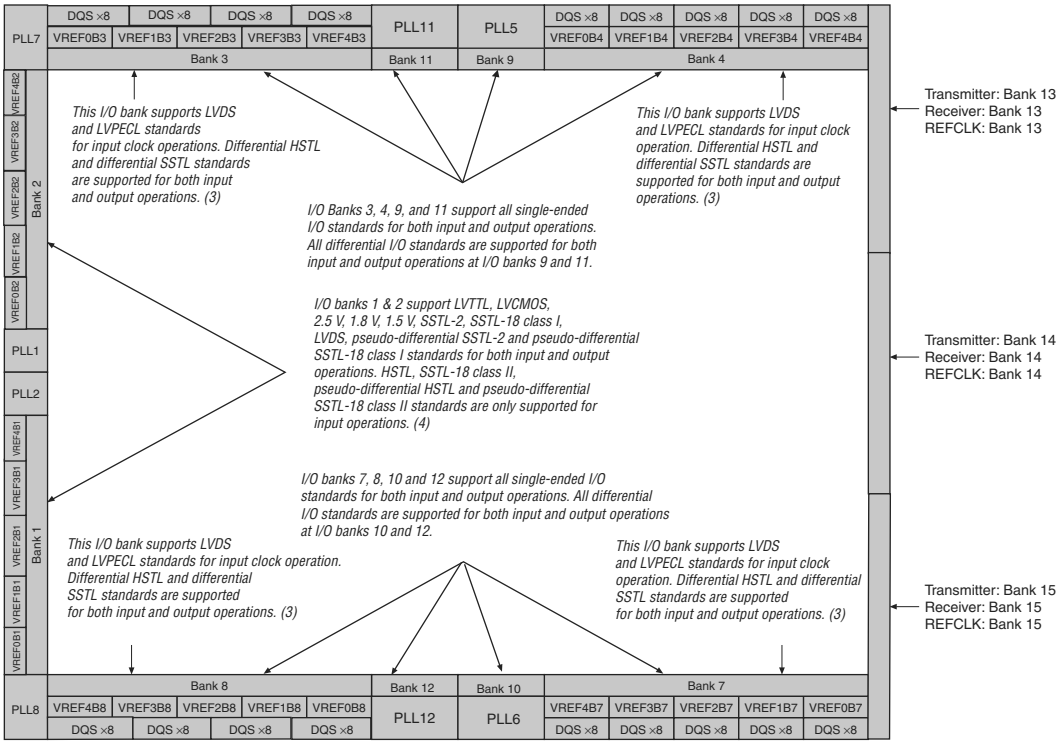
The Arria GX ALM can operate in one of the following modes:

- Normal mode
- Extended LUT mode
- Arithmetic mode
- Shared arithmetic mode

Each mode uses ALM resources differently. Each mode has 11 available inputs to the ALM (refer to Figure 2–28)—the eight data inputs from the LAB local interconnect; carry-in from the previous ALM or LAB; the shared arithmetic chain connection from the previous ALM or LAB; and the register chain connection—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset/load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all ALM modes. For more information about LAB-wide control signals, refer to “LAB Control Signals” on page 2–30.

The Quartus II software and supported third-party synthesis tools, in conjunction with parameterized functions such as library of parameterized modules (LPM) functions, automatically choose the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions. If required, you can also create special-purpose functions that specify which ALM operating mode to use for optimal performance.

Figure 2–78. Arria GX I/O Banks *(Note 1), (2)*



Notes to Figure 2–78:

(1) Figure 2–78 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

(2) Depending on the size of the device, different device members have different numbers of V_{REF} groups. For the exact locations, refer to the pin list and the Quartus II software.

(3) Banks 9 through 12 are enhanced PLL external clock output banks.

(4) Horizontal I/O banks feature SERDES and DPA circuitry for high-speed differential I/O standards. For more information about differential I/O standards, refer to the *High-Speed Differential I/O Interfaces in Arria GX Devices* chapter.

Each I/O bank has its own VCCIO pins. A single device can support 1.5-, 1.8-, 2.5-, and 3.3-V interfaces; each bank can support a different V_{CCIO} level independently. Each bank also has dedicated VREF pins to support the voltage-referenced standards (such as SSTL-2).

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. Each bank can support one V_{REF} voltage level. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTL, LVCMOS, and 3.3-V PCI for inputs and outputs.

On-Chip Termination

Arria GX devices provide differential (for the LVDS technology I/O standard) and on-chip series termination to reduce reflections and maintain signal integrity. There is no calibration support for these on-chip termination resistors. On-chip termination simplifies board design by minimizing the number of external termination resistors required. Termination can be placed inside the package, eliminating small stubs that can still lead to reflections.

Table 3–1. Arria GX JTAG Instructions

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer.
EXTEST *(1)*	00 0000 1111	Allows external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing IDCODE to be serially shifted out of TDO.
HIGHZ *(1)*	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP *(1)*	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions	—	Used when configuring an Arria GX device via the JTAG port with a USB-Blaster™, MasterBlaster™, ByteBlasterMV™, EthernetBlaster™, or ByteBlaster II download cable, or when using a **.jam** or **.jbc** via an embedded processor or JRunner™.
PULSE_NCONFIG	00 0000 0001	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.
CONFIG_IO *(2)*	00 0000 1101	Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, during, or after configuration. Stops configuration if executed during configuration. Once issued, the CONFIG_IO instruction holds nSTATUS low to reset the configuration device. nSTATUS is held low until the IOE configuration register is loaded and the TAP controller state machine transitions to the UPDATE_DR state.

Notes to Table 3–1:

(1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

(2) For more information about using the CONFIG_IO instruction, refer to the *MorphIO: An I/O Reconfiguration Solution for Altera Devices* White Paper.

Configuring Arria GX FPGAs with JRunner

The JRunner software driver configures Altera FPGAs, including Arria GX FPGAs, through the ByteBlaster™ II or ByteBlasterMV cables in JTAG mode. The programming input file supported is in Raw Binary File (**.rbf**) format. JRunner also requires a Chain Description File (**.cdf**) generated by the Quartus II software. JRunner is targeted for embedded JTAG configuration. The source code is developed for the Windows NT operating system (OS), but can be customized to run on other platforms.

For more information about the JRunner software driver, refer to the *AN414: JRunner Software Driver: An Embedded Solution for PLD JTAG Configuration* and the source files on the Altera website.

Programming Serial Configuration Devices with SRunner

You can program a serial configuration device in-system by an external microprocessor using SRunner™. SRunner is a software driver developed for embedded serial configuration device programming that can be easily customized to fit into different embedded systems. SRunner software driver reads a raw programming data file (**.rpd**) and writes to serial configuration devices. The serial configuration device programming time using SRunner software driver is comparable to the programming time when using the Quartus II software.

For more information about SRunner, refer to the *AN418: SRunner: An Embedded Solution for Serial Configuration Device Programming* and the source code on the Altera website.

For more information about programming serial configuration devices, refer to the *Serial Configuration Devices (EPCS1, EPCS4, EPCS64, and EPCS128) Data Sheet* in the *Configuration Handbook*.

Configuring Arria GX FPGAs with the MicroBlaster Driver

The MicroBlaster™ software driver supports a raw binary file (RBF) programming input file and is ideal for embedded FPP or PS configuration. The source code is developed for the Windows NT operating system, although it can be customized to run on other operating systems.

For more information about the MicroBlaster software driver, refer to the *Configuring the MicroBlaster Fast Passive Parallel Software Driver White Paper* or the *AN423: Configuring the MicroBlaster Passive Serial Software Driver*.

PLL Reconfiguration

The phase-locked loops (PLLs) in the Arria GX device family support reconfiguration of their multiply, divide, VCO-phase selection, and bandwidth selection settings without reconfiguring the entire device. You can use either serial data from the logic array or regular I/O pins to program the PLL's counter settings in a serial chain. This option provides considerable flexibility for frequency synthesis, allowing real-time variation of the PLL frequency and delay. The rest of the device is functional while reconfiguring the PLL.

Table 4–6. Arria GX Transceiver Block AC Specification (Part 3 of 3)

Symbol / Description	Conditions	–6 Speed Grade Commercial and Industrial			Units
		Min	Typ	Max	
Transmitter PLL					
VCO frequency range	—	500	—	1562.5	MHz
Bandwidth at 3.125 Gbps	BW = Low	—	3	—	MHz
	BW = Med	—	5	—	
	BW = High	—	9	—	
Bandwidth at 2.5 Gbps	BW = Low	—	1	—	MHz
	BW = Med	—	2	—	
	BW = High	—	4	—	
TX PLL lock time from `gxb_powerdown` de-assertion *(9)*, *(14)*	—	—	—	100	us
PCS					
Interface speed per mode	—	25	—	156.25	MHz
Digital Reset Pulse Width	—	Minimum is 2 parallel clock cycles			—

Notes to Table 4–6:

(1) Spread spectrum clocking is allowed only in PCI Express (PIPE) mode if the upstream transmitter and the receiver share the same clock source.
(2) The reference clock DC coupling option is only available in PCI Express (PIPE) mode for the HCSL I/O standard.
(3) The `fixedclk` is used in PIPE mode receiver detect circuitry.
(4) The device cannot tolerate prolonged operation at this absolute maximum.
(5) The rate matcher supports only up to ± 300 PPM for PIPE mode and ± 100 PPM for GIGE mode.
(6) This parameter is measured by embedding the run length data in a PRBS sequence.
(7) Signal detect threshold detector circuitry is available only in PCI Express (PIPE mode).
(8) Time taken for `rx_pll_locked` to go high from `rx_analogreset` deassertion. Refer to Figure 4–1.
(9) For lock times specific to the protocols, refer to protocol characterization documents.
(10) Time for which the CDR needs to stay in LTR mode after `rx_pll_locked` is asserted and before `rx_locktodata` is asserted in manual mode. Refer to Figure 4–1.
(11) Time taken to recover valid data from GXB after the `rx_locktodata` signal is asserted in manual mode. Measurement results are based on PRBS31, for native data rates only. Refer to Figure 4–1.
(12) Time taken to recover valid data from GXB after the `rx_freqlocked` signal goes high in automatic mode. Measurement results are based on PRBS31, for native data rates only. Refer to Figure 4–2.
(13) This is applicable only to PCI Express (PIPE) ×4 and XAUI ×4 mode.
(14) Time taken to lock `TX PLL` from `gxb_powerdown` deassertion.
(15) The 1.2 V RX VICM settings is intended for DC-coupled LVDS links.

Figure 4–1 shows the lock time parameters in manual mode. Figure 4–2 shows the lock time parameters in automatic mode.

LTD = Lock to data
LTR = Lock to reference clock

Table 4–7. Arria GX Transceiver Block AC Specification *(Note 1), (2), (3)* (Part 4 of 4)

Description	Condition	–6 Speed Grade Commercial & Industrial	Units
SDI Receiver Jitter Tolerance *(8)*			
Sinusoidal Jitter Tolerance (peak-to-peak)	Jitter Frequency = 15 KHz Data Rate = 2.97 Gbps (3G) REFCLK = 148.5 MHz Pattern = Single Line Scramble Color Bar No Equalization DC Gain = 0 dB	> 2	UI
	Jitter Frequency = 100 KHz Data Rate = 2.97 Gbps (3G) REFCLK = 148.5 MHz Pattern = Single Line Scramble Color Bar No Equalization DC Gain = 0 dB	> 0.3	UI
	Jitter Frequency = 148.5 MHz Data Rate = 2.97 Gbps (3G) REFCLK = 148.5 MHz Pattern = Single Line Scramble Color Bar No Equalization DC Gain = 0 dB	> 0.3	UI
Sinusoidal Jitter Tolerance (peak-to-peak)	Jitter Frequency = 20 KHz Data Rate = 1.485 Gbps (HD) REFCLK = 74.25 MHz Pattern = 75% Color Bar No Equalization DC Gain = 0 dB	> 1	UI
	Jitter Frequency = 100 KHz Data Rate = 1.485 Gbps (HD) REFCLK = 74.25 MHz Pattern = 75% Color Bar No Equalization DC Gain = 0 dB	> 0.2	UI

Notes to Table 4–7:

(1) Dedicated REFCLK pins were used to drive the input reference clocks.
(2) Jitter numbers specified are valid for the stated conditions only.
(3) Refer to the protocol characterization documents for detailed information.
(4) The jitter numbers for XAUI are compliant to the IEEE802.3ae-2002 Specification.
(5) The jitter numbers for PCI Express are compliant to the PCIe Base Specification 2.0.
(6) The jitter numbers for Serial RapidIO are compliant to the RapidIO Specification 1.3.
(7) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
(8) The HD-SDI and 3G-SDI jitter numbers are compliant to the SMPTE292M and SMPTE424M specifications.

Table 4–24. 3.3-V PCI Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	—	0.5 V_{CCIO}	—	V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage	—	–0.3	—	0.3 V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 V_{CCIO}	—	—	V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA	—	—	0.1 V_{CCIO}	V

Table 4–25. PCI-X Mode 1 Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage	—	3.0	3.6	V
V_{IH}	High-level input voltage	—	0.5 V_{CCIO}	V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 V_{CCIO}	V
V_{IPU}	Input pull-up voltage	—	0.7 V_{CCIO}	—	V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 V_{CCIO}	—	V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA	—	0.1 V_{CCIO}	V

Table 4–26. SSTL-18 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	1.71	1.8	1.89	V
V_{REF}	Reference voltage	—	0.855	0.9	0.945	V
V_{TT}	Termination voltage	—	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{IH} (DC)	High-level DC input voltage	—	V_{REF} + 0.125	—	—	V
V_{IL} (DC)	Low-level DC input voltage	—	—	—	V_{REF} – 0.125	V
V_{IH} (AC)	High-level AC input voltage	—	V_{REF} + 0.25	—	—	V
V_{IL} (AC)	Low-level AC input voltage	—	—	—	V_{REF} – 0.25	V
V_{OH}	High-level output voltage	I_{OH} = –6.7 mA *(1)*	V_{TT} + 0.475	—	—	V
V_{OL}	Low-level output voltage	I_{OL} = 6.7 mA *(1)*	—	—	V_{TT} – 0.475	V

Note to Table 4–26:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Arria GX Architecture* chapter.

Table 4–27. SSTL-18 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	1.71	1.8	1.89	V
V_{REF}	Reference voltage	—	0.855	0.9	0.945	V
V_{TT}	Termination voltage	—	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{IH} (DC)	High-level DC input voltage	—	V_{REF} + 0.125	—	—	V
V_{IL} (DC)	Low-level DC input voltage	—	—	—	V_{REF} – 0.125	V
V_{IH} (AC)	High-level AC input voltage	—	V_{REF} + 0.25	—	—	V
V_{IL} (AC)	Low-level AC input voltage	—	—	—	V_{REF} – 0.25	V

Table 4–30. SSTL-2 Class II Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IL} (DC)	Low-level DC input voltage	—	–0.3	—	V_{REF} – 0.18	V
V_{IH} (AC)	High-level AC input voltage	—	V_{REF} + 0.35	—	—	V
V_{IL} (AC)	Low-level AC input voltage	—	—	—	V_{REF} – 0.35	V
V_{OH}	High-level output voltage	I_{OH} = –16.4 mA *(1)*	V_{TT} + 0.76	—	—	V
V_{OL}	Low-level output voltage	I_{OL} = 16.4 mA *(1)*	—	—	V_{TT} – 0.76	V

Note to Table 4–30:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Arria GX Architecture* chapter.

Table 4–31. SSTL-2 Class I & II Differential Specifications *(Note 1)*

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	2.375	2.5	2.625	V
V_{SWING} (DC)	DC differential input voltage	0.36	—	—	V
V_X (AC)	AC differential input cross point voltage	(V_{CCIO}/2) – 0.2	—	(V_{CCIO}/2) + 0.2	V
V_{SWING} (AC)	AC differential input voltage	0.7	—	—	V
V_{ISO}	Input clock signal offset voltage	—	0.5 V_{CCIO}	—	V
ΔV_{ISO}	Input clock signal offset voltage variation	—	200	—	mV
V_{OX} (AC)	AC differential output cross point voltage	(V_{CCIO}/2) – 0.2	—	(V_{CCIO}/2) + 0.2	V

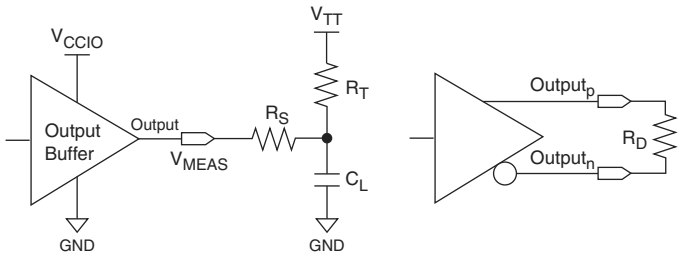
Note to Table 4–31:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Arria GX Architecture* chapter.

Table 4–32. 1.2-V HSTL Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	1.14	1.2	1.26	V
V_{REF}	Reference voltage	0.48 V_{CCIO}	0.5 V_{CCIO}	0.52 V_{CCIO}	V
V_{IH} (DC)	High-level DC input voltage	V_{REF} + 0.08	—	V_{CCIO} + 0.15	V
V_{IL} (DC)	Low-level DC input voltage	–0.15	—	V_{REF} – 0.08	V
V_{IH} (AC)	High-level AC input voltage	V_{REF} + 0.15	—	V_{CCIO} + 0.24	V
V_{IL} (AC)	Low-level AC input voltage	–0.24	—	V_{REF} – 0.15	V
V_{OH}	High-level output voltage	V_{REF} + 0.15	—	V_{CCIO} + 0.15	V
V_{OL}	Low-level output voltage	–0.15	—	V_{REF} – 0.15	V

Figure 4–7. Output Delay Timing Reporting Setup Modeled by Quartus II



Notes to Figure 4–7:

(1) Output pin timing is reported at the output pin of the FPGA device. Additional delays for loading and board trace delay need to be accounted for with IBIS model simulations.

(2) V_{CCPD} is 3.085 V unless otherwise specified.

(3) V_{CCINT} is 1.12 V unless otherwise specified.

Table 4–44. Output Timing Measurement Methodology for Output Pins *(Note 1), (2), (3)*

I/O Standard	Loading and Termination						Measurement Point
	R_S (Ω)	R_D (Ω)	R_T (Ω)	V_{CCIO} (V)	V_{TT} (V)	C_L (pF)	V_{MEAS} (V)
LVTTL *(4)*	—	—	—	3.135	—	0	1.5675
LVCMOS *(4)*	—	—	—	3.135	—	0	1.5675
2.5 V *(4)*	—	—	—	2.375	—	0	1.1875
1.8 V *(4)*	—	—	—	1.710	—	0	0.855
1.5 V *(4)*	—	—	—	1.425	—	0	0.7125
PCI *(5)*	—	—	—	2.970	—	10	1.485
PCI-X *(5)*	—	—	—	2.970	—	10	1.485
SSTL-2 Class I	25	—	50	2.325	1.123	0	1.1625
SSTL-2 Class II	25	—	25	2.325	1.123	0	1.1625
SSTL-18 Class I	25	—	50	1.660	0.790	0	0.83
SSTL-18 Class II	25	—	25	1.660	0.790	0	0.83
1.8-V HSTL Class I	—	—	50	1.660	0.790	0	0.83
1.8-V HSTL Class II	—	—	25	1.660	0.790	0	0.83
1.5-V HSTL Class I	—	—	50	1.375	0.648	0	0.6875
1.5-V HSTL Class II	—	—	25	1.375	0.648	0	0.6875
1.2-V HSTL with OCT	—	—	—	1.140	—	0	0.570
Differential SSTL-2 Class I	25	—	50	2.325	1.123	0	1.1625
Differential SSTL-2 Class II	25	—	25	2.325	1.123	0	1.1625
Differential SSTL-18 Class I	50	—	50	1.660	0.790	0	0.83
Differential SSTL-18 Class II	25	—	25	1.660	0.790	0	0.83
1.5-V differential HSTL Class I	—	—	50	1.375	0.648	0	0.6875
1.5-V differential HSTL Class II	—	—	25	1.375	0.648	0	0.6875
1.8-V differential HSTL Class I	—	—	50	1.660	0.790	0	0.83

Table 4–45. Timing Measurement Methodology for Input Pins *(Note 1)*, *(2)*, *(3)*, *(4)* (Part 2 of 2)

I/O Standard	Measurement Conditions			Measurement Point
	V_{CCIO} (V)	V_{REF} (V)	Edge Rate (ns)	VMEAS (V)
Differential SSTL-18 Class II	1.660	0.830	1.660	0.83
1.5-V differential HSTL Class I	1.375	0.688	1.375	0.6875
1.5-V differential HSTL Class II	1.375	0.688	1.375	0.6875
1.8-V differential HSTL Class I	1.660	0.830	1.660	0.83
1.8-V differential HSTL Class II	1.660	0.830	1.660	0.83
LVDS	2.325	—	0.100	1.1625
LVPECL	3.135	—	0.100	1.5675

Notes to Table 4–45:

(1) Input buffer sees no load at buffer input.
(2) Input measuring point at buffer input is 0.5 V_{CCIO}.
(3) Output measuring point is 0.5 V_{CC} at internal node.
(4) Input edge rate is 1 V/ns.
(5) Less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V with less than 30-mV ripple.
(6) V_{CCPD} = 2.97 V, less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V.

Clock Network Skew Adders

The Quartus II software models skew within dedicated clock networks such as global and regional clocks. Therefore, the intra-clock network skew adder is not specified. Table 4–46 specifies the intra clock skew between any two clock networks driving any registers in the Arria GX device.

Table 4–46. Clock Network Specifications

Name	Description	Min	Typ	Max	Units
Clock skew adder EP1AGX20/35 *(1)*	Inter-clock network, same side	—	—	± 50	ps
	Inter-clock network, entire chip	—	—	± 100	ps
Clock skew adder EP1AGX50/60 *(1)*	Inter-clock network, same side	—	—	± 50	ps
	Inter-clock network, entire chip	—	—	± 100	ps
Clock skew adder EP1AGX90 *(1)*	Inter-clock network, same side	—	—	± 55	ps
	Inter-clock network, entire chip	—	—	± 110	ps

Note to Table 4–46:

(1) This is in addition to intra-clock network skew, which is modeled in the Quartus II software.

Default Capacitive Loading of Different I/O Standards

See Table 4–47 for default capacitive loading of different I/O standards.

Table 4–47. Default Loading of Different I/O Standards for Arria GX Devices (Part 1 of 2)

I/O Standard	Capacitive Load	Units
LVTTL	0	pF
LVCMOS	0	pF
2.5 V	0	pF

Table 4–51. EP1AGX20 Column Pins Output Timing Parameters (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
1.8 V	6 mA	GCLK	t_{CO}	2.695	2.695	6.155	ns
		GCLK PLL	t_{CO}	1.253	1.253	3.049	ns
1.8 V	8 mA	GCLK	t_{CO}	2.697	2.697	6.064	ns
		GCLK PLL	t_{CO}	1.255	1.255	2.958	ns
1.8 V	10 mA	GCLK	t_{CO}	2.651	2.651	5.987	ns
		GCLK PLL	t_{CO}	1.209	1.209	2.881	ns
1.8 V	12 mA	GCLK	t_{CO}	2.652	2.652	5.930	ns
		GCLK PLL	t_{CO}	1.210	1.210	2.824	ns
1.5 V	2 mA	GCLK	t_{CO}	2.746	2.746	6.723	ns
		GCLK PLL	t_{CO}	1.304	1.304	3.617	ns
1.5 V	4 mA	GCLK	t_{CO}	2.682	2.682	6.154	ns
		GCLK PLL	t_{CO}	1.240	1.240	3.048	ns
1.5 V	6 mA	GCLK	t_{CO}	2.685	2.685	6.036	ns
		GCLK PLL	t_{CO}	1.243	1.243	2.930	ns
1.5 V	8 mA	GCLK	t_{CO}	2.644	2.644	5.983	ns
		GCLK PLL	t_{CO}	1.202	1.202	2.877	ns
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.629	2.629	5.762	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.650	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.612	2.612	5.712	ns
		GCLK PLL	t_{CO}	1.167	1.167	2.600	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.590	2.590	5.639	ns
		GCLK PLL	t_{CO}	1.145	1.145	2.527	ns
SSTL-2 CLASS II	20 mA	GCLK	t_{CO}	2.591	2.591	5.626	ns
		GCLK PLL	t_{CO}	1.146	1.146	2.514	ns
SSTL-2 CLASS II	24 mA	GCLK	t_{CO}	2.587	2.587	5.624	ns
		GCLK PLL	t_{CO}	1.142	1.142	2.512	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.626	2.626	5.733	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.627	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.630	2.630	5.694	ns
		GCLK PLL	t_{CO}	1.185	1.185	2.582	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.609	2.609	5.675	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.563	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.614	2.614	5.673	ns
		GCLK PLL	t_{CO}	1.169	1.169	2.561	ns
SSTL-18 CLASS I	12 mA	GCLK	t_{CO}	2.608	2.608	5.659	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.547	ns
SSTL-18 CLASS II	8 mA	GCLK	t_{CO}	2.597	2.597	5.625	ns
		GCLK PLL	t_{CO}	1.152	1.152	2.513	ns

Table 4–59 lists column pin delay adders when using the regional clock in Arria GX devices.

Table 4–59. EP1AGX35 Column Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.099	0.099	0.254	ns
RCLK PLL input adder	–0.012	–0.012	–0.01	ns
RCLK output adder	–0.086	–0.086	–0.244	ns
RCLK PLL output adder	1.253	1.253	3.133	ns

EP1AGX50 I/O Timing Parameters

Table 4–60 through Table 4–63 list the maximum I/O timing parameters for EP1AGX50 devices for I/O standards which support general purpose I/O pins.

Table 4–60 lists I/O timing specifications.

Table 4–60. EP1AGX50 Row Pins Input Timing Parameters (Part 1 of 2)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.550	1.550	3.542	ns
		t_H	–1.445	–1.445	–3.265	ns
	GCLK PLL	t_{SU}	2.978	2.978	6.626	ns
		t_H	–2.873	–2.873	–6.349	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.550	1.550	3.542	ns
		t_H	–1.445	–1.445	–3.265	ns
	GCLK PLL	t_{SU}	2.978	2.978	6.626	ns
		t_H	–2.873	–2.873	–6.349	ns
2.5 V	GCLK	t_{SU}	1.562	1.562	3.523	ns
		t_H	–1.457	–1.457	–3.246	ns
	GCLK PLL	t_{SU}	2.990	2.990	6.607	ns
		t_H	–2.885	–2.885	–6.330	ns
1.8 V	GCLK	t_{SU}	1.628	1.628	3.730	ns
		t_H	–1.523	–1.523	–3.453	ns
	GCLK PLL	t_{SU}	3.056	3.056	6.814	ns
		t_H	–2.951	–2.951	–6.537	ns
1.5 V	GCLK	t_{SU}	1.631	1.631	3.825	ns
		t_H	–1.526	–1.526	–3.548	ns
	GCLK PLL	t_{SU}	3.059	3.059	6.909	ns
		t_H	–2.954	–2.954	–6.632	ns

Table 4–60. EP1AGX50 Row Pins Input Timing Parameters (Part 2 of 2)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
SSTL-2 CLASS I	GCLK	t_{SU}	1.375	1.375	2.997	ns
		t_H	–1.270	–1.270	–2.720	ns
	GCLK PLL	t_{SU}	2.802	2.802	6.079	ns
		t_H	–2.697	–2.697	–5.802	ns
SSTL-2 CLASS II	GCLK	t_{SU}	1.375	1.375	2.997	ns
		t_H	–1.270	–1.270	–2.720	ns
	GCLK PLL	t_{SU}	2.802	2.802	6.079	ns
		t_H	–2.697	–2.697	–5.802	ns
SSTL-18 CLASS I	GCLK	t_{SU}	1.406	1.406	3.104	ns
		t_H	–1.301	–1.301	–2.827	ns
	GCLK PLL	t_{SU}	2.834	2.834	6.188	ns
		t_H	–2.729	–2.729	–5.911	ns
SSTL-18 CLASS II	GCLK	t_{SU}	1.407	1.407	3.106	ns
		t_H	–1.302	–1.302	–2.829	ns
	GCLK PLL	t_{SU}	2.834	2.834	6.188	ns
		t_H	–2.729	–2.729	–5.911	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	1.406	1.406	3.104	ns
		t_H	–1.301	–1.301	–2.827	ns
	GCLK PLL	t_{SU}	2.834	2.834	6.188	ns
		t_H	–2.729	–2.729	–5.911	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	1.407	1.407	3.106	ns
		t_H	–1.302	–1.302	–2.829	ns
	GCLK PLL	t_{SU}	2.834	2.834	6.188	ns
		t_H	–2.729	–2.729	–5.911	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.432	1.432	3.232	ns
		t_H	–1.327	–1.327	–2.955	ns
	GCLK PLL	t_{SU}	2.860	2.860	6.316	ns
		t_H	–2.755	–2.755	–6.039	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.433	1.433	3.234	ns
		t_H	–1.328	–1.328	–2.957	ns
	GCLK PLL	t_{SU}	2.860	2.860	6.316	ns
		t_H	–2.755	–2.755	–6.039	ns
LVDS	GCLK	t_{SU}	1.341	1.341	3.088	ns
		t_H	–1.236	–1.236	–2.811	ns
	GCLK PLL	t_{SU}	2.769	2.769	6.171	ns
		t_H	–2.664	–2.664	–5.894	ns

Table 4–62. EP1AGX50 Row Pins Output Timing Parameters (Part 3 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.606	2.606	5.480	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.396	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.608	2.608	5.442	ns
		GCLK PLL	t_{CO}	1.181	1.181	2.360	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.590	2.590	5.438	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.356	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.594	2.594	5.427	ns
		GCLK PLL	t_{CO}	1.167	1.167	2.345	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.585	2.585	5.426	ns
		GCLK PLL	t_{CO}	1.158	1.158	2.344	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.605	2.605	5.457	ns
		GCLK PLL	t_{CO}	1.177	1.177	2.373	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.607	2.607	5.441	ns
		GCLK PLL	t_{CO}	1.180	1.180	2.359	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.592	2.592	5.433	ns
		GCLK PLL	t_{CO}	1.165	1.165	2.351	ns
LVDS	—	GCLK	t_{CO}	2.654	2.654	5.613	ns
		GCLK PLL	t_{CO}	1.226	1.226	2.530	ns

Table 4–63 lists I/O timing specifications.

Table 4–63. EP1AGX50 Column Pins Output Timing Parameters (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	2.948	2.948	6.608	ns
		GCLK PLL	t_{CO}	1.476	1.476	3.447	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.797	2.797	6.203	ns
		GCLK PLL	t_{CO}	1.331	1.331	3.075	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.722	2.722	6.204	ns
		GCLK PLL	t_{CO}	1.264	1.264	3.075	ns
3.3-V LVTTL	16 mA	GCLK	t_{CO}	2.694	2.694	6.024	ns
		GCLK PLL	t_{CO}	1.238	1.238	2.906	ns
3.3-V LVTTL	20 mA	GCLK	t_{CO}	2.670	2.670	5.896	ns
		GCLK PLL	t_{CO}	1.216	1.216	2.781	ns
3.3-V LVTTL	24 mA	GCLK	t_{CO}	2.660	2.660	5.895	ns
		GCLK PLL	t_{CO}	1.209	1.209	2.783	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.797	2.797	6.203	ns
		GCLK PLL	t_{CO}	1.331	1.331	3.075	ns

Table 4–64 lists row pin delay adders when using the regional clock in Arria GX devices.

Table 4–64. EP1AGX50 Row Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.151	0.151	0.329	ns
RCLK PLL input adder	0.011	0.011	0.016	ns
RCLK output adder	–0.151	–0.151	–0.329	ns
RCLK PLL output adder	–0.011	–0.011	–0.016	ns

Table 4–65 lists column pin delay adders when using the regional clock in Arria GX devices.

Table 4–65. EP1AGX50 Column Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.146	0.146	0.334	ns
RCLK PLL input adder	–1.713	–1.713	–3.645	ns
RCLK output adder	–0.146	–0.146	–0.336	ns
RCLK PLL output adder	1.716	1.716	4.488	ns

EP1AGX60 I/O Timing Parameters

Table 4–66 through Table 4–69 list the maximum I/O timing parameters for EP1AGX60 devices for I/O standards which support general purpose I/O pins.

Table 4–66 lists I/O timing specifications.

Table 4–66. EP1AGX60 Row Pins Input Timing Parameters (Part 1 of 3)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.413	1.413	3.113	ns
		t_H	–1.308	–1.308	–2.836	ns
	GCLK PLL	t_{SU}	2.975	2.975	6.536	ns
		t_H	–2.870	–2.870	–6.259	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.413	1.413	3.113	ns
		t_H	–1.308	–1.308	–2.836	ns
	GCLK PLL	t_{SU}	2.975	2.975	6.536	ns
		t_H	–2.870	–2.870	–6.259	ns
2.5 V	GCLK	t_{SU}	1.425	1.425	3.094	ns
		t_H	–1.320	–1.320	–2.817	ns
	GCLK PLL	t_{SU}	2.987	2.987	6.517	ns
		t_H	–2.882	–2.882	–6.240	ns

Table 4–69. EP1AGX60 Column Pins Output Timing Parameters (Part 3 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
SSTL-18 CLASS II	16 mA	GCLK	t_{CO}	2.737	2.737	6.025	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.585	ns
SSTL-18 CLASS II	18 mA	GCLK	t_{CO}	2.733	2.733	6.033	ns
		GCLK PLL	t_{CO}	1.160	1.160	2.593	ns
SSTL-18 CLASS II	20 mA	GCLK	t_{CO}	2.733	2.733	6.031	ns
		GCLK PLL	t_{CO}	1.160	1.160	2.591	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.756	2.756	6.086	ns
		GCLK PLL	t_{CO}	1.186	1.186	2.651	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.762	2.762	6.071	ns
		GCLK PLL	t_{CO}	1.189	1.189	2.631	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.740	2.740	6.060	ns
		GCLK PLL	t_{CO}	1.167	1.167	2.620	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.744	2.744	6.066	ns
		GCLK PLL	t_{CO}	1.171	1.171	2.626	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.736	2.736	6.059	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.619	ns
1.8-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.719	2.719	5.823	ns
		GCLK PLL	t_{CO}	1.146	1.146	2.383	ns
1.8-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.721	2.721	5.834	ns
		GCLK PLL	t_{CO}	1.148	1.148	2.394	ns
1.8-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.721	2.721	5.843	ns
		GCLK PLL	t_{CO}	1.148	1.148	2.403	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.756	2.756	6.085	ns
		GCLK PLL	t_{CO}	1.186	1.186	2.650	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.761	2.761	6.063	ns
		GCLK PLL	t_{CO}	1.188	1.188	2.623	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.743	2.743	6.065	ns
		GCLK PLL	t_{CO}	1.170	1.170	2.625	ns
1.5-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.743	2.743	6.067	ns
		GCLK PLL	t_{CO}	1.170	1.170	2.627	ns
1.5-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.737	2.737	6.065	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.625	ns
1.5-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.724	2.724	5.877	ns
		GCLK PLL	t_{CO}	1.151	1.151	2.437	ns
1.5-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.727	2.727	5.887	ns
		GCLK PLL	t_{CO}	1.154	1.154	2.447	ns
1.5-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.729	2.729	5.900	ns
		GCLK PLL	t_{CO}	1.156	1.156	2.460	ns