Altera - EP1AGX60DF780C6N Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

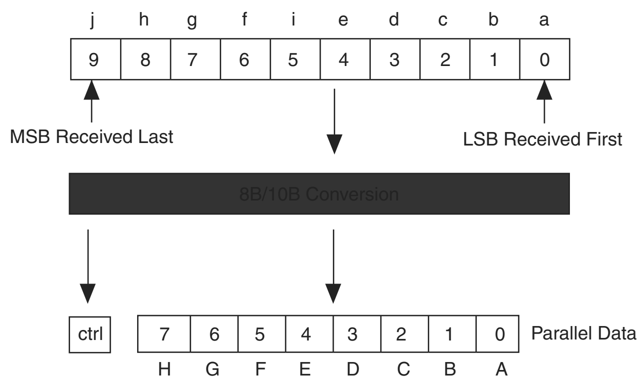
Details	
Product Status	Active
Number of LABs/CLBs	3005
Number of Logic Elements/Cells	60100
Total RAM Bits	2528640
Number of I/O	350
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep1agx60df780c6n

8B/10B Decoder

The 8B/10B decoder is used in all supported functional modes. The 8B/10B decoder takes in 10-bit data from the rate matcher and decodes it into 8-bit data + 1-bit control identifier, thereby restoring the original transmitted data at the receiver. The 8B/10B decoder indicates whether the received 10-bit character is a data or control code through the `rx_ctrldetect` port. If the received 10-bit code group is a control character (`Kx.y`), the `rx_ctrldetect` signal is driven high and if it is a data character (`Dx.y`), the `rx_ctrldetect` signal is driven low.

Figure 2–17 shows a 10-bit code group decoded to an 8-bit data and a 1-bit control indicator.

Figure 2–17. 10-Bit to 8-Bit Conversion

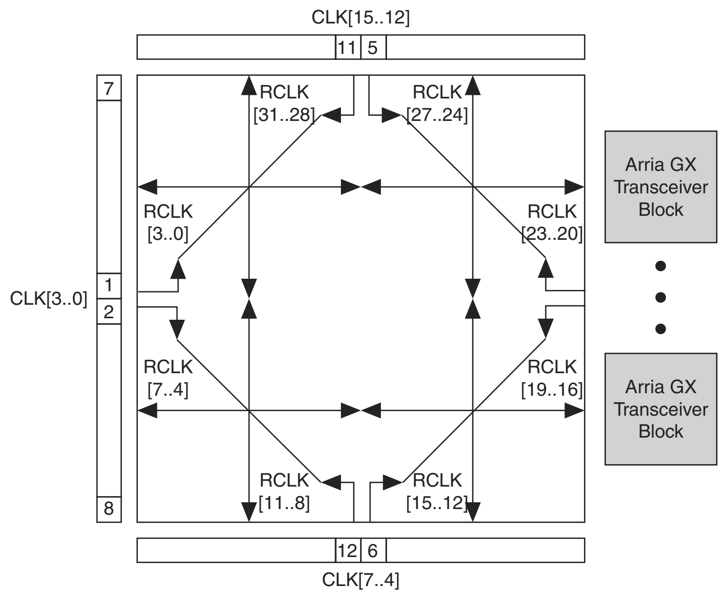


If the received 10-bit code is not a part of valid Dx.y or Kx.y code groups, the 8B/10B decoder block asserts an error flag on the `rx_errdetect` port. If the received 10-bit code is detected with incorrect running disparity, the 8B/10B decoder block asserts an error flag on the `rx_disperr` and `rx_errdetect` ports. The error flag signals (`rx_errdetect` and `rx_disperr`) have the same data path delay from the 8B/10B decoder to the PLD-transceiver interface as the bad code group.

Receiver State Machine

The receiver state machine operates in Basic, GIGE, PCI Express (PIPE), and XAUI modes. In GIGE mode, the receiver state machine replaces invalid code groups with K30.7. In XAUI mode, the receiver state machine translates the XAUI PCS code group to the XAUI XGMII code group.

Figure 2–24. Regional Clock Resources in Arria GX Devices



For the RCLK or GCLK network to route into the transceiver, a local route input output (LRIO) channel is required. Each LRIO clock region has up to eight clock paths and each transceiver block has a maximum of eight clock paths for connecting with LRIO clocks. These resources are limited and determine the number of clocks that can be used between the PLD and transceiver blocks. Table 2–7 and Table 2–8 list the number of LRIO resources available for Arria GX devices with different numbers of transceiver blocks.

Table 2–7. Available Clocking Connections for Transceivers in EP1AGX35D, EP1AGX50D, and EP1AGX60D

Source	Clock Resource		Transceiver	
	Global Clock	Regional Clock	Bank13 8 Clock I/O	Bank14 8 Clock I/O
Region0 8 LRIO clock	✓	RCLK 20-27	✓	—
Region1 8 LRIO clock	✓	RCLK 12-19	—	✓

Table 2–8. Available Clocking Connections for Transceivers in EP1AGX60E and EP1AGX90E

Source	Clock Resource		Transceiver		
	Global Clock	Regional Clock	Bank13 8 Clock I/O	Bank14 8 Clock I/O	Bank15 8 Clock I/O
Region0 8 LRIO clock	✓	RCLK 20-27	✓	—	—
Region1 8 LRIO clock	✓	RCLK 20-27	✓	✓	—
Region2 8 LRIO clock	✓	RCLK 12-19	—	✓	✓
Region3 8 LRIO clock	✓	RCLK 12-19	—	—	✓

In addition to the clear and load/preset ports, Arria GX devices provide a device-wide reset pin (`DEV_CLRn`) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This device-wide reset overrides all other control signals.

MultiTrack Interconnect

In Arria GX architecture, the MultiTrack interconnect structure with DirectDrive technology provides connections between ALMs, TriMatrix memory, DSP blocks, and device I/O pins. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different lengths and speeds used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement in the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when migrating through different device densities. Dedicated row interconnects route signals to and from LABs, DSP blocks, and TriMatrix memory in the same row.

These row resources include:

- Direct link interconnects between LABs and adjacent blocks
- R4 interconnects traversing four blocks to the right or left
- R24 row interconnects for high-speed access across the length of the device

The direct link interconnect allows a LAB, DSP block, or TriMatrix memory block to drive into the local interconnect of its left and right neighbors and then back into itself, providing fast communication between adjacent LABs and/or blocks without using row interconnect resources.

The R4 interconnects span four LABs, three LABs and one M512 RAM block, two LABs and one M4K RAM block, or two LABs and one DSP block to the right or left of a source LAB. These resources are used for fast row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. Figure 2–39 shows R4 interconnect connections from a LAB.

R4 interconnects can drive and be driven by DSP blocks and RAM blocks and row IOEs. For LAB interfacing, a primary LAB or LAB neighbor can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive onto the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive onto the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. R4 interconnects can also drive C4 and C16 interconnects for connections from one row to another. Additionally, R4 interconnects can drive R24 interconnects.

Figure 2–52 and Figure 2–53 show the DSP block interfaces to LAB rows.

Figure 2–52. DSP Block Interconnect Interface

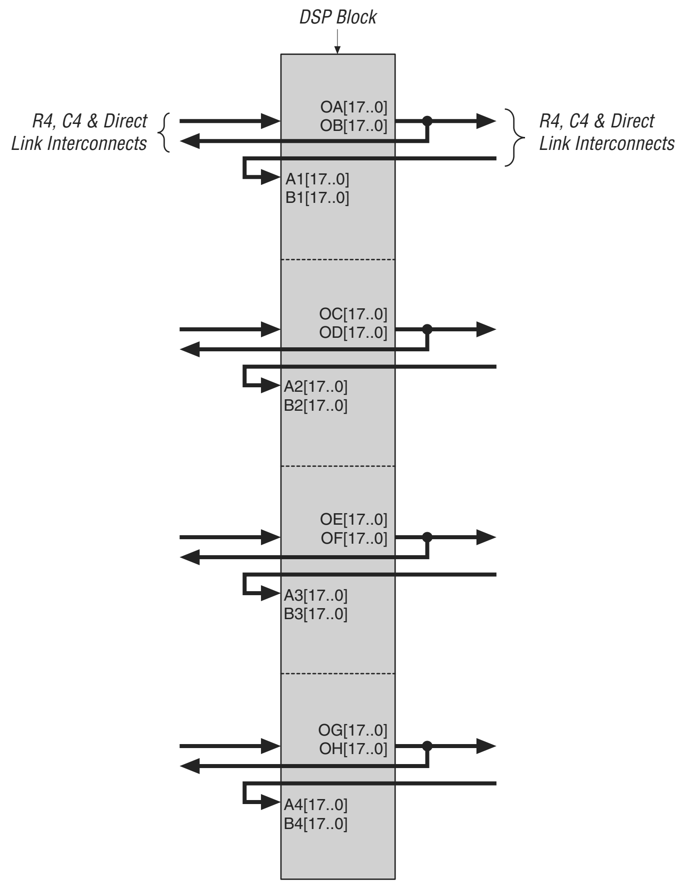


Table 2–15. DSP Block Signal Sources and Destinations

LAB Row at Interface	Control Signals Generated	Data Inputs	Data Outputs
0	clock0 aclr0 ena0 mult01_saturate addnsub1_round/ accum_round addnsub1 signa sourcea sourceb	A1[17..0] B1[17..0]	OA[17..0] OB[17..0]
1	clock1 aclr1 ena1 accum_saturate mult01_round accum_sload sourcea sourceb mode0	A2[17..0] B2[17..0]	OC[17..0] OD[17..0]
2	clock2 aclr2 ena2 mult23_saturate addnsub3_round/ accum_round addnsub3 sign_b sourcea sourceb	A3[17..0] B3[17..0]	OE[17..0] OF[17..0]
3	clock3 aclr3 ena3 accum_saturate mult23_round accum_sload sourcea sourceb mode1	A4[17..0] B4[17..0]	OG[17..0] OH[17..0]

Table 2–19. Global and Regional Clock Connections from Left Side Clock Pins and Fast PLL Outputs (Part 2 of 2)

Left Side Global & Regional Clock Network Connectivity	CLK0	CLK1	CLK2	CLK3	RCLK0	RCLK1	RCLK2	RCLK3	RCLK4	RCLK5	RCLK6	RCLK7
RCLKDRV7	—	—	—	—	—	—	—	✓	—	—	—	✓
PLL 1 Outputs												
c0	✓	✓	—	—	✓	—	✓	—	✓	—	✓	—
c1	✓	✓	—	—	—	✓	—	✓		✓	—	✓
c2	—	—	✓	✓	✓	—	✓	—	✓	—	✓	—
c3	—	—	✓	✓	—	✓	—	✓	—	✓	—	✓
PLL 2 Outputs												
c0	✓	✓	—	—	—	✓	—	✓	—	✓	—	✓
c1	✓	✓	—	—	✓	—	✓	—	✓	—	✓	—
c2	—	—	✓	✓	—	✓	—	✓	—	✓	—	✓
c3	—	—	✓	✓	✓	—	✓	—	✓	—	✓	—
PLL 7 Outputs												
c0	—	—	✓	✓	—	✓	—	✓	—	—	—	—
c1	—	—	✓	✓	✓	—	✓	—	—	—	—	—
c2	✓	✓	—	—	—	✓	—	✓	—	—	—	—
c3	✓	✓	—	—	✓	—	✓	—	—	—	—	—
PLL 8 Outputs												
c0	—	—	✓	✓	—	—	—	—	✓	—	✓	—
c1	—	—	✓	✓	—	—	—	—	—	✓	—	✓
c2	✓	✓	—	—	—	—	—	—	✓	—	✓	—
c3	✓	✓	—	—	—	—	—	—	—	✓	—	✓

A path in which a pin directly drives a register can require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinational logic may not require the delay. Programmable delays exist for decreasing input-pin-to-logic-array and IOE input register delays. The Quartus II Compiler can program these delays to automatically minimize setup time while providing a zero hold time. Programmable delays can increase the register-to-pin delays for output and/or output enable registers. Programmable delays are no longer required to ensure zero hold times for logic array register-to-IOE register transfers. The Quartus II Compiler can create zero hold time for these transfers. Table 2–22 shows the programmable delays for Arria GX devices.

Table 2–22. Arria GX Devices Programmable Delay Chain

Programmable Delays	Quartus II Logic Option
Input pin to logic array delay	Input delay from pin to internal cells
Input pin to input register delay	Input delay from pin to input register
Output pin delay	Delay from output register to output pin
Output enable register t_{CO} delay	Delay to output enable pin

IOE registers in Arria GX devices share the same source for clear or preset. You can program preset or clear for each individual IOE. You can also program the registers to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power-up. If one register in an IOE uses a preset or clear signal, all registers in the IOE must use that same signal if they require preset or clear. Additionally, a synchronous reset signal is available for the IOE registers.

Double Data Rate I/O Pins

Arria GX devices have six registers in the IOE, which support DDR interfacing by clocking data on both positive and negative clock edges. The IOEs in Arria GX devices support DDR inputs, DDR outputs, and bidirectional DDR modes. When using the IOE for DDR inputs, the two input registers clock double rate input data on alternating edges. An input latch is also used in the IOE for DDR input acquisition. The latch holds the data that is present during the clock high times, allowing both bits of data to be synchronous with the same clock edge (either rising or falling). Figure 2–73 shows an IOE configured for DDR input. Figure 2–74 shows the DDR input timing diagram.

On-Chip Series Termination (R_S OCT)

Arria GX devices support driver impedance matching to provide the I/O driver with controlled output impedance that closely matches the impedance of the transmission line. As a result, reflections can be significantly reduced. Arria GX devices support R_S OCT for single-ended I/O standards with typical R_S values of 25 and 50 Ω. Once matching impedance is selected, current drive strength is no longer selectable. Table 2–26 shows the list of output standards that support R_S OCT.

For more information about R_S OCT supported by Arria GX devices, refer to the *Selectable I/O Standards in Arria GX Devices* chapter.

For more information about tolerance specifications for OCT without calibration, refer to the *DC & Switching Characteristics* chapter.

MultiVolt I/O Interface

The Arria GX architecture supports the MultiVolt I/O interface feature that allows Arria GX devices in all packages to interface with systems of different supply voltages. Arria GX `VCCINT` pins must always be connected to a 1.2-V power supply. With a 1.2-V V_{CCINT} level, input pins are 1.2-, 1.5-, 1.8-, 2.5-, and 3.3-V tolerant. The `VCCIO` pins can be connected to either a 1.2-, 1.5-, 1.8-, 2.5-, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (for example, when `VCCIO` pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). Arria GX `VCCPD` power pins must be connected to a 3.3-V power supply. These power pins are used to supply the pre-driver power to the output buffers, which increases the performance of the output pins. The `VCCPD` pins also power configuration input pins and JTAG input pins.

Table 2–27 lists Arria GX MultiVolt I/O support.

Table 2–27. Arria GX MultiVolt I/O Support *(Note 1)*

V_{CCIO} (V)	Input Signal (V)					Output Signal (V)					
	1.2	1.5	1.8	2.5	3.3	1.2	1.5	1.8	2.5	3.3	5.0
1.2	*(4)*	✓ *(2)*	✓ *(2)*	✓ *(2)*	✓ *(2)*	✓ *(4)*	—	—	—	—	—
1.5	*(4)*	✓	✓	✓ *(2)*	✓ *(2)*	✓ *(3)*	✓	—	—	—	—
1.8	*(4)*	✓	✓	✓ *(2)*	✓ *(2)*	✓ *(3)*	✓ *(3)*	✓	—	—	—
2.5	*(4)*	—	—	✓	✓	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓	—	—
3.3	*(4)*	—	—	✓	✓	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓	✓

Notes to Table 2–27:

(1) To drive inputs higher than V_{CCIO} but less than 4.0 V, disable the PCI clamping diode and select the **Allow LVTTL and LVCMOS input levels to overdrive input buffer** option in the Quartus II software.

(2) The pin current may be slightly higher than the default value. You must verify that the driving device's V_{OL} maximum and V_{OH} minimum voltages do not violate the applicable Arria GX V_{IL} maximum and V_{IH} minimum voltage specifications.

(3) Although V_{CCIO} specifies the voltage necessary for the Arria GX device to drive out, a receiving device powered at a different level can still interface with the Arria GX device if it has inputs that tolerate the V_{CCIO} value.

(4) Arria GX devices support 1.2-V HSTL. They do not support 1.2-V LVTTL and 1.2-V LVCMOS.

Table 4–8 and Table 4–9 list the transmitter and receiver PCS latency for each mode, respectively.

Table 4–8. PCS Latency *(Note 1)*

Functional Mode	Configuration	Transmitter PCS Latency					
		TX PIPE	TX Phase Comp FIFO	Byte Serializer	TX State Machine	8B/10B Encoder	Sum *(2)*
XAUI	—	—	2–3	1	0.5	0.5	4–5
PIPE	×1, ×4, ×8 8-bit channel width	1	3–4	1	—	1	6–7
	×1, ×4, ×8 16-bit channel width	1	3–4	1	—	0.5	6–7
GIGE	—	—	2–3	1	—	1	4–5
Serial RapidIO	1.25 Gbps, 2.5 Gbps, 3.125 Gbps	—	2–3	1	—	0.5	4–5
SDI	HD10-bit channel width	—	2–3	1	—	1	4–5
	HD, 3G 20-bit channel width	—	2–3	1	—	0.5	4–5
BASIC Single Width	8-bit/10-bit channel width	—	2–3	1	—	1	4–5
	16-bit/20-bit channel width	—	2–3	1	—	0.5	4–5

Notes to Table 4–8:

(1) The latency numbers are with respect to the PLD-transceiver interface clock cycles.

(2) The total latency number is rounded off in the Sum column.

Table 4–9. PCS Latency (Part 1 of 2) (Part 1 of 2)

Functional Mode	Configuration	Receiver PCS Latency									
		Word Aligner	Deskew FIFO	Rate Matcher *(3)*	8B/10B Decoder	Receiver State Machine	Byte Deserializer	Byte Order	Receiver Phase Comp FIFO	Receiver PIPE	Sum *(2)*
XAUI	—	2–2.5	2–2.5	5.5–6.5	0.5	1	1	1	1–2	—	14–17
PIPE	×1, ×4 8-bit channel width	4–5	—	11–13	1	—	1	1	2–3	1	21–25
	×1, ×4 16-bit channel width	2–2.5	—	5.5–6.5	0.5	—	1	1	2–3	1	13–16
GIGE	—	4–5	—	11–13	1	—	1	1	1–2	—	19–23
Serial RapidIO	1.25 Gbps, 2.5 Gbps, 3.125 Gbps	2–2.5	—	—	0.5	—	1	1	1–2	—	6–7
SDI	HD 10-bit channel width	5	—	—	1	—	1	1	1–2	—	9–10
	HD, 3G 20-bit channel width	2.5	—	—	0.5	—	1	1	1–2	—	6–7

Table 4–14. Arria GX Device DC Operating Conditions (Part 2 of 2) *(Note 1)*

Symbol	Parameter	Conditions	Device	Min	Typ	Max	Units
R_{CONF} *(4)*	Value of I/O pin pull-up resistor before and during configuration	V_i = 0, V_{CCIO} = 3.3 V	—	10	25	50	kΩ
		V_i = 0, V_{CCIO} = 2.5 V	—	15	35	70	kΩ
		V_i = 0, V_{CCIO} = 1.8 V	—	30	50	100	kΩ
		V_i = 0, V_{CCIO} = 1.5 V	—	40	75	150	kΩ
		V_i = 0, V_{CCIO} = 1.2 V	—	50	90	170	kΩ
	Recommended value of I/O pin external pull-down resistor before and during configuration	—	—	—	1	2	kΩ

Notes to Table 4–14:

(1) Typical values are for T_A = 25 °C, V_{CCINT} = 1.2 V, and V_{CCIO} = 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

(2) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, 1.5, and 1.2 V).

(3) Maximum values depend on the actual TJ and design utilization. For maximum values, refer to the Excel-based PowerPlay Early Power Estimator (available at PowerPlay Early Power Estimators (EPE) and Power Analyzer) or the Quartus® II PowerPlay Power Analyzer feature for maximum values. For more information, refer to "Power Consumption" on page 4–25.

(4) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.

I/O Standard Specifications

Table 4–15 through Table 4–38 show the Arria GX device family I/O standard specifications.

Table 4–15. LVTTL Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO} *(1)*	Output supply voltage	—	3.135	3.465	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.3	0.8	V
V_{OH}	High-level output voltage	I_{OH} = –4 mA *(2)*	2.4	—	V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA *(2)*	—	0.45	V

Notes to Table 4–15:

(1) Arria GX devices comply to the narrow range for the supply voltage as specified in the EIA/JEDEC Standard, JESD8-B.

(2) This specification is supported across all the programmable drive strength settings available for this I/O standard.

Table 4–16. LVCMOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO} *(1)*	Output supply voltage	—	3.135	3.465	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.3	0.8	V
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, I_{OH} = –0.1 mA *(2)*	V_{CCIO} – 0.2	—	V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, I_{OL} = 0.1 mA *(2)*	—	0.2	V

Notes to Table 4–16:

(1) Arria GX devices comply to the narrow range for the supply voltage as specified in the EIA/JEDEC Standard, JESD8-B.

(2) This specification is supported across all the programmable drive strength available for this I/O standard.

Table 4–24. 3.3-V PCI Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	—	0.5 V_{CCIO}	—	V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage	—	–0.3	—	0.3 V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 V_{CCIO}	—	—	V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA	—	—	0.1 V_{CCIO}	V

Table 4–25. PCI-X Mode 1 Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage	—	3.0	3.6	V
V_{IH}	High-level input voltage	—	0.5 V_{CCIO}	V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 V_{CCIO}	V
V_{IPU}	Input pull-up voltage	—	0.7 V_{CCIO}	—	V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 V_{CCIO}	—	V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA	—	0.1 V_{CCIO}	V

Table 4–26. SSTL-18 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	1.71	1.8	1.89	V
V_{REF}	Reference voltage	—	0.855	0.9	0.945	V
V_{TT}	Termination voltage	—	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{IH} (DC)	High-level DC input voltage	—	V_{REF} + 0.125	—	—	V
V_{IL} (DC)	Low-level DC input voltage	—	—	—	V_{REF} – 0.125	V
V_{IH} (AC)	High-level AC input voltage	—	V_{REF} + 0.25	—	—	V
V_{IL} (AC)	Low-level AC input voltage	—	—	—	V_{REF} – 0.25	V
V_{OH}	High-level output voltage	I_{OH} = –6.7 mA *(1)*	V_{TT} + 0.475	—	—	V
V_{OL}	Low-level output voltage	I_{OL} = 6.7 mA *(1)*	—	—	V_{TT} – 0.475	V

Note to Table 4–26:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Arria GX Architecture* chapter.

Table 4–27. SSTL-18 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	1.71	1.8	1.89	V
V_{REF}	Reference voltage	—	0.855	0.9	0.945	V
V_{TT}	Termination voltage	—	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{IH} (DC)	High-level DC input voltage	—	V_{REF} + 0.125	—	—	V
V_{IL} (DC)	Low-level DC input voltage	—	—	—	V_{REF} – 0.125	V
V_{IH} (AC)	High-level AC input voltage	—	V_{REF} + 0.25	—	—	V
V_{IL} (AC)	Low-level AC input voltage	—	—	—	V_{REF} – 0.25	V

Table 4–51. EP1AGX20 Column Pins Output Timing Parameters (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
1.8 V	6 mA	GCLK	t_{CO}	2.695	2.695	6.155	ns
		GCLK PLL	t_{CO}	1.253	1.253	3.049	ns
1.8 V	8 mA	GCLK	t_{CO}	2.697	2.697	6.064	ns
		GCLK PLL	t_{CO}	1.255	1.255	2.958	ns
1.8 V	10 mA	GCLK	t_{CO}	2.651	2.651	5.987	ns
		GCLK PLL	t_{CO}	1.209	1.209	2.881	ns
1.8 V	12 mA	GCLK	t_{CO}	2.652	2.652	5.930	ns
		GCLK PLL	t_{CO}	1.210	1.210	2.824	ns
1.5 V	2 mA	GCLK	t_{CO}	2.746	2.746	6.723	ns
		GCLK PLL	t_{CO}	1.304	1.304	3.617	ns
1.5 V	4 mA	GCLK	t_{CO}	2.682	2.682	6.154	ns
		GCLK PLL	t_{CO}	1.240	1.240	3.048	ns
1.5 V	6 mA	GCLK	t_{CO}	2.685	2.685	6.036	ns
		GCLK PLL	t_{CO}	1.243	1.243	2.930	ns
1.5 V	8 mA	GCLK	t_{CO}	2.644	2.644	5.983	ns
		GCLK PLL	t_{CO}	1.202	1.202	2.877	ns
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.629	2.629	5.762	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.650	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.612	2.612	5.712	ns
		GCLK PLL	t_{CO}	1.167	1.167	2.600	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.590	2.590	5.639	ns
		GCLK PLL	t_{CO}	1.145	1.145	2.527	ns
SSTL-2 CLASS II	20 mA	GCLK	t_{CO}	2.591	2.591	5.626	ns
		GCLK PLL	t_{CO}	1.146	1.146	2.514	ns
SSTL-2 CLASS II	24 mA	GCLK	t_{CO}	2.587	2.587	5.624	ns
		GCLK PLL	t_{CO}	1.142	1.142	2.512	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.626	2.626	5.733	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.627	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.630	2.630	5.694	ns
		GCLK PLL	t_{CO}	1.185	1.185	2.582	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.609	2.609	5.675	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.563	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.614	2.614	5.673	ns
		GCLK PLL	t_{CO}	1.169	1.169	2.561	ns
SSTL-18 CLASS I	12 mA	GCLK	t_{CO}	2.608	2.608	5.659	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.547	ns
SSTL-18 CLASS II	8 mA	GCLK	t_{CO}	2.597	2.597	5.625	ns
		GCLK PLL	t_{CO}	1.152	1.152	2.513	ns

Table 4–51. EP1AGX20 Column Pins Output Timing Parameters (Part 3 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
SSTL-18 CLASS II	16 mA	GCLK	t_{CO}	2.609	2.609	5.603	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.491	ns
SSTL-18 CLASS II	18 mA	GCLK	t_{CO}	2.605	2.605	5.611	ns
		GCLK PLL	t_{CO}	1.160	1.160	2.499	ns
SSTL-18 CLASS II	20 mA	GCLK	t_{CO}	2.605	2.605	5.609	ns
		GCLK PLL	t_{CO}	1.160	1.160	2.497	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.629	2.629	5.664	ns
		GCLK PLL	t_{CO}	1.187	1.187	2.558	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.634	2.634	5.649	ns
		GCLK PLL	t_{CO}	1.189	1.189	2.537	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.612	2.612	5.638	ns
		GCLK PLL	t_{CO}	1.167	1.167	2.526	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.616	2.616	5.644	ns
		GCLK PLL	t_{CO}	1.171	1.171	2.532	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.608	2.608	5.637	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.525	ns
1.8-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.591	2.591	5.401	ns
		GCLK PLL	t_{CO}	1.146	1.146	2.289	ns
1.8-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.593	2.593	5.412	ns
		GCLK PLL	t_{CO}	1.148	1.148	2.300	ns
1.8-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.593	2.593	5.421	ns
		GCLK PLL	t_{CO}	1.148	1.148	2.309	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.629	2.629	5.663	ns
		GCLK PLL	t_{CO}	1.187	1.187	2.557	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.633	2.633	5.641	ns
		GCLK PLL	t_{CO}	1.188	1.188	2.529	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.615	2.615	5.643	ns
		GCLK PLL	t_{CO}	1.170	1.170	2.531	ns
1.5-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.615	2.615	5.645	ns
		GCLK PLL	t_{CO}	1.170	1.170	2.533	ns
1.5-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.609	2.609	5.643	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.531	ns
1.5-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.596	2.596	5.455	ns
		GCLK PLL	t_{CO}	1.151	1.151	2.343	ns
1.5-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.599	2.599	5.465	ns
		GCLK PLL	t_{CO}	1.154	1.154	2.353	ns
1.5-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.601	2.601	5.478	ns
		GCLK PLL	t_{CO}	1.156	1.156	2.366	ns

Table 4–61 lists I/O timing specifications.

Table 4–61. EP1AGX50 Column Pins Input Timing Parameters (Part 1 of 2)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.242	1.242	2.902	ns
		t_H	–1.137	–1.137	–2.625	ns
	GCLK PLL	t_{SU}	2.684	2.684	6.009	ns
		t_H	–2.579	–2.579	–5.732	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.242	1.242	2.902	ns
		t_H	–1.137	–1.137	–2.625	ns
	GCLK PLL	t_{SU}	2.684	2.684	6.009	ns
		t_H	–2.579	–2.579	–5.732	ns
2.5 V	GCLK	t_{SU}	1.252	1.252	2.884	ns
		t_H	–1.147	–1.147	–2.607	ns
	GCLK PLL	t_{SU}	2.694	2.694	5.991	ns
		t_H	–2.589	–2.589	–5.714	ns
1.8 V	GCLK	t_{SU}	1.318	1.318	3.094	ns
		t_H	–1.213	–1.213	–2.817	ns
	GCLK PLL	t_{SU}	2.760	2.760	6.201	ns
		t_H	–2.655	–2.655	–5.924	ns
1.5 V	GCLK	t_{SU}	1.321	1.321	3.187	ns
		t_H	–1.216	–1.216	–2.910	ns
	GCLK PLL	t_{SU}	2.763	2.763	6.294	ns
		t_H	–2.658	–2.658	–6.017	ns
SSTL-2 CLASS I	GCLK	t_{SU}	1.034	1.034	2.314	ns
		t_H	–0.929	–0.929	–2.037	ns
	GCLK PLL	t_{SU}	2.500	2.500	5.457	ns
		t_H	–2.395	–2.395	–5.180	ns
SSTL-2 CLASS II	GCLK	t_{SU}	1.034	1.034	2.314	ns
		t_H	–0.929	–0.929	–2.037	ns
	GCLK PLL	t_{SU}	2.500	2.500	5.457	ns
		t_H	–2.395	–2.395	–5.180	ns
SSTL-18 CLASS I	GCLK	t_{SU}	1.104	1.104	2.466	ns
		t_H	–0.999	–0.999	–2.189	ns
	GCLK PLL	t_{SU}	2.546	2.546	5.573	ns
		t_H	–2.441	–2.441	–5.296	ns
SSTL-18 CLASS II	GCLK	t_{SU}	1.074	1.074	2.424	ns
		t_H	–0.969	–0.969	–2.147	ns
	GCLK PLL	t_{SU}	2.539	2.539	5.564	ns
		t_H	–2.434	–2.434	–5.287	ns

Table 4–64 lists row pin delay adders when using the regional clock in Arria GX devices.

Table 4–64. EP1AGX50 Row Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
`RCLK` input adder	0.151	0.151	0.329	ns
`RCLK` PLL input adder	0.011	0.011	0.016	ns
`RCLK` output adder	–0.151	–0.151	–0.329	ns
`RCLK` PLL output adder	–0.011	–0.011	–0.016	ns

Table 4–65 lists column pin delay adders when using the regional clock in Arria GX devices.

Table 4–65. EP1AGX50 Column Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
`RCLK` input adder	0.146	0.146	0.334	ns
`RCLK` PLL input adder	–1.713	–1.713	–3.645	ns
`RCLK` output adder	–0.146	–0.146	–0.336	ns
`RCLK` PLL output adder	1.716	1.716	4.488	ns

EP1AGX60 I/O Timing Parameters

Table 4–66 through Table 4–69 list the maximum I/O timing parameters for EP1AGX60 devices for I/O standards which support general purpose I/O pins.

Table 4–66 lists I/O timing specifications.

Table 4–66. EP1AGX60 Row Pins Input Timing Parameters (Part 1 of 3)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	`GCLK`	t_{SU}	1.413	1.413	3.113	ns
		t_H	–1.308	–1.308	–2.836	ns
	`GCLK PLL`	t_{SU}	2.975	2.975	6.536	ns
		t_H	–2.870	–2.870	–6.259	ns
3.3-V LVCMOS	`GCLK`	t_{SU}	1.413	1.413	3.113	ns
		t_H	–1.308	–1.308	–2.836	ns
	`GCLK PLL`	t_{SU}	2.975	2.975	6.536	ns
		t_H	–2.870	–2.870	–6.259	ns
2.5 V	`GCLK`	t_{SU}	1.425	1.425	3.094	ns
		t_H	–1.320	–1.320	–2.817	ns
	`GCLK PLL`	t_{SU}	2.987	2.987	6.517	ns
		t_H	–2.882	–2.882	–6.240	ns

Table 4–77 lists column pin delay adders when using the regional clock in Arria GX devices.

Table 4–77. EP1AGX90 Column Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
`RCLK` input adder	0.138	0.138	0.354	ns
`RCLK` PLL input adder	–1.697	–1.697	–3.607	ns
`RCLK` output adder	–0.138	–0.138	–0.353	ns
`RCLK` PLL output adder	1.966	1.966	5.188	ns

Dedicated Clock Pin Timing

Table 4–79 through Table 4–98 list clock pin timing for Arria GX devices when the clock is driven by the global clock, regional clock, periphery clock, and a PLL.

Table 4–78 lists Arria GX clock timing parameters.

Table 4–78. Arria GX Clock Timing Parameters

Symbol	Parameter
t_{CIN}	Delay from clock pad to I/O input register
t_{COUT}	Delay from clock pad to I/O output register
t_{PLLCIN}	Delay from PLL `inclk` pad to I/O input register
$t_{PLLCOUT}$	Delay from PLL `inclk` pad to I/O output register

EP1AGX20 Clock Timing Parameters

Table 4–79 through Table 4–80 list the `GCLK` clock timing parameters for EP1AGX20 devices.

Table 4–79 lists clock timing specifications.

Table 4–79. EP1AGX20 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
`tcin`	1.394	1.394	3.161	ns
`tcout`	1.399	1.399	3.155	ns
`tpllcin`	–0.027	–0.027	0.091	ns
`tpllcout`	–0.022	–0.022	0.085	ns

Table 4–106. Arria GX Maximum Output Toggle Rate for Row I/O Pins

I/O Standards	Drive Strength	–6 Speed Grade	Units
1.8-V HSTL CLASS I	4 mA	280	MHz
	6 mA	420	MHz
	8 mA	561	MHz
	10 mA	561	MHz
	12 mA	607	MHz
1.5-V HSTL CLASS I	4 mA	280	MHz
	6 mA	420	MHz
	8 mA	561	MHz
LVDS	—	598	MHz

Table 4–107 lists maximum output clock rate for dedicated clock pins.

Table 4–107. Arria GX Maximum Output Clock Rate for Dedicated Clock Pins (Part 1 of 4)

I/O Standards	Drive Strength	–6 Speed Grade	Units
3.3-V LVTTL	4 mA	196	MHz
	8 mA	303	MHz
	12 mA	393	MHz
	16 mA	486	MHz
	20 mA	570	MHz
	24 mA	626	MHz
3.3-V LVCMOS	4 mA	215	MHz
	8 mA	411	MHz
	12 mA	626	MHz
	16 mA	819	MHz
	20 mA	874	MHz
	24 mA	934	MHz
2.5 V	4 mA	168	MHz
	8 mA	355	MHz
	12 mA	514	MHz
	16 mA	766	MHz
1.8 V	2 mA	97	MHz
	4 mA	215	MHz
	6 mA	336	MHz
	8 mA	486	MHz
	10 mA	706	MHz
	12 mA	925	MHz
1.5 V	2 mA	168	MHz
	4 mA	303	MHz
	6 mA	350	MHz
	8 mA	392	MHz

Table 4–116. Enhanced PLL Specifications (Part 2 of 2)

Name	Description	Min	Typ	Max	Units
$t_{RECONFIGWAIT}$	The time required for the wait after the reconfiguration is done and the areset is applied.	—	—	2	us

Notes to Table 4–116:

(1) This is limited by the I/O f_{MAX}.

(2) If the counter cascading feature of the PLL is used, there is no minimum output clock frequency.

Table 4–117. Fast PLL Specifications (Part 1 of 2)

Name	Description	Min	Typ	Max	Units
f_{IN}	Input clock frequency	16.08	—	640	MHz
f_{INPFD}	Input frequency to the PFD	16.08	—	500	MHz
f_{INDUTY}	Input clock duty cycle	40	—	60	%
$t_{INJITTER}$	Input clock jitter tolerance in terms of period jitter. Bandwidth ≤ 2 MHz	—	0.5	—	ns (p-p)
	Input clock jitter tolerance in terms of period jitter. Bandwidth > 0.2 MHz	—	1.0	—	ns (p-p)
f_{VCO}	Upper VCO frequency range	300	—	840	MHz
	Lower VCO frequency range	150	—	420	MHz
f_{OUT}	PLL output frequency to `GCLK` or `RCLK`	4.6875	—	550	MHz
	PLL output frequency to LVDS or DPA clock	150	—	840	MHz
f_{OUT_EXT}	PLL clock output frequency to regular I/O	4.6875	—	*(1)*	MHz
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for fast PLLs	—	$75/f_{SCANCLK}$	—	ns
f_{CLBW}	PLL closed-loop bandwidth	1.16	5	28	MHz
t_{LOCK}	Time required for the PLL to lock from the time it is enabled or the end of the device configuration	—	0.03	1	ms
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±30	ps
t_{ARESET}	Minimum pulse width on `areset` signal.	10	—	—	ns

Visual Cue	Meaning
`Courier type`	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. Active-low signals are denoted by suffix `n`. For example, `resetn`. Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).
1., 2., 3., and a., b., c., and so on.	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■	Bullets indicate a list of items when the sequence of the items is not important.
☞	The hand points to information that requires special attention.
⚠ CAUTION	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
↵	The angled arrow instructs you to press **Enter**.
	The feet direct you to more information about a particular topic.