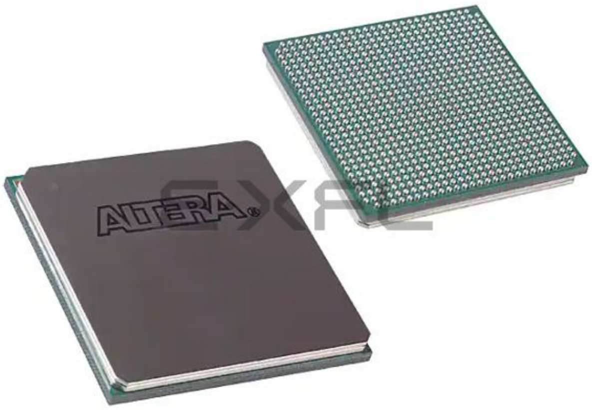

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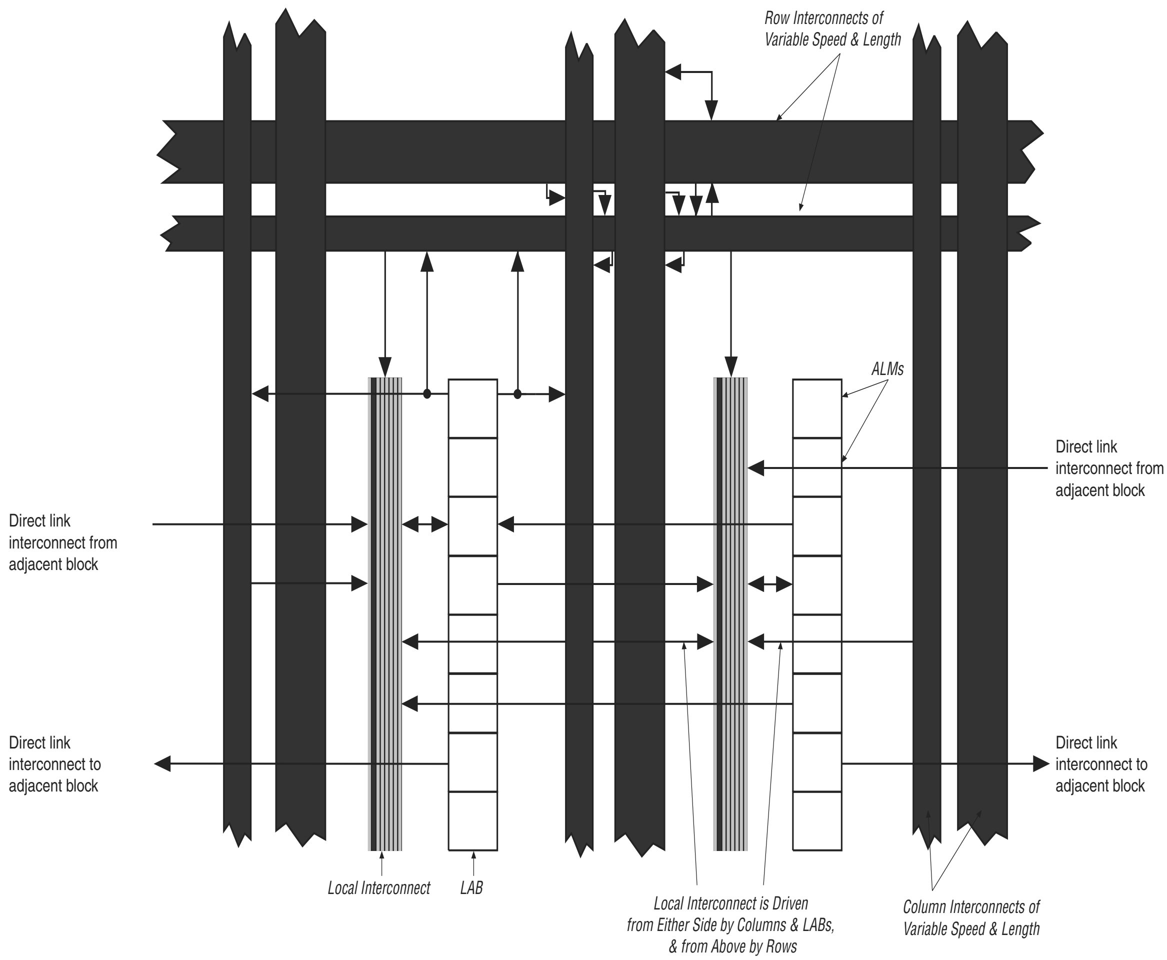
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3005
Number of Logic Elements/Cells	60100
Total RAM Bits	2528640
Number of I/O	350
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	780-BBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1agx60df780i6n

Figure 2–25. Arria GX LAB Structure



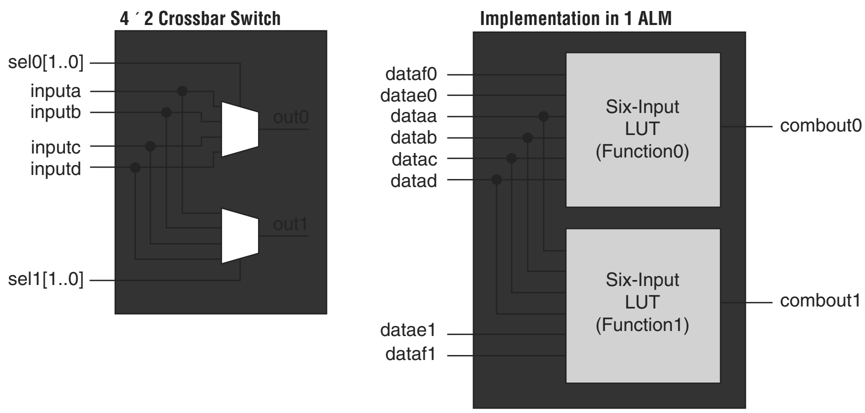
LAB Interconnects

The LAB local interconnect can drive all eight ALMs in the same LAB. It is driven by column and row interconnects and ALM outputs in the same LAB. Neighboring LABs, M512 RAM blocks, M4K RAM blocks, M-RAM blocks, or digital signal processing (DSP) blocks from the left and right can also drive the local interconnect of a LAB through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each ALM can drive 24 ALMs through fast local and direct link interconnects.

To pack two five-input functions into one ALM, the functions must have at least two common inputs. The common inputs are `dataa` and `datab`. The combination of a four-input function with a five-input function requires one common input (either `dataa` or `datab`).

To implement two six-input functions in one ALM, four inputs must be shared and the combinational function must be the same. For example, a 4 × 2 crossbar switch (two 4-to-1 multiplexers with common inputs and unique select lines) can be implemented in one ALM, as shown in Figure 2–31. The shared inputs are `dataa`, `datab`, `datac`, and `datad`, while the unique select lines are `datae0` and `dataf0` for `function0`, and `datae1` and `dataf1` for `function1`. This crossbar switch consumes four LUTs in a four-input LUT-based architecture.

Figure 2–31. 4 × 2 Crossbar Switch Example



In a sparsely used device, functions that can be placed into one ALM can be implemented in separate ALMs. The Quartus II Compiler spreads a design out to achieve the best possible performance. As a device begins to fill up, the Quartus II software automatically uses the full potential of the Arria GX ALM. The Quartus II Compiler automatically searches for functions of common inputs or completely independent functions to be placed into one ALM and to make efficient use of the device resources. In addition, you can manually control resource usage by setting location assignments. Any six-input function can be implemented utilizing inputs `dataa`, `datab`, `datac`, `datad`, and either `datae0` and `dataf0` or `datae1` and `dataf1`. If `datae0` and `dataf0` are used, the output is driven to `register0`, and/or `register0` is bypassed and the data drives out to the interconnect using the top set of output drivers (refer to Figure 2–32). If `datae1` and `dataf1` are used, the output drives to `register1` and/or bypasses `register1` and drives to the interconnect using the bottom set of output drivers. The Quartus II Compiler automatically selects the inputs to the LUT. Asynchronous load data for the register comes from the `datae` or `dataf` input of the ALM. ALMs in normal mode support register packing.

Figure 2–49. M-RAM Row Unit Interface to Interconnect

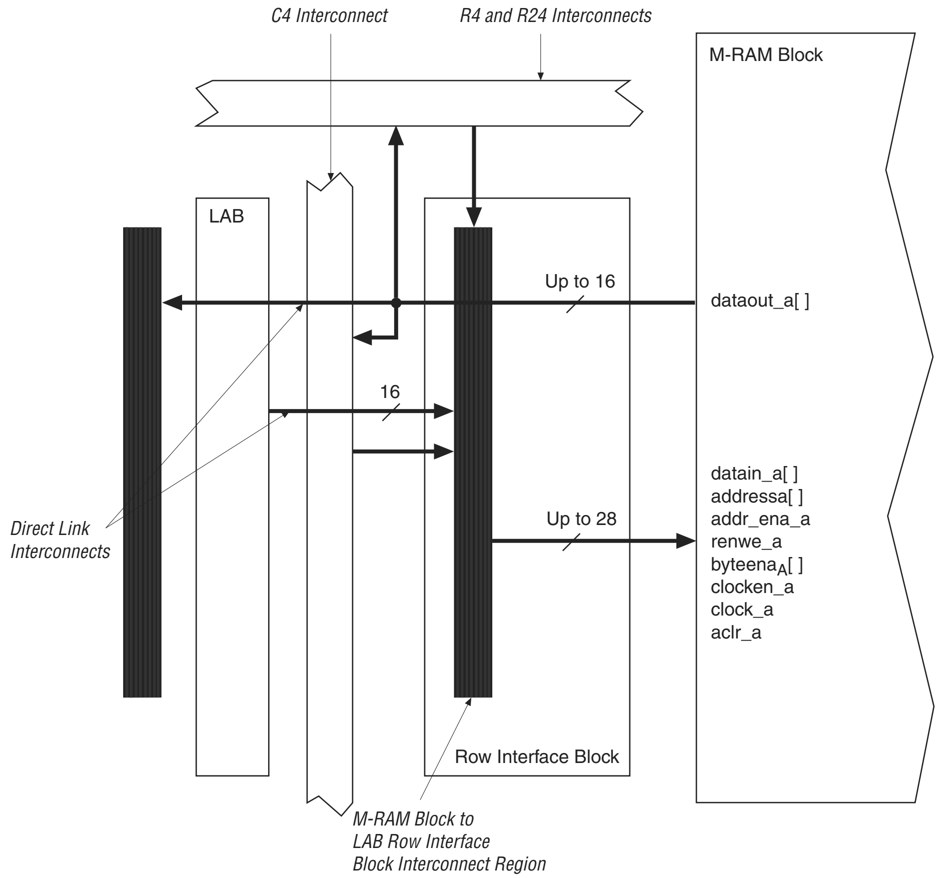


Table 2–12 lists the input and output data signal connections along with the address and control signal input connections to the row unit interfaces (L0 to L5 and R0 to R5).

Table 2–12. M-RAM Row Interface Unit Signals (Part 1 of 2)

Unit Interface Block	Input Signals	Output Signals
L0	`datain_a[14..0]` `byteena_a[1..0]`	`dataout_a[11..0]`
L1	`datain_a[29..15]` `byteena_a[3..2]`	`dataout_a[23..12]`

L2	`datain_a[35..30]`
	`addressa[4..0]`
	`addr_ena_a`
	`clock_a`
	`clocken_a`
	`renwe_a`
	`aclr_a`
		`dataout_a[35..24]`

L3	`addressa[15..5]` `datain_a[41..36]`	`dataout_a[47..36]`

Table 2–12. M-RAM Row Interface Unit Signals (Part 2 of 2)

Unit Interface Block	Input Signals	Output Signals
L4	datain_a[56..42] byteena_a[5..4]	dataout_a[59..48]
L5	datain_a[71..57] byteena_a[7..6]	dataout_a[71..60]
R0	datain_b[14..0] byteena_b[1..0]	dataout_b[11..0]
R1	datain_b[29..15] byteena_b[3..2]	dataout_b[23..12]
R2	datain_b[35..30] addressb[4..0] addr_ena_b clock_b clocken_b renwe_b aclr_b	dataout_b[35..24]
R3	addressb[15..5] datain_b[41..36]	dataout_b[47..36]
R4	datain_b[56..42] byteena_b[5..4]	dataout_b[59..48]
R5	datain_b[71..57] byteena_b[7..6]	dataout_b[71..60]

For more information about TriMatrix memory, refer to the *TriMatrix Embedded Memory Blocks in Arria GX Devices* chapter.

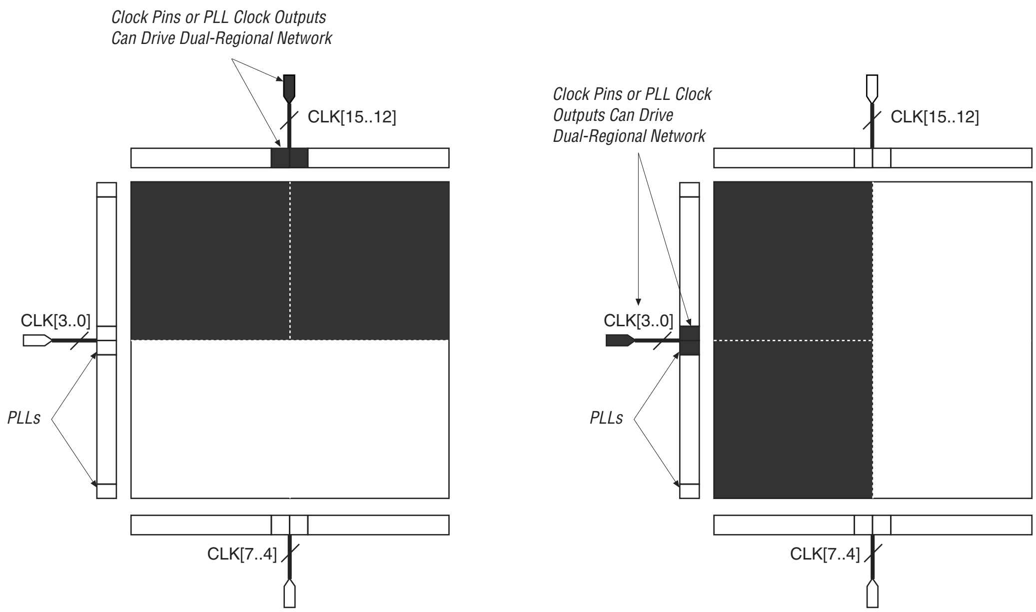
Digital Signal Processing Block

The most commonly used DSP functions are finite impulse response (FIR) filters, complex FIR filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, direct cosine transform (DCT) functions, and correlators. All of these use the multiplier as the fundamental building block. Additionally, some applications need specialized operations such as multiply-add and multiply-accumulate operations. Arria GX devices provide DSP blocks to meet the arithmetic requirements of these functions.

Each Arria GX device has two to four columns of DSP blocks to efficiently implement DSP functions faster than ALM-based implementations. Each DSP block can be configured to support up to:

- Eight 9 × 9-bit multipliers
- Four 18 × 18-bit multipliers
- One 36 × 36-bit multiplier

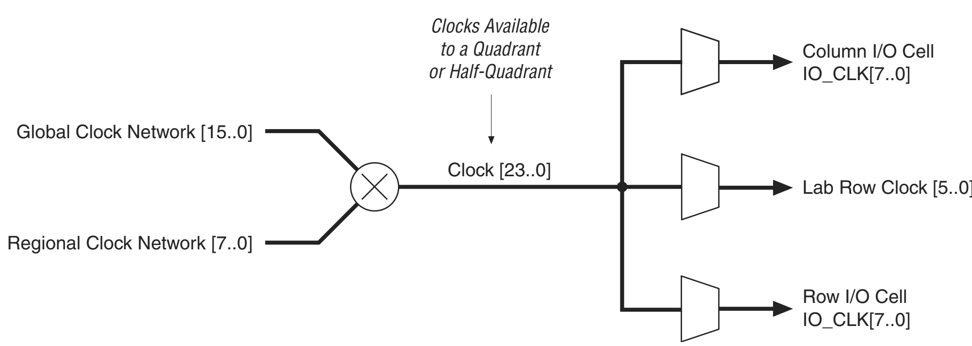
Figure 2–56. Dual-Regional Clocks



Combined Resources

Within each quadrant, there are 24 distinct dedicated clocking resources consisting of 16 global clock lines and eight regional clock lines. Multiplexers are used with these clocks to form buses to drive LAB row clocks, column IOE clocks, or row IOE clocks. Another multiplexer is used at the LAB level to select three of the six row clocks to feed the ALM registers in the LAB (refer to Figure 2–57).

Figure 2–57. Hierarchical Clock Networks Per Quadrant



You can use the Quartus II software to control whether a clock input pin drives either a GCLK, RCLK, or dual-RCLK network. The Quartus II software automatically selects the clocking resources if not specified.

Table 2–20. Global and Regional Clock Connections from Top Clock Pins and Enhanced PLL Outputs

Top Side Global and Regional Clock Network Connectivity	DLLCLK	CLK12	CLK13	CLK14	CLK15	RCLK24	RCLK25	RCLK26	RCLK27	RCLK28	RCLK29	RCLK30	RCLK31
Clock pins													
CLK12p	✓	✓	✓	—	—	✓	—	—	—	✓	—	—	—
CLK13p	✓	✓	✓	—	—	—	✓	—	—	—	✓	—	—
CLK14p	✓	—	—	✓	✓	—	—	✓	—	—	—	✓	—
CLK15p	✓	—	—	✓	✓	—	—	—	✓	—	—	—	✓
CLK12n	—	✓	—	—	—	✓	—	—	—	✓	—	—	—
CLK13n	—	—	✓	—	—	—	✓	—	—	—	✓	—	—
CLK14n	—	—	—	✓	—	—	—	✓	—	—	—	✓	—
CLK15n	—	—	—	—	✓	—	—	—	✓	—	—	—	✓
Drivers from internal logic													
GCLKDRV0	—	✓	—	—	—	—	—	—	—	—	—	—	—
GCLKDRV1	—	—	✓	—	—	—	—	—	—	—	—	—	—
GCLKDRV2	—	—	—	✓	—	—	—	—	—	—	—	—	—
GCLKDRV3	—	—	—	—	✓	—	—	—	—	—	—	—	—
RCLKDRV0	—	—	—	—	—	✓	—	—	—	✓	—	—	—
RCLKDRV1	—	—	—	—	—	—	✓	—	—	—	✓	—	—
RCLKDRV2	—	—	—	—	—	—	—	✓	—	—	—	✓	—
RCLKDRV3	—	—	—	—	—	—	—	—	✓	—	—	—	✓
RCLKDRV4	—	—	—	—	—	✓	—	—	—	✓	—	—	—
RCLKDRV5	—	—	—	—	—	—	✓	—	—	—	✓	—	—
RCLKDRV6	—	—	—	—	—	—	—	✓	—	—	—	✓	—
RCLKDRV7	—	—	—	—	—	—	—	—	✓	—	—	—	✓
Enhanced PLL5 outputs													
c0	✓	✓	✓	—	—	✓	—	—	—	✓	—	—	—
c1	✓	✓	✓	—	—	—	✓	—	—	—	✓	—	—
c2	✓	—	—	✓	✓	—	—	✓	—	—	—	✓	—
c3	✓	—	—	✓	✓	—	—	—	✓	—	—	—	✓
c4	✓	—	—	—	—	✓	—	✓	—	✓	—	✓	—
c5	✓	—	—	—	—	—	✓	—	✓	—	✓	—	✓
Enhanced PLL 11 outputs													
c0	—	✓	✓	—	—	✓	—	—	—	✓	—	—	—
c1	—	✓	✓	—	—	—	✓	—	—	—	✓	—	—
c2	—	—	—	✓	✓	—	—	✓	—	—	—	✓	—
c3	—	—	—	✓	✓	—	—	—	✓	—	—	—	✓
c4	—	—	—	—	—	✓	—	✓	—	✓	—	✓	—
c5	—	—	—	—	—	—	✓	—	✓	—	✓	—	✓

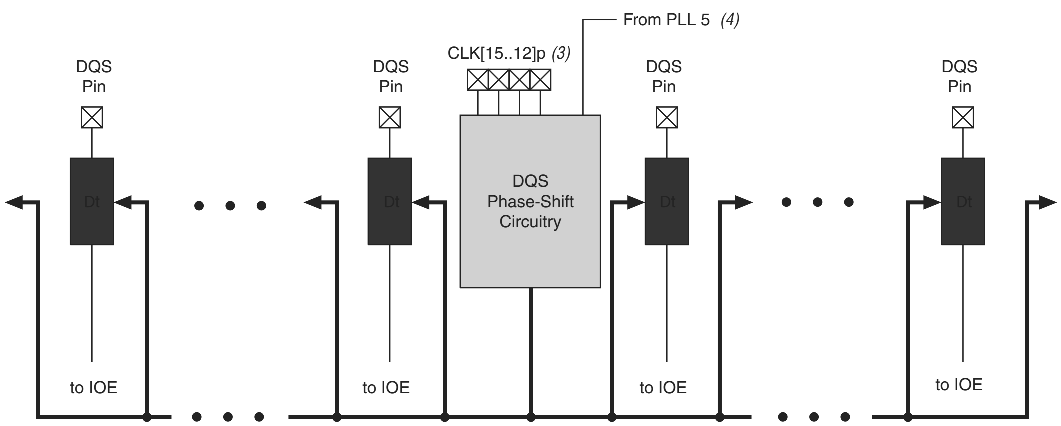
Table 2–21. Global and Regional Clock Connections from Bottom Clock Pins and Enhanced PLL Outputs

Bottom Side Global and Regional Clock Network Connectivity	DLLCLK	CLK4	CLK5	CLK6	CLK7	RCLK8	RCLK9	RCLK10	RCLK11	RCLK12	RCLK13	RCLK14	RCLK15
Clock pins													
CLK4p	✓	✓	✓	—	—	✓	—	—	—	✓	—	—	—
CLK5p	✓	✓	✓	—	—	—	✓	—	—	—	✓	—	—
CLK6p	✓	—	—	✓	✓	—	—	✓	—	—	—	✓	—
CLK7p	✓	—	—	✓	✓	—	—	—	✓	—	—	—	✓
CLK4n	—	✓	—	—	—	✓	—	—	—	✓	—	—	—
CLK5n	—	—	✓	—	—	—	✓	—	—	—	✓	—	—
CLK6n	—	—	—	✓	—	—	—	✓	—	—	—	✓	—
CLK7n	—	—	—	—	✓	—	—	—	✓	—	—	—	✓
Drivers from internal logic													
GCLKDRV0	—	✓	—	—	—	—	—	—	—	—	—	—	—
GCLKDRV1	—	—	✓	—	—	—	—	—	—	—	—	—	—
GCLKDRV2	—	—	—	✓	—	—	—	—	—	—	—	—	—
GCLKDRV3	—	—	—	—	✓	—	—	—	—	—	—	—	—
RCLKDRV0	—	—	—	—	—	✓	—	—	—	✓	—	—	—
RCLKDRV1	—	—	—	—	—	—	✓	—	—	—	✓	—	—
RCLKDRV2	—	—	—	—	—	—	—	✓	—	—	—	✓	—
RCLKDRV3	—	—	—	—	—	—	—	—	✓	—	—	—	✓
RCLKDRV4	—	—	—	—	—	✓	—	—	—	✓	—	—	—
RCLKDRV5	—	—	—	—	—	—	✓	—	—	—	✓	—	—
RCLKDRV6	—	—	—	—	—	—	—	✓	—	—	—	✓	—
RCLKDRV7	—	—	—	—	—	—	—	—	✓	—	—	—	✓
Enhanced PLL 6 outputs													
c0	✓	✓	✓	—	—	✓	—	—	—	✓	—	—	—
c1	✓	✓	✓	—	—	—	✓	—	—	—	✓	—	—
c2	✓	—	—	✓	✓	—	—	✓	—	—		✓	
c3	✓	—	—	✓	✓	—	—	—	✓	—	—	—	✓
c4	✓	—	—	—	—	✓	—	✓	—	✓	—	✓	—
c5	✓	—	—	—	—	—	✓	—	✓	—	✓	—	✓
Enhanced PLL 12 outputs													
c0	—	✓	✓	—	—	✓	—	—	—	✓	—	—	—
c1	—	✓	✓	—	—	—	✓	—	—	—	✓	—	—
c2	—	—	—	✓	✓	—	—	✓	—	—	—	✓	—
c3	—	—	—	✓	✓	—	—	—	✓	—	—	—	✓
c4	—	—	—	—	—	✓	—	✓	—	✓	—	✓	—
c5	—	—	—	—	—	—	✓	—	✓	—	✓	—	✓

The Arria GX device has two phase-shifting reference circuits, one on the top and one on the bottom of the device. The circuit on the top controls the compensated delay elements for all DQS pins on the top. The circuit on the bottom controls the compensated delay elements for all DQS pins on the bottom.

Each phase-shifting reference circuit is driven by a system reference clock, which must have the same frequency as the DQS signal. Clock pins `CLK[15..12]p` feed phase circuitry on the top of the device and clock pins `CLK[7..4]p` feed phase circuitry on the bottom of the device. In addition, PLL clock outputs can also feed the phase-shifting reference circuits. Figure 2–77 shows the phase-shift reference circuit control of each DQS delay shift on the top of the device. This same circuit is duplicated on the bottom of the device.

Figure 2–77. DQS Phase-Shift Circuitry *(Note 1)*, *(2)*



Notes to Figure 2–77:

(1) There are up to 18 pairs of DQS pins available on the top or bottom of the Arria GX device. There are up to 10 pairs on the right side and 8 pairs on the left side of the DQS phase-shift circuitry.

(2) The “t” module represents the DQS logic block.

(3) Clock pins `CLK[15..12]p` feed phase-shift circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase circuitry on the bottom of the device. You can also use a PLL clock output as a reference clock to phase shift circuitry.

(4) You can only use PLL 5 to feed the DQS phase-shift circuitry on the top of the device and PLL 6 to feed the DQS phase-shift circuitry on the bottom of the device.

These dedicated circuits combined with enhanced PLL clocking and phase-shift ability provide a complete hardware solution for interfacing to high-speed memory.

For more information about external memory interfaces, refer to the *External Memory Interfaces in Arria GX Devices* chapter.

Programmable Drive Strength

The output buffer for each Arria GX device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL, LVCMOS, SSTL, and HSTL standards have several levels of drive strength that you can control. The default setting used in the Quartus II software is the maximum current strength setting that is used to achieve maximum I/O performance. For all I/O standards, the minimum setting is the lowest drive strength that guarantees the I_{OH}/I_{OL} of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot.

Table 2–34. EP1AGX90 Device Differential Channels *(Note 1)*

Package	Transmitter/Receiver	Total Channels	Center Fast PLLs		Corner Fast PLLs
			PLL1	PLL2	PLL7
1,152-pin FineLine BGA	Transmitter	45	23	22	23
			22	23	—
	Receiver	47	23	24	23
			24	23	—

Note to Table 2–34:

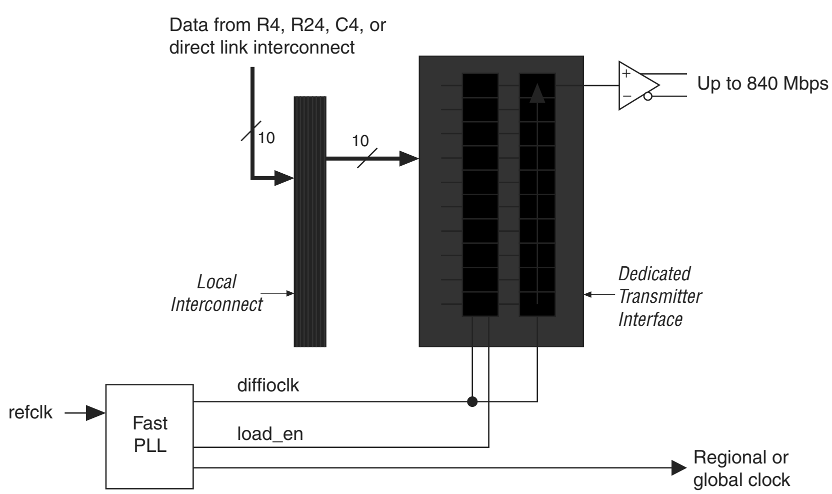
(1) The total number of receiver channels includes the four non-dedicated clock channels that can be optionally used as data channels.

Dedicated Circuitry with DPA Support

Arria GX devices support source-synchronous interfacing with LVDS signaling at up to 840 Mbps. Arria GX devices can transmit or receive serial channels along with a low-speed or high-speed clock.

The receiving device PLL multiplies the clock by an integer factor W = 1 through 32. The SERDES factor J determines the parallel data width to deserialize from receivers or to serialize for transmitters. The SERDES factor J can be set to 4, 5, 6, 7, 8, 9, or 10 and does not have to equal the PLL clock-multiplication W value. A design using the dynamic phase aligner also supports all of these J factor values. For a J factor of 1, the Arria GX device bypasses the SERDES block. For a J factor of 2, the Arria GX device bypasses the SERDES block, and the DDR input and output registers are used in the IOE. Figure 2–79 shows the block diagram of the Arria GX transmitter channel.

Figure 2–79. Arria GX Transmitter Channel



Each Arria GX receiver channel features a DPA block for phase detection and selection, a SERDES, a synchronizer, and a data realigner circuit. You can bypass the dynamic phase aligner without affecting the basic source-synchronous operation of the channel. In addition, you can dynamically switch between using the DPA block or bypassing the block via a control signal from the logic array.

Table 3–1. Arria GX JTAG Instructions

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer.
EXTEST *(1)*	00 0000 1111	Allows external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing IDCODE to be serially shifted out of TDO.
HIGHZ *(1)*	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP *(1)*	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions	—	Used when configuring an Arria GX device via the JTAG port with a USB-Blaster™, MasterBlaster™, ByteBlasterMV™, EthernetBlaster™, or ByteBlaster II download cable, or when using a **.jam** or **.jbc** via an embedded processor or JRunner™.
PULSE_NCONFIG	00 0000 0001	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.
CONFIG_IO *(2)*	00 0000 1101	Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, during, or after configuration. Stops configuration if executed during configuration. Once issued, the CONFIG_IO instruction holds nSTATUS low to reset the configuration device. nSTATUS is held low until the IOE configuration register is loaded and the TAP controller state machine transitions to the UPDATE_DR state.

Notes to Table 3–1:

(1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

(2) For more information about using the CONFIG_IO instruction, refer to the *MorphIO: An I/O Reconfiguration Solution for Altera Devices* White Paper.

Table 4–12. Typical Pre-Emphasis (First Post-Tap), *(Note 1)*

V_{cc} HTX = 1.5 V	First Post Tap Pre-Emphasis Level				
V_{OD} Setting (mV)	1	2	3	4	5
1000	—	—	23%	36%	49%
1200	—	—	17%	25%	35%

Note to Table 4–12:

(1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

Table 4–13. Typical Pre-Emphasis (First Post-Tap), *(Note 1)*

V_{cc} HTX = 1.2 V	First Post Tap Pre-Emphasis Level				
V_{OD} Setting (mV)	1	2	3	4	5
	TX Term = 100 Ω				
320	24%	61%	114%	—	—
480	—	31%	55%	86%	121%
640	—	20%	35%	54%	72%
800	—	—	23%	36%	49%
960	—	—	18%	25%	35%

Note to Table 4–13:

(1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

DC Electrical Characteristics

Table 4–14 lists the Arria GX device family DC electrical characteristics.

Table 4–14. Arria GX Device DC Operating Conditions (Part 1 of 2) *(Note 1)*

Symbol	Parameter	Conditions	Device	Min	Typ	Max	Units
I_I	Input pin leakage current	$V_I = V_{CCIOmax}$ to 0 V *(2)*	All	–10	—	10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V *(2)*	All	–10	—	10	µA
I_{CCINT0}	V_{CCINT} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25 °C	EP1AGX20/35	—	0.30	*(3)*	A
			EP1AGX50/60	—	0.50	*(3)*	A
			EP1AGX90	—	0.62	*(3)*	A
I_{CCPD0}	V_{CCPD} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25 °C, V_{CCPD} = 3.3V	EP1AGX20/35	—	2.7	*(3)*	mA
			EP1AGX50/60	—	3.6	*(3)*	mA
			EP1AGX90	—	4.3	*(3)*	mA
I_{CCIO0}	V_{CCIO} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25 °C	EP1AGX20/35	—	4.0	*(3)*	mA
			EP1AGX50/60	—	4.0	*(3)*	mA
			EP1AGX90	—	4.0	*(3)*	mA

Table 4–41. Series On-Chip Termination Specification for Left I/O Banks

Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	Industrial Max	Units
25-Ω R_S 3.3/2.5	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.3/2.5V	±30	±30	%
50-Ω R_S 3.3/2.5/1.8	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5/1.8V	±30	±30	%
50-Ω R_S 1.5	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.5V	±36	±36	%
R_D	Internal differential termination for LVDS (100-Ω setting)	V_{CCIO} = 2.5V	±20	±25	%

Pin Capacitance

Table 4–42 shows the Arria GX device family pin capacitance.

Table 4–42. Arria GX Device Capacitance *(Note 1)*

Symbol	Parameter	Typical	Units
C_{IOTB}	Input capacitance on I/O pins in I/O banks 3, 4, 7, and 8.	5.0	pF
C_{IOL}	Input capacitance on I/O pins in I/O banks 1 and 2, including high-speed differential receiver and transmitter pins.	6.1	pF
C_{CLKTB}	Input capacitance on top/bottom clock input pins: `CLK[4..7]` and `CLK[12..15]`.	6.0	pF
C_{CLKL}	Input capacitance on left clock inputs: `CLK0` and `CLK2`.	6.1	pF
C_{CLKL+}	Input capacitance on left clock inputs: `CLK1` and `CLK3`.	3.3	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output/feedback pins in PLL banks 11 and 12.	6.7	pF

Note to Table 4–42:

(1) Capacitance is sample-tested only. Capacitance is measured using time-domain reflections (TDR). Measurement accuracy is within ±0.5 pF.

Power Consumption

Altera offers two ways to calculate power for a design: the Excel-based PowerPlay early power estimator power calculator and the Quartus II PowerPlay power analyzer feature.

The interactive Excel-based PowerPlay Early Power Estimator is typically used prior to designing the FPGA in order to get an estimate of device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after place-and-route is complete. The power analyzer can apply a combination of user-entered, simulation-derived and estimated signal activities which, combined with detailed circuit models, can yield very accurate power estimates.

In both cases, these calculations should only be used as an estimation of power, not as a specification.

Table 4–44. Output Timing Measurement Methodology for Output Pins *(Note 1), (2), (3)*

I/O Standard	Loading and Termination						Measurement Point
	R_S (Ω)	R_D (Ω)	R_T (Ω)	V_{CCIO} (V)	V_{TT} (V)	C_L (pF)	V_{MEAS} (V)
1.8-V differential HSTL Class II	—	—	25	1.660	0.790	0	0.83
LVDS	—	100	—	2.325	—	0	1.1625
LVPECL	—	100	—	3.135	—	0	1.5675

Notes to Table 4–44:

(1) Input measurement point at internal node is 0.5 V_{CCINT}.

(2) Output measuring point for V_{MEAS} at buffer output is 0.5 V_{CCIO}.

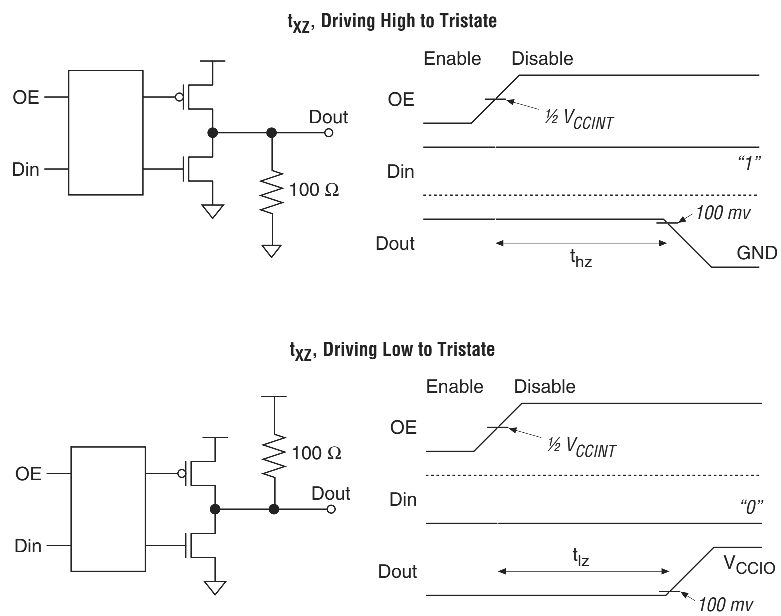
(3) Input stimulus edge rate is 0 to V_{CC} in 0.2 ns (internal signal) from the driver preceding the I/O buffer.

(4) Less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V with less than 30-mV ripple.

(5) V_{CCPD} = 2.97 V, less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V.

Figure 4–8 and Figure 4–9 show the measurement setup for output disable and output enable timing.

Figure 4–8. Measurement Setup for t_{xz} *(Note 1)*



Note to Figure 4–8:

(1) V_{CCINT} is 1.12 V for this measurement.

Table 4–49. EP1AGX20 Column Pins Input Timing Parameters (Part 2 of 3)

I/O Standard	Clock	Parameter	Fast Corner Industrial	Fast Corner Commercial	–6 Speed Grade	Units
SSTL-2 CLASS II	GCLK	t_{SU}	1.075	1.075	2.372	ns
		t_H	–0.970	–0.970	–2.095	ns
	GCLK PLL	t_{SU}	2.517	2.517	5.480	ns
		t_H	–2.412	–2.412	–5.203	ns
SSTL-18 CLASS I	GCLK	t_{SU}	1.113	1.113	2.479	ns
		t_H	–1.008	–1.008	–2.202	ns
	GCLK PLL	t_{SU}	2.555	2.555	5.585	ns
		t_H	–2.450	–2.450	–5.308	ns
SSTL-18 CLASS II	GCLK	t_{SU}	1.114	1.114	2.479	ns
		t_H	–1.009	–1.009	–2.202	ns
	GCLK PLL	t_{SU}	2.556	2.556	5.587	ns
		t_H	–2.451	–2.451	–5.310	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	1.113	1.113	2.479	ns
		t_H	–1.008	–1.008	–2.202	ns
	GCLK PLL	t_{SU}	2.555	2.555	5.585	ns
		t_H	–2.450	–2.450	–5.308	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	1.114	1.114	2.479	ns
		t_H	–1.009	–1.009	–2.202	ns
	GCLK PLL	t_{SU}	2.556	2.556	5.587	ns
		t_H	–2.451	–2.451	–5.310	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.131	1.131	2.607	ns
		t_H	–1.026	–1.026	–2.330	ns
	GCLK PLL	t_{SU}	2.573	2.573	5.713	ns
		t_H	–2.468	–2.468	–5.436	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.132	1.132	2.607	ns
		t_H	–1.027	–1.027	–2.330	ns
	GCLK PLL	t_{SU}	2.574	2.574	5.715	ns
		t_H	–2.469	–2.469	–5.438	ns
3.3-V PCI	GCLK	t_{SU}	1.256	1.256	2.903	ns
		t_H	–1.151	–1.151	–2.626	ns
	GCLK PLL	t_{SU}	2.698	2.698	6.009	ns
		t_H	–2.593	–2.593	–5.732	ns
3.3-V PCI-X	GCLK	t_{SU}	1.256	1.256	2.903	ns
		t_H	–1.151	–1.151	–2.626	ns
	GCLK PLL	t_{SU}	2.698	2.698	6.009	ns
		t_H	–2.593	–2.593	–5.732	ns

Table 4–50. EP1AGX20 Row Pins output Timing Parameters (Part 2 of 2)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.626	2.626	5.614	ns
		GCLK PLL	t_{CO}	1.207	1.207	2.542	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.602	2.602	5.538	ns
		GCLK PLL	t_{CO}	1.183	1.183	2.466	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.568	2.568	5.407	ns
		GCLK PLL	t_{CO}	1.149	1.149	2.335	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.614	2.614	5.556	ns
		GCLK PLL	t_{CO}	1.195	1.195	2.484	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.618	2.618	5.485	ns
		GCLK PLL	t_{CO}	1.199	1.199	2.413	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.594	2.594	5.468	ns
		GCLK PLL	t_{CO}	1.175	1.175	2.396	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.597	2.597	5.447	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.375	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.595	2.595	5.466	ns
		GCLK PLL	t_{CO}	1.176	1.176	2.394	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.598	2.598	5.430	ns
		GCLK PLL	t_{CO}	1.179	1.179	2.358	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.580	2.580	5.426	ns
		GCLK PLL	t_{CO}	1.161	1.161	2.354	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.584	2.584	5.415	ns
		GCLK PLL	t_{CO}	1.165	1.165	2.343	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.575	2.575	5.414	ns
		GCLK PLL	t_{CO}	1.156	1.156	2.342	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.594	2.594	5.443	ns
		GCLK PLL	t_{CO}	1.175	1.175	2.371	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.597	2.597	5.429	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.357	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.582	2.582	5.421	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.349	ns
LVDS	—	GCLK	t_{CO}	2.654	2.654	5.613	ns
		GCLK PLL	t_{CO}	1.226	1.226	2.530	ns

Table 4–55. EP1AGX35 Column Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.131	1.131	2.607	ns
		t_H	–1.026	–1.026	–2.330	ns
	GCLK PLL	t_{SU}	2.573	2.573	5.713	ns
		t_H	–2.468	–2.468	–5.436	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.132	1.132	2.607	ns
		t_H	–1.027	–1.027	–2.330	ns
	GCLK PLL	t_{SU}	2.574	2.574	5.715	ns
		t_H	–2.469	–2.469	–5.438	ns
3.3-V PCI	GCLK	t_{SU}	1.256	1.256	2.903	ns
		t_H	–1.151	–1.151	–2.626	ns
	GCLK PLL	t_{SU}	2.698	2.698	6.009	ns
		t_H	–2.593	–2.593	–5.732	ns
3.3-V PCI-X	GCLK	t_{SU}	1.256	1.256	2.903	ns
		t_H	–1.151	–1.151	–2.626	ns
	GCLK PLL	t_{SU}	2.698	2.698	6.009	ns
		t_H	–2.593	–2.593	–5.732	ns
LVDS	GCLK	t_{SU}	1.106	1.106	2.489	ns
		t_H	–1.001	–1.001	–2.212	ns
	GCLK PLL	t_{SU}	2.530	2.530	5.564	ns
		t_H	–2.425	–2.425	–5.287	ns

Table 4–56 lists I/O timing specifications.

Table 4–56. EP1AGX35 Row Pins Output Timing Parameters (Part 1 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	2.904	2.904	6.699	ns
		GCLK PLL	t_{CO}	1.485	1.485	3.627	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.776	2.776	6.059	ns
		GCLK PLL	t_{CO}	1.357	1.357	2.987	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.720	2.720	6.022	ns
		GCLK PLL	t_{CO}	1.301	1.301	2.950	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.776	2.776	6.059	ns
		GCLK PLL	t_{CO}	1.357	1.357	2.987	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.670	2.670	5.753	ns
		GCLK PLL	t_{CO}	1.251	1.251	2.681	ns
2.5 V	4 mA	GCLK	t_{CO}	2.759	2.759	6.033	ns
		GCLK PLL	t_{CO}	1.340	1.340	2.961	ns

Table 4–61 lists I/O timing specifications.

Table 4–61. EP1AGX50 Column Pins Input Timing Parameters (Part 1 of 2)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.242	1.242	2.902	ns
		t_H	–1.137	–1.137	–2.625	ns
	GCLK PLL	t_{SU}	2.684	2.684	6.009	ns
		t_H	–2.579	–2.579	–5.732	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.242	1.242	2.902	ns
		t_H	–1.137	–1.137	–2.625	ns
	GCLK PLL	t_{SU}	2.684	2.684	6.009	ns
		t_H	–2.579	–2.579	–5.732	ns
2.5 V	GCLK	t_{SU}	1.252	1.252	2.884	ns
		t_H	–1.147	–1.147	–2.607	ns
	GCLK PLL	t_{SU}	2.694	2.694	5.991	ns
		t_H	–2.589	–2.589	–5.714	ns
1.8 V	GCLK	t_{SU}	1.318	1.318	3.094	ns
		t_H	–1.213	–1.213	–2.817	ns
	GCLK PLL	t_{SU}	2.760	2.760	6.201	ns
		t_H	–2.655	–2.655	–5.924	ns
1.5 V	GCLK	t_{SU}	1.321	1.321	3.187	ns
		t_H	–1.216	–1.216	–2.910	ns
	GCLK PLL	t_{SU}	2.763	2.763	6.294	ns
		t_H	–2.658	–2.658	–6.017	ns
SSTL-2 CLASS I	GCLK	t_{SU}	1.034	1.034	2.314	ns
		t_H	–0.929	–0.929	–2.037	ns
	GCLK PLL	t_{SU}	2.500	2.500	5.457	ns
		t_H	–2.395	–2.395	–5.180	ns
SSTL-2 CLASS II	GCLK	t_{SU}	1.034	1.034	2.314	ns
		t_H	–0.929	–0.929	–2.037	ns
	GCLK PLL	t_{SU}	2.500	2.500	5.457	ns
		t_H	–2.395	–2.395	–5.180	ns
SSTL-18 CLASS I	GCLK	t_{SU}	1.104	1.104	2.466	ns
		t_H	–0.999	–0.999	–2.189	ns
	GCLK PLL	t_{SU}	2.546	2.546	5.573	ns
		t_H	–2.441	–2.441	–5.296	ns
SSTL-18 CLASS II	GCLK	t_{SU}	1.074	1.074	2.424	ns
		t_H	–0.969	–0.969	–2.147	ns
	GCLK PLL	t_{SU}	2.539	2.539	5.564	ns
		t_H	–2.434	–2.434	–5.287	ns

Table 4–63. EP1AGX50 Column Pins Output Timing Parameters (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.695	2.695	5.893	ns
		GCLK PLL	t_{CO}	1.239	1.239	2.780	ns
3.3-V LVCMOS	12 mA	GCLK	t_{CO}	2.663	2.663	5.809	ns
		GCLK PLL	t_{CO}	1.211	1.211	2.702	ns
3.3-V LVCMOS	16 mA	GCLK	t_{CO}	2.666	2.666	5.776	ns
		GCLK PLL	t_{CO}	1.218	1.218	2.670	ns
3.3-V LVCMOS	20 mA	GCLK	t_{CO}	2.651	2.651	5.758	ns
		GCLK PLL	t_{CO}	1.205	1.205	2.652	ns
3.3-V LVCMOS	24 mA	GCLK	t_{CO}	2.638	2.638	5.736	ns
		GCLK PLL	t_{CO}	1.194	1.194	2.630	ns
2.5 V	4 mA	GCLK	t_{CO}	2.754	2.754	6.240	ns
		GCLK PLL	t_{CO}	1.293	1.293	3.107	ns
2.5 V	8 mA	GCLK	t_{CO}	2.697	2.697	5.963	ns
		GCLK PLL	t_{CO}	1.241	1.241	2.845	ns
2.5 V	12 mA	GCLK	t_{CO}	2.672	2.672	5.837	ns
		GCLK PLL	t_{CO}	1.220	1.220	2.728	ns
2.5 V	16 mA	GCLK	t_{CO}	2.654	2.654	5.760	ns
		GCLK PLL	t_{CO}	1.202	1.202	2.654	ns
1.8 V	2 mA	GCLK	t_{CO}	2.804	2.804	7.295	ns
		GCLK PLL	t_{CO}	1.333	1.333	4.099	ns
1.8 V	4 mA	GCLK	t_{CO}	2.808	2.808	6.479	ns
		GCLK PLL	t_{CO}	1.338	1.338	3.325	ns
1.8 V	6 mA	GCLK	t_{CO}	2.717	2.717	6.195	ns
		GCLK PLL	t_{CO}	1.262	1.262	3.061	ns
1.8 V	8 mA	GCLK	t_{CO}	2.719	2.719	6.098	ns
		GCLK PLL	t_{CO}	1.264	1.264	2.970	ns
1.8 V	10 mA	GCLK	t_{CO}	2.671	2.671	6.012	ns
		GCLK PLL	t_{CO}	1.218	1.218	2.893	ns
1.8 V	12 mA	GCLK	t_{CO}	2.671	2.671	5.953	ns
		GCLK PLL	t_{CO}	1.219	1.219	2.836	ns
1.5 V	2 mA	GCLK	t_{CO}	2.779	2.779	6.815	ns
		GCLK PLL	t_{CO}	1.313	1.313	3.629	ns
1.5 V	4 mA	GCLK	t_{CO}	2.703	2.703	6.210	ns
		GCLK PLL	t_{CO}	1.249	1.249	3.060	ns
1.5 V	6 mA	GCLK	t_{CO}	2.705	2.705	6.118	ns
		GCLK PLL	t_{CO}	1.252	1.252	2.942	ns
1.5 V	8 mA	GCLK	t_{CO}	2.660	2.660	6.014	ns
		GCLK PLL	t_{CO}	1.211	1.211	2.889	ns

Table 4–73. EP1AGX90 Column Pins Input Timing Parameters (Part 2 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
1.8 V	GCLK	t_{SU}	1.094	1.094	2.482	ns
		t_H	–0.989	–0.989	–2.205	ns
	GCLK PLL	t_{SU}	3.158	3.158	6.617	ns
		t_H	–3.053	–3.053	–6.340	ns
1.5 V	GCLK	t_{SU}	1.097	1.097	2.575	ns
		t_H	–0.992	–0.992	–2.298	ns
	GCLK PLL	t_{SU}	3.161	3.161	6.710	ns
		t_H	–3.056	–3.056	–6.433	ns
SSTL-2 CLASS I	GCLK	t_{SU}	0.844	0.844	1.751	ns
		t_H	–0.739	–0.739	–1.474	ns
	GCLK PLL	t_{SU}	2.908	2.908	5.886	ns
		t_H	–2.803	–2.803	–5.609	ns
SSTL-2 CLASS II	GCLK	t_{SU}	0.844	0.844	1.751	ns
		t_H	–0.739	–0.739	–1.474	ns
	GCLK PLL	t_{SU}	2.908	2.908	5.886	ns
		t_H	–2.803	–2.803	–5.609	ns
SSTL-18 CLASS I	GCLK	t_{SU}	0.880	0.880	1.854	ns
		t_H	–0.775	–0.775	–1.577	ns
	GCLK PLL	t_{SU}	2.944	2.944	5.989	ns
		t_H	–2.839	–2.839	–5.712	ns
SSTL-18 CLASS II	GCLK	t_{SU}	0.883	0.883	1.858	ns
		t_H	–0.778	–0.778	–1.581	ns
	GCLK PLL	t_{SU}	2.947	2.947	5.993	ns
		t_H	–2.842	–2.842	–5.716	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	0.880	0.880	1.854	ns
		t_H	–0.775	–0.775	–1.577	ns
	GCLK PLL	t_{SU}	2.944	2.944	5.989	ns
		t_H	–2.839	–2.839	–5.712	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	0.883	0.883	1.858	ns
		t_H	–0.778	–0.778	–1.581	ns
	GCLK PLL	t_{SU}	2.947	2.947	5.993	ns
		t_H	–2.842	–2.842	–5.716	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	0.898	0.898	1.982	ns
		t_H	–0.793	–0.793	–1.705	ns
	GCLK PLL	t_{SU}	2.962	2.962	6.117	ns
		t_H	–2.857	–2.857	–5.840	ns

Table 4–75. EP1AGX90 Column Pins Output Timing Parameters (Part 3 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.860	2.860	6.313	ns
		GCLK PLL	t_{CO}	0.798	0.798	2.182	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.839	2.839	6.294	ns
		GCLK PLL	t_{CO}	0.777	0.777	2.163	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.844	2.844	6.292	ns
		GCLK PLL	t_{CO}	0.782	0.782	2.161	ns
SSTL-18 CLASS I	12 mA	GCLK	t_{CO}	2.838	2.838	6.278	ns
		GCLK PLL	t_{CO}	0.776	0.776	2.147	ns
SSTL-18 CLASS II	8 mA	GCLK	t_{CO}	2.827	2.827	6.244	ns
		GCLK PLL	t_{CO}	0.765	0.765	2.113	ns
SSTL-18 CLASS II	16 mA	GCLK	t_{CO}	2.839	2.839	6.222	ns
		GCLK PLL	t_{CO}	0.777	0.777	2.091	ns
SSTL-18 CLASS II	18 mA	GCLK	t_{CO}	2.835	2.835	6.230	ns
		GCLK PLL	t_{CO}	0.773	0.773	2.099	ns
SSTL-18 CLASS II	20 mA	GCLK	t_{CO}	2.835	2.835	6.228	ns
		GCLK PLL	t_{CO}	0.773	0.773	2.097	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.861	2.861	6.287	ns
		GCLK PLL	t_{CO}	0.797	0.797	2.152	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.864	2.864	6.268	ns
		GCLK PLL	t_{CO}	0.802	0.802	2.137	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.842	2.842	6.257	ns
		GCLK PLL	t_{CO}	0.780	0.780	2.126	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.846	2.846	6.263	ns
		GCLK PLL	t_{CO}	0.784	0.784	2.132	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.838	2.838	6.256	ns
		GCLK PLL	t_{CO}	0.776	0.776	2.125	ns
1.8-V HSTL CLASS II	16 mA	GCLK	t_{CO}	2.821	2.821	6.020	ns
		GCLK PLL	t_{CO}	0.759	0.759	1.889	ns
1.8-V HSTL CLASS II	18 mA	GCLK	t_{CO}	2.823	2.823	6.031	ns
		GCLK PLL	t_{CO}	0.761	0.761	1.900	ns
1.8-V HSTL CLASS II	20 mA	GCLK	t_{CO}	2.823	2.823	6.040	ns
		GCLK PLL	t_{CO}	0.761	0.761	1.909	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.861	2.861	6.286	ns
		GCLK PLL	t_{CO}	0.797	0.797	2.151	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.863	2.863	6.260	ns
		GCLK PLL	t_{CO}	0.801	0.801	2.129	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.845	2.845	6.262	ns
		GCLK PLL	t_{CO}	0.783	0.783	2.131	ns