Intel - EP1AGX60EF1152C6N Datasheet

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	3005
Number of Logic Elements/Cells	60100
Total RAM Bits	2528640
Number of I/O	514
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1agx60ef1152c6n

Table 1–1. Arria GX Device Features (Part 2 of 2)

Feature	EP1AGX20C	EP1AGX35C/D		EP1AGX50C/D		EP1AGX60C/D/E			EP1AGX90E
	C	C	D	C	D	C	D	E	E
Source-synchronous transmit channels	29	29	29	29	29, 42	29	29	42	45
M512 RAM blocks (32 × 18 bits)	166	197		313		326			478
M4K RAM blocks (128 × 36 bits)	118	140		242		252			400
M-RAM blocks (4096 × 144 bits)	1	1		2		2			4
Total RAM bits	1,229,184	1,348,416		2,475,072		2,528,640			4,477,824
Embedded multipliers (18 × 18)	40	56		104		128			176
DSP blocks	10	14		26		32			44
PLLs	4	4		4	4, 8	4		8	8
Maximum user I/O pins	230, 341	230	341	229	350, 514	229	350	514	538

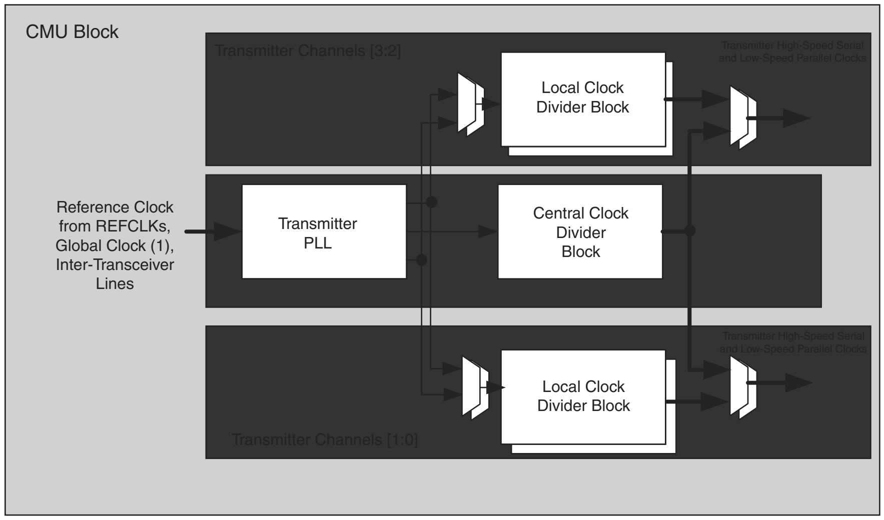
Arria GX devices are available in space-saving FBGA packages (refer to Table 1–2). All Arria GX devices support vertical migration within the same package. With vertical migration support, designers can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities. For I/O pin migration across densities, the designer must cross-reference the available I/O pins with the device pin-outs for all planned densities of a given package type to identify which I/O pins are migratable.

Table 1–2. Arria GX Package Options (Pin Counts and Transceiver Channels) (Part 1 of 2)

Device	Transceiver Channels	Source-Synchronous Channels		Maximum User I/O Pin Count		
		Receive	Transmit	484-Pin FBGA (23 mm)	780-Pin FBGA (29 mm)	1152-Pin FBGA (35 mm)
EP1AGX20C	4	31	29	230	341	—
EP1AGX35C	4	31	29	230	—	—
EP1AGX50C	4	31	29	229	—	—
EP1AGX60C	4	31	29	229	—	—
EP1AGX35D	8	31	29	—	341	—
EP1AGX50D	8	31, 42	29, 42	—	350	514

Figure 2–3 shows the block diagram of the clock multiplier unit.

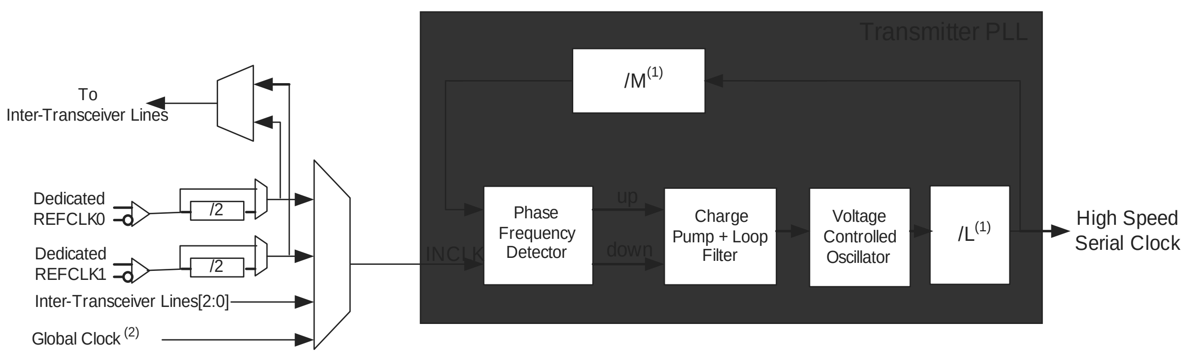
Figure 2–3. Clock Multiplier Unit



The transmitter PLL multiplies the input reference clock to generate the high-speed serial clock required to support the intended protocol. It implements a half-rate voltage controlled oscillator (VCO) that generates a clock at half the frequency of the serial data rate for which it is configured.

Figure 2–4 shows the block diagram of the transmitter PLL.

Figure 2–4. Transmitter PLL



Notes to Figure 2–4:

(1) You only need to select the protocol and the available input reference clock frequency in the ALTGXB MegaWizard Plug-In Manager. Based on your selections, the MegaWizard Plug-In Manager automatically selects the necessary /M and /L dividers (clock multiplication factors).

(2) The global clock line must be driven from an input pin only.

The reference clock input to the transmitter PLL can be derived from:

- One of two available dedicated reference clock input pins (`REFCLK0` or `REFCLK1`) of the associated transceiver block
- PLD global clock network (must be driven directly from an input clock pin and cannot be driven by user logic or enhanced PLL)

You can dynamically put the PCI Express (PIPE) mode transceiver in reverse parallel loopback by controlling the `tx_detectrxloopback` port instantiated in the MegaWizard Plug-In Manager. A high on the `tx_detectrxloopback` port in P0 power state puts the transceiver in reverse parallel loopback. A high on the `tx_detectrxloopback` port in any other power state does not put the transceiver in reverse parallel loopback.

As seen in Figure 2–21, the serial data received on the `rx_datain` port in reverse parallel loopback goes through the CRU, deserializer, word aligner, and the rate matcher blocks. The parallel data at the output of the receiver rate matcher block is looped back to the input of the transmitter serializer block. The serializer converts the parallel data to serial data and feeds it to the transmitter output buffer that drives the data out on the `tx_dataout` port. The data at the output of the rate matcher also goes through the 8B/10B decoder, byte deserializer, and receiver phase compensation FIFO before being fed to the PLD on the `rx_dataout` port.

Reset and Powerdown

Arria GX transceivers offer a power saving advantage with their ability to shut off functions that are not needed.

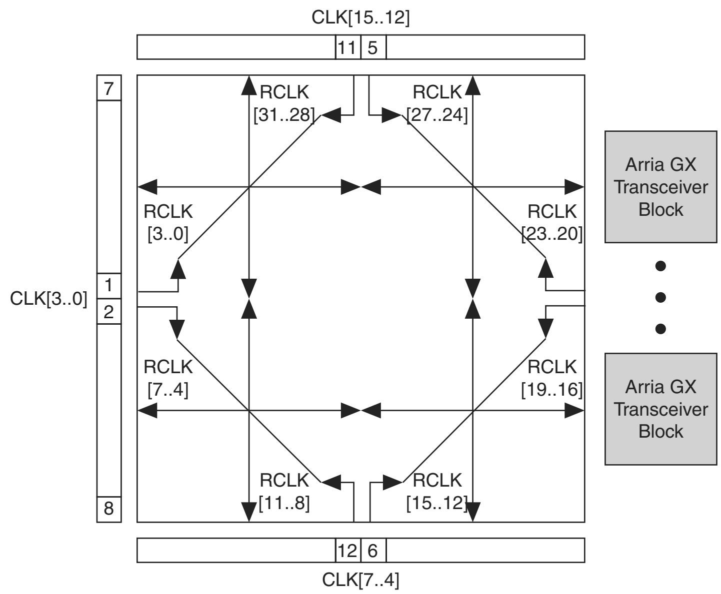
The following three reset signals are available per transceiver channel and can be used to individually reset the digital and analog portions within each channel:

- `tx_digitalreset`
- `rx_analogreset`
- `rx_digitalreset`

The following two powerdown signals are available per transceiver block and can be used to shut down an entire transceiver block that is not being used:

- `gxb_powerdown`
- `gxb_enable`

Figure 2–24. Regional Clock Resources in Arria GX Devices



For the RCLK or GCLK network to route into the transceiver, a local route input output (LRIO) channel is required. Each LRIO clock region has up to eight clock paths and each transceiver block has a maximum of eight clock paths for connecting with LRIO clocks. These resources are limited and determine the number of clocks that can be used between the PLD and transceiver blocks. Table 2–7 and Table 2–8 list the number of LRIO resources available for Arria GX devices with different numbers of transceiver blocks.

Table 2–7. Available Clocking Connections for Transceivers in EP1AGX35D, EP1AGX50D, and EP1AGX60D

Source	Clock Resource		Transceiver	
	Global Clock	Regional Clock	Bank13 8 Clock I/O	Bank14 8 Clock I/O
Region0 8 LRIO clock	✓	RCLK 20-27	✓	—
Region1 8 LRIO clock	✓	RCLK 12-19	—	✓

Table 2–8. Available Clocking Connections for Transceivers in EP1AGX60E and EP1AGX90E

Source	Clock Resource		Transceiver		
	Global Clock	Regional Clock	Bank13 8 Clock I/O	Bank14 8 Clock I/O	Bank15 8 Clock I/O
Region0 8 LRIO clock	✓	RCLK 20-27	✓	—	—
Region1 8 LRIO clock	✓	RCLK 20-27	✓	✓	—
Region2 8 LRIO clock	✓	RCLK 12-19	—	✓	✓
Region3 8 LRIO clock	✓	RCLK 12-19	—	—	✓

Figure 2–51. DSP Block Diagram for 18 × 18-Bit Configuration

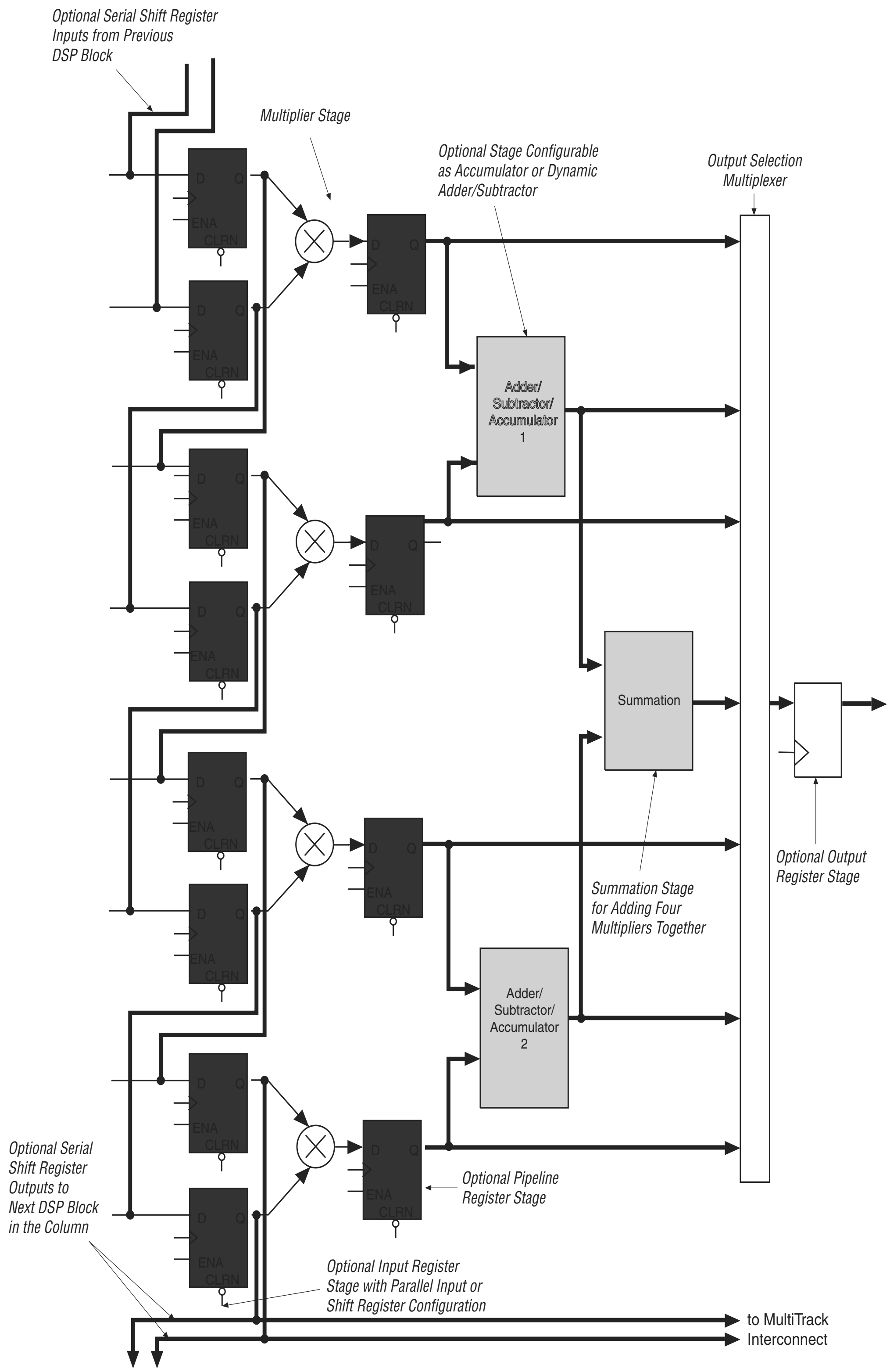
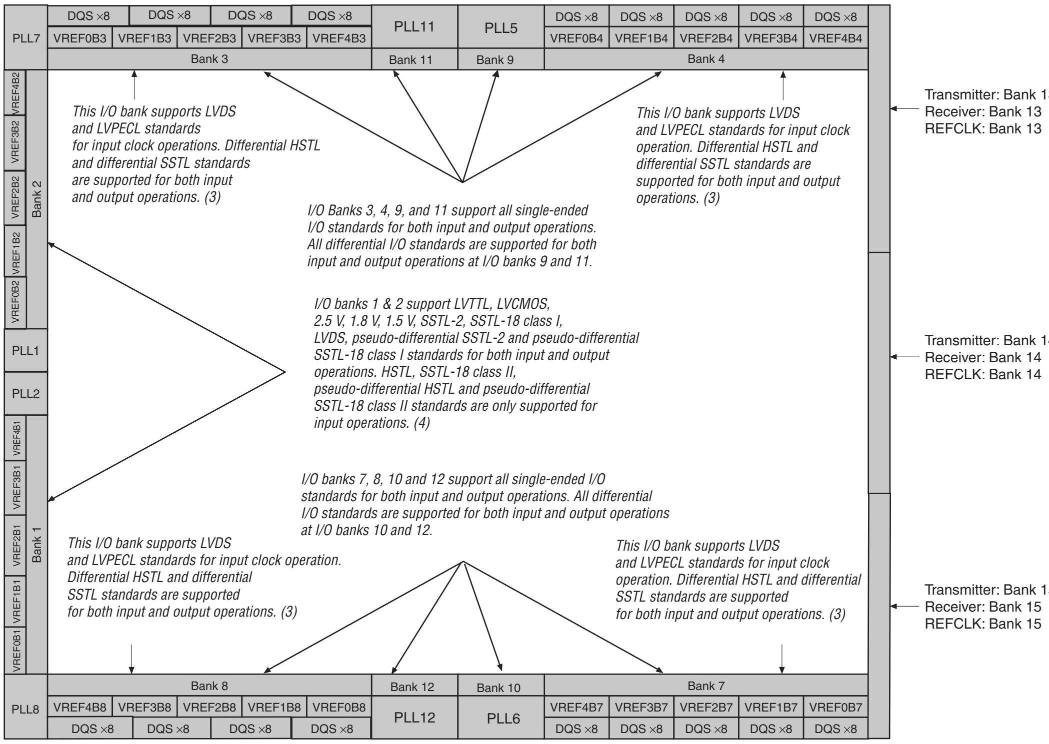


Figure 2–78. Arria GX I/O Banks *(Note 1)*, *(2)*



Notes to Figure 2–78:

(1) Figure 2–78 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

(2) Depending on the size of the device, different device members have different numbers of V_{REF} groups. For the exact locations, refer to the pin list and the Quartus II software.

(3) Banks 9 through 12 are enhanced PLL external clock output banks.

(4) Horizontal I/O banks feature SERDES and DPA circuitry for high-speed differential I/O standards. For more information about differential I/O standards, refer to the *High-Speed Differential I/O Interfaces in Arria GX Devices* chapter.

Each I/O bank has its own `VCCIO` pins. A single device can support 1.5-, 1.8-, 2.5-, and 3.3-V interfaces; each bank can support a different V_{CCIO} level independently. Each bank also has dedicated `VREF` pins to support the voltage-referenced standards (such as SSTL-2).

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. Each bank can support one V_{REF} voltage level. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTL, LVCMOS, and 3.3-V PCI for inputs and outputs.

On-Chip Termination

Arria GX devices provide differential (for the LVDS technology I/O standard) and on-chip series termination to reduce reflections and maintain signal integrity. There is no calibration support for these on-chip termination resistors. On-chip termination simplifies board design by minimizing the number of external termination resistors required. Termination can be placed inside the package, eliminating small stubs that can still lead to reflections.

Table 2–29. Supported TDO/TDI Voltage Combinations

Device	TDI Input Buffer Power	Arria GX TDO V_{CCIO} Voltage Level in I/O Bank 4				
		V_{CCIO} = 3.3 V	V_{CCIO} = 2.5 V	V_{CCIO} = 1.8 V	V_{CCIO} = 1.5 V	V_{CCIO} = 1.2 V
Arria GX	Always V_{CCPD} (3.3 V)	✓ *(1)*	✓ *(2)*	✓ *(3)*	Level shifter required	Level shifter required
Non-Arria GX	VCC = 3.3 V	✓ *(1)*	✓ *(2)*	✓ *(3)*	Level shifter required	Level shifter required
	VCC = 2.5 V	✓ *(1), (4)*	✓ *(2)*	✓ *(3)*	Level shifter required	Level shifter required
	VCC = 1.8 V	✓ *(1), (4)*	✓ *(2), (5)*	✓	Level shifter required	Level shifter required
	VCC = 1.5 V	✓ *(1), (4)*	✓ *(2), (5)*	✓ *(6)*	✓	✓

Notes to Table 2–29:

(1) The `TDO` output buffer meets V_{OH} (MIN) = 2.4 V.
(2) The `TDO` output buffer meets V_{OH} (MIN) = 2.0 V.
(3) An external 250-Ω pull-up resistor is not required, but recommended if signal levels on the board are not optimal.
(4) Input buffer must be 3.3-V tolerant.
(5) Input buffer must be 2.5-V tolerant.
(6) Input buffer must be 1.8-V tolerant.

High-Speed Differential I/O with DPA Support

Arria GX devices contain dedicated circuitry for supporting differential standards at speeds up to 840 Mbps. LVDS differential I/O standards are supported in the Arria GX device. In addition, the LVPECL I/O standard is supported on input and output clock pins on the top and bottom I/O banks.

The high-speed differential I/O circuitry supports the following high-speed I/O interconnect standards and applications:

- SPI-4 Phase 2 (POS-PHY Level 4)
- SFI-4
- Parallel RapidIO standard

There are two dedicated high-speed PLLs (PLL1 and PLL2) in the EP1AGX20 and EP1AGX35 devices and up to four dedicated high-speed PLLs (PLL1, PLL2, PLL7, and PLL8) in the EP1AGX50, EP1AGX60, and EP1AGX90 devices to multiply reference clocks and drive high-speed differential SERDES channels in I/O banks 1 and 2.

Table 2–30 through Table 2–34 list the number of channels that each fast PLL can clock in each of the Arria GX devices. In Table 2–30 through Table 2–34 the first row for each transmitter or receiver provides the maximum number of channels that each fast PLL can drive in its adjacent I/O bank (I/O Bank 1 **or** I/O Bank 2). The second row shows the maximum number of channels that each fast PLL can drive in both I/O banks (I/O Bank 1 **and** I/O Bank 2). For example, in the 780-pin FineLine BGA EP1AGX20 device, PLL 1 can drive a maximum of 16 transmitter channels in I/O Bank 2 or a maximum of 29 transmitter channels in I/O Banks 1 and 2. The Quartus II software can also merge receiver and transmitter PLLs when a receiver is driving a transmitter. In this case, one fast PLL can drive both the maximum numbers of receiver and transmitter channels.

☞ For more information, refer to the "Differential Pin Placement Guidelines" section in the *High-Speed Differential I/O Interfaces with DPA in Arria GX Devices* chapter.

Table 2–30. EP1AGX20 Device Differential Channels *(Note 1)*

Package	Transmitter/Receiver	Total Channels	Center Fast PLLs	
			PLL1	PLL2
484-pin FineLine BGA	Transmitter	29	16	13
			13	16
	Receiver	31	17	14
			14	17
780-pin FineLine GBA	Transmitter	29	16	13
			13	16
	Receiver	31	17	14
			14	17

Note to Table 2–30:

(1) The total number of receiver channels includes the four non-dedicated clock channels that can be optionally used as data channels.

Table 2–31. EP1AGX35 Device Differential Channels *(Note 1)*

Package	Transmitter/Receiver	Total Channels	Center Fast PLLs	
			PLL1	PLL2
484-pin FineLine BGA	Transmitter	29	16	13
			13	16
	Receiver	31	17	14
			14	17
780-pin FineLine BGA	Transmitter	29	16	13
			13	16
	Receiver	31	17	14
			14	17

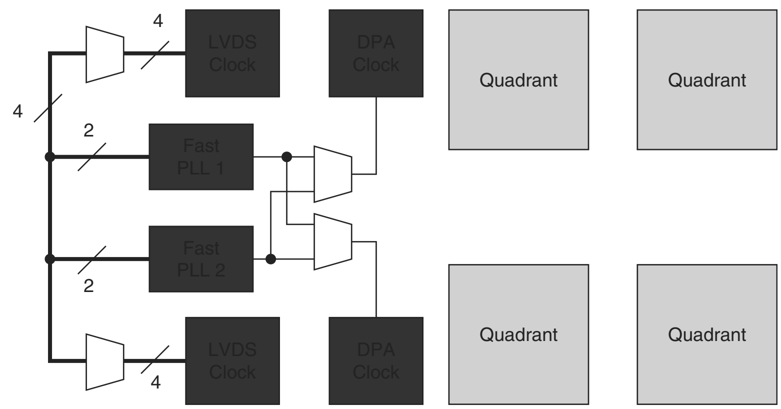
Note to Table 2–31:

(1) The total number of receiver channels includes the four non-dedicated clock channels that can be optionally used as data channels.

Fast PLL and Channel Layout

The receiver and transmitter channels are interleaved as such that each I/O bank on the left side of the device has one receiver channel and one transmitter channel per LAB row. Figure 2–81 shows the fast PLL and channel layout in the EP1AGX20C, EP1AGX35C/D, EP1AGX50C/D and EP1AGX60C/D devices. Figure 2–82 shows the fast PLL and channel layout in EP1AGX60E and EP1AGX90E devices.

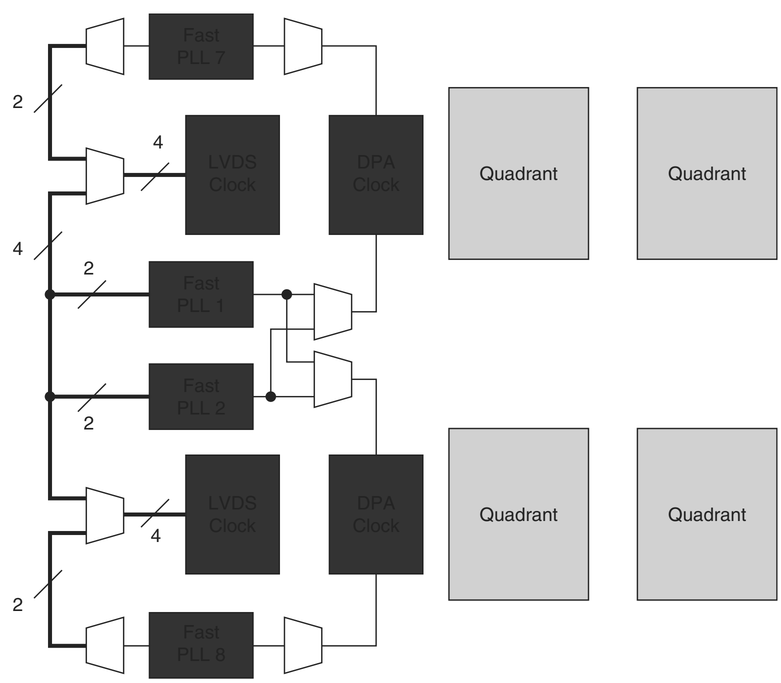
Figure 2–81. Fast PLL and Channel Layout in EP1AGX20C, EP1AGX35C/D, EP1AGX50C/D, EP1AGX60C/D Devices *(Note 1)*



Note to Figure 2–81:

(1) For the number of channels each device supports, refer to Table 2–30.

Figure 2–82. Fast PLL and Channel Layout in EP1AGX60E and EP1AGX90E Devices *(Note 1)*



Note to Figure 2–82:

(1) For the number of channels each device supports, refer to Table 2–30 through Table 2–34.

In addition to the number of configuration methods supported, Arria GX devices also offer decompression and remote system upgrade features. The decompression feature allows Arria GX FPGAs to receive a compressed configuration bitstream and decompress this data in real-time, reducing storage requirements and configuration time. The remote system upgrade feature allows real-time system upgrades from remote locations of Arria GX designs. For more information, refer to “Configuration Schemes” on page 3–5.

Operating Modes

The Arria GX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power up, and before and during configuration. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

SRAM configuration elements allow you to reconfigure Arria GX devices in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, re-initializes the device, and resumes user-mode operation. You can perform in-field upgrades by distributing new configuration files either within the system or remotely.

PORSEL is a dedicated input pin used to select power-on reset (POR) delay times of 12 ms or 100 ms during power up. When the PORSEL pin is connected to ground, the POR time is 100 ms. When the PORSEL pin is connected to V_{CC}, the POR time is 12 ms.

The nIO_PULLUP pin is a dedicated input that chooses whether the internal pull-up resistors on the user I/O pins and dual-purpose configuration I/O pins (nCSO, ASDO, DATA[7..0], nWS, nRS, RDYnBSY, nCS, CS, RUnLU, PGM[2..0], CLKUSR, INIT_DONE, DEV_OE, DEV_CLR) are on or off before and during configuration. A logic high (1.5, 1.8, 2.5, 3.3 V) turns off the weak internal pull-up resistors, while a logic low turns them on.

Arria GX devices also offer a new power supply, V_{CCPD}, which must be connected to 3.3 V in order to power the 3.3-V/2.5-V buffer available on the configuration input pins and JTAG pins. V_{CCPD} applies to all the JTAG input pins (TCK, TMS, TDI, and TRST) and the following configuration pins: nCONFIG, DCLK (when used as an input), nIO_PULLUP, DATA[7..0], RUnLU, nCE, nWS, nRS, CS, nCS, and CLKUSR. The V_{CCSEL} pin allows the V_{CCIO} setting (of the banks where the configuration inputs reside) to be independent of the voltage required by the configuration inputs. Therefore, when selecting the V_{CCIO} voltage, you do not have to take the VIL and VIH levels driven to the configuration inputs into consideration. The configuration input pins, nCONFIG, DCLK (when used as an input), nIO_PULLUP, RUnLU, nCE, nWS, nRS, CS, nCS, and CLKUSR, have a dual buffer design: a 3.3-V/2.5-V input buffer and a 1.8-V/1.5-V input buffer. The V_{CCSEL} input pin selects which input buffer is used. The 3.3-V/2.5-V input buffer is powered by V_{CCPD}, while the 1.8-V/1.5-V input buffer is powered by V_{CCIO}.

Table 4–12. Typical Pre-Emphasis (First Post-Tap), *(Note 1)*

V_{cc} HTX = 1.5 V	First Post Tap Pre-Emphasis Level				
V_{OD} Setting (mV)	**1**	**2**	**3**	**4**	**5**
1000	—	—	23%	36%	49%
1200	—	—	17%	25%	35%

Note to Table 4–12:

(1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

Table 4–13. Typical Pre-Emphasis (First Post-Tap), *(Note 1)*

V_{cc} HTX = 1.2 V	First Post Tap Pre-Emphasis Level				
V_{OD} Setting (mV)	**1**	**2**	**3**	**4**	**5**
	TX Term = 100 Ω				
320	24%	61%	114%	—	—
480	—	31%	55%	86%	121%
640	—	20%	35%	54%	72%
800	—	—	23%	36%	49%
960	—	—	18%	25%	35%

Note to Table 4–13:

(1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

DC Electrical Characteristics

Table 4–14 lists the Arria GX device family DC electrical characteristics.

Table 4–14. Arria GX Device DC Operating Conditions (Part 1 of 2) *(Note 1)*

Symbol	Parameter	Conditions	Device	Min	Typ	Max	Units
I_I	Input pin leakage current	$V_I = V_{CCIOmax}$ to 0 V *(2)*	All	–10	—	10	μA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V *(2)*	All	–10	—	10	μA
I_{CCINT0}	V_{CCINT} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25 °C	EP1AGX20/35	—	0.30	*(3)*	A
			EP1AGX50/60	—	0.50	*(3)*	A
			EP1AGX90	—	0.62	*(3)*	A
I_{CCPD0}	V_{CCPD} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25 °C, V_{CCPD} = 3.3V	EP1AGX20/35	—	2.7	*(3)*	mA
			EP1AGX50/60	—	3.6	*(3)*	mA
			EP1AGX90	—	4.3	*(3)*	mA
I_{CCIO0}	V_{CCIO} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25 °C	EP1AGX20/35	—	4.0	*(3)*	mA
			EP1AGX50/60	—	4.0	*(3)*	mA
			EP1AGX90	—	4.0	*(3)*	mA

Table 4–17. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO} *(1)*	Output supply voltage	—	2.375	2.625	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.3	0.7	V
V_{OH}	High-level output voltage	I_{OH} = –1 mA *(2)*	2.0	—	V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA *(2)*	—	0.4	V

Notes to Table 4–17:

(1) The Arria GX device V_{CCIO} voltage level support of 2.5 to 5% is narrower than defined in the normal range of the EIA/JEDEC standard.

(2) This specification is supported across all the programmable drive settings available for this I/O standard.

Table 4–18. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO} *(1)*	Output supply voltage	—	1.71	1.89	V
V_{IH}	High-level input voltage	—	0.65 × V_{CCIO}	2.25	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(2)*	V_{CCIO} – 0.45	—	V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(2)*	—	0.45	V

Notes to Table 4–18:

(1) The Arria GX device V_{CCIO} voltage level support of 1.8 to 5% is narrower than defined in the normal range of the EIA/JEDEC standard.

(2) This specification is supported across all the programmable drive settings available for this I/O standard, as shown in *Arria GX Architecture* chapter.

Table 4–19. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO} *(1)*	Output supply voltage	—	1.425	1.575	V
V_{IH}	High-level input voltage	—	0.65 V_{CCIO}	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(2)*	0.75 V_{CCIO}	—	V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(2)*	—	0.25 V_{CCIO}	V

Notes to Table 4–19:

(1) The Arria GX device V_{CCIO} voltage level support of 1.5 to 5% is narrower than defined in the normal range of the EIA/JEDEC standard.

(2) This specification is supported across all the programmable drive settings available for this I/O standard, as shown in the *Arria GX Architecture* chapter.

Figure 4–5 and Figure 4–6 show receiver input and transmitter output waveforms, respectively, for all differential I/O standards (LVDS and LVPECL).

Table 4–21. 3.3-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO} *(1)*	I/O supply voltage for top and bottom PLL banks (9, 10, 11, and 12)	—	3.135	3.3	3.465	V
V_{ID}	Input differential voltage swing (single-ended)	—	100	350	900	mV
V_{ICM}	Input common mode voltage	—	200	1,250	1,800	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	250	—	710	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	840	—	1,570	mV
R_L	Receiver differential input discrete resistor (external to Arria GX devices)	—	90	100	110	Ω

Note to Table 4–21:

(1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT}, not V_{CCIO}. The PLL clock output/feedback differential buffers are powered by `VCC_PLL_OUT`. For differential clock output/feedback operation, connect `VCC_PLL_OUT` to 3.3 V.

Table 4–22. 3.3-V PCML Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage	3.135	3.3	3.465	V
V_{ID}	Input differential voltage swing (single-ended)	300	—	600	mV
V_{ICM}	Input common mode voltage	1.5	—	3.465	V
V_{OD}	Output differential voltage (single-ended)	300	370	500	mV
ΔV_{OD}	Change in V_{OD} between high and low	—	—	50	mV
V_{OCM}	Output common mode voltage	2.5	2.85	3.3	V
ΔV_{OCM}	Change in V_{OCM} between high and low	—	—	50	mV
V_T	Output termination voltage	—	V_{CCIO}	—	V
R_1	Output external pull-up resistors	45	50	55	Ω
R_2	Output external pull-up resistors	45	50	55	Ω

Table 4–23. LVPECL Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units	Parameter
V_{CCIO} *(1)*	I/O supply voltage	—	3.135	3.3	3.465	V
V_{ID}	Input differential voltage swing (single-ended)	—	300	600	1,000	mV
V_{ICM}	Input common mode voltage	—	1.0	—	2.5	V
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	525	—	970	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	1,650	—	2,250	mV
R_L	Receiver differential input resistor	—	90	100	110	Ω

Note to Table 4–23:

(1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT}, not V_{CCIO}. The PLL clock output/feedback differential buffers are powered by `VCC_PLL_OUT`. For differential clock output/feedback operation, connect `VCC_PLL_OUT` to 3.3 V.

For more information about PowerPlay tools, refer to the *PowerPlay Early Power Estimator and PowerPlay Power Analyzer* page and the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

For typical I_{CC} standby specifications, refer to Table 4–14 on page 4–14 .

I/O Timing Model

The DirectDrive technology and MultiTrack interconnect ensures predictable performance, accurate simulation, and accurate timing analysis across all Arria GX device densities and speed grades. This section describes and specifies the performance of I/Os.

All specifications are representative of worst-case supply voltage and junction temperature conditions.

The timing numbers listed in the tables of this section are extracted from the Quartus II software version 7.1.

Preliminary, Correlated, and Final Timing

Timing models can have either preliminary, correlated, or final status. The Quartus II software issues an informational message during design compilation if the timing models are preliminary. Table 4–43 lists the status of the Arria GX device timing models.

- **Preliminary** status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.
- **Correlated** numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.
- **Final timing** numbers are based on complete correlation to actual devices and addressing any minor deviations from the correlated timing model. When the timing models are final, all or most of the Arria GX family devices have been completely characterized and no further changes to the timing model are expected.

Table 4–43. Arria GX Device Timing Model Status

Device	Preliminary	Correlated	Final
EP1AGX20	—	—	✓
EP1AGX35	—	—	✓
EP1AGX50	—	—	✓
EP1AGX60	—	—	✓
EP1AGX90	—	—	✓

Table 4–49. EP1AGX20 Column Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
LVDS	GCLK	t_{SU}	1.106	1.106	2.489	ns
		t_H	–1.001	–1.001	–2.212	ns
	GCLK PLL	t_{SU}	2.530	2.530	5.564	ns
		t_H	–2.425	–2.425	–5.287	ns

Table 4–50 describes I/O timing specifications.

Table 4–50. EP1AGX20 Row Pins output Timing Parameters (Part 1 of 2)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	2.904	2.904	6.699	ns
		GCLK PLL	t_{CO}	1.485	1.485	3.627	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.776	2.776	6.059	ns
		GCLK PLL	t_{CO}	1.357	1.357	2.987	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.720	2.720	6.022	ns
		GCLK PLL	t_{CO}	1.301	1.301	2.950	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.776	2.776	6.059	ns
		GCLK PLL	t_{CO}	1.357	1.357	2.987	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.670	2.670	5.753	ns
		GCLK PLL	t_{CO}	1.251	1.251	2.681	ns
2.5 V	4 mA	GCLK	t_{CO}	2.759	2.759	6.033	ns
		GCLK PLL	t_{CO}	1.340	1.340	2.961	ns
2.5 V	8 mA	GCLK	t_{CO}	2.656	2.656	5.775	ns
		GCLK PLL	t_{CO}	1.237	1.237	2.703	ns
2.5 V	12 mA	GCLK	t_{CO}	2.637	2.637	5.661	ns
		GCLK PLL	t_{CO}	1.218	1.218	2.589	ns
1.8 V	2 mA	GCLK	t_{CO}	2.829	2.829	7.052	ns
		GCLK PLL	t_{CO}	1.410	1.410	3.980	ns
1.8 V	4 mA	GCLK	t_{CO}	2.818	2.818	6.273	ns
		GCLK PLL	t_{CO}	1.399	1.399	3.201	ns
1.8 V	6 mA	GCLK	t_{CO}	2.707	2.707	5.972	ns
		GCLK PLL	t_{CO}	1.288	1.288	2.900	ns
1.8 V	8 mA	GCLK	t_{CO}	2.676	2.676	5.858	ns
		GCLK PLL	t_{CO}	1.257	1.257	2.786	ns
1.5 V	2 mA	GCLK	t_{CO}	2.789	2.789	6.551	ns
		GCLK PLL	t_{CO}	1.370	1.370	3.479	ns
1.5 V	4 mA	GCLK	t_{CO}	2.682	2.682	5.950	ns
		GCLK PLL	t_{CO}	1.263	1.263	2.878	ns

Table 4–51 describes I/O timing specifications.

Table 4–51. EP1AGX20 Column Pins Output Timing Parameters (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	2.909	2.909	6.541	ns
		GCLK PLL	t_{CO}	1.467	1.467	3.435	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.764	2.764	6.169	ns
		GCLK PLL	t_{CO}	1.322	1.322	3.063	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.697	2.697	6.169	ns
		GCLK PLL	t_{CO}	1.255	1.255	3.063	ns
3.3-V LVTTL	16 mA	GCLK	t_{CO}	2.671	2.671	6.000	ns
		GCLK PLL	t_{CO}	1.229	1.229	2.894	ns
3.3-V LVTTL	20 mA	GCLK	t_{CO}	2.649	2.649	5.875	ns
		GCLK PLL	t_{CO}	1.207	1.207	2.769	ns
3.3-V LVTTL	24 mA	GCLK	t_{CO}	2.642	2.642	5.877	ns
		GCLK PLL	t_{CO}	1.200	1.200	2.771	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.764	2.764	6.169	ns
		GCLK PLL	t_{CO}	1.322	1.322	3.063	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.672	2.672	5.874	ns
		GCLK PLL	t_{CO}	1.230	1.230	2.768	ns
3.3-V LVCMOS	12 mA	GCLK	t_{CO}	2.644	2.644	5.796	ns
		GCLK PLL	t_{CO}	1.202	1.202	2.690	ns
3.3-V LVCMOS	16 mA	GCLK	t_{CO}	2.651	2.651	5.764	ns
		GCLK PLL	t_{CO}	1.209	1.209	2.658	ns
3.3-V LVCMOS	20 mA	GCLK	t_{CO}	2.638	2.638	5.746	ns
		GCLK PLL	t_{CO}	1.196	1.196	2.640	ns
3.3-V LVCMOS	24 mA	GCLK	t_{CO}	2.627	2.627	5.724	ns
		GCLK PLL	t_{CO}	1.185	1.185	2.618	ns
2.5 V	4 mA	GCLK	t_{CO}	2.726	2.726	6.201	ns
		GCLK PLL	t_{CO}	1.284	1.284	3.095	ns
2.5 V	8 mA	GCLK	t_{CO}	2.674	2.674	5.939	ns
		GCLK PLL	t_{CO}	1.232	1.232	2.833	ns
2.5 V	12 mA	GCLK	t_{CO}	2.653	2.653	5.822	ns
		GCLK PLL	t_{CO}	1.211	1.211	2.716	ns
2.5 V	16 mA	GCLK	t_{CO}	2.635	2.635	5.748	ns
		GCLK PLL	t_{CO}	1.193	1.193	2.642	ns
1.8 V	2 mA	GCLK	t_{CO}	2.766	2.766	7.193	ns
		GCLK PLL	t_{CO}	1.324	1.324	4.087	ns
1.8 V	4 mA	GCLK	t_{CO}	2.771	2.771	6.419	ns
		GCLK PLL	t_{CO}	1.329	1.329	3.313	ns

Table 4–69. EP1AGX60 Column Pins Output Timing Parameters (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
1.8 V	6 mA	GCLK	t_{CO}	2.822	2.822	6.577	ns
		GCLK PLL	t_{CO}	1.252	1.252	3.142	ns
1.8 V	8 mA	GCLK	t_{CO}	2.824	2.824	6.486	ns
		GCLK PLL	t_{CO}	1.254	1.254	3.051	ns
1.8 V	10 mA	GCLK	t_{CO}	2.778	2.778	6.409	ns
		GCLK PLL	t_{CO}	1.208	1.208	2.974	ns
1.8 V	12 mA	GCLK	t_{CO}	2.779	2.779	6.352	ns
		GCLK PLL	t_{CO}	1.209	1.209	2.917	ns
1.5 V	2 mA	GCLK	t_{CO}	2.873	2.873	7.145	ns
		GCLK PLL	t_{CO}	1.303	1.303	3.710	ns
1.5 V	4 mA	GCLK	t_{CO}	2.809	2.809	6.576	ns
		GCLK PLL	t_{CO}	1.239	1.239	3.141	ns
1.5 V	6 mA	GCLK	t_{CO}	2.812	2.812	6.458	ns
		GCLK PLL	t_{CO}	1.242	1.242	3.023	ns
1.5 V	8 mA	GCLK	t_{CO}	2.771	2.771	6.405	ns
		GCLK PLL	t_{CO}	1.201	1.201	2.970	ns
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.757	2.757	6.184	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.744	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.740	2.740	6.134	ns
		GCLK PLL	t_{CO}	1.167	1.167	2.694	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.718	2.718	6.061	ns
		GCLK PLL	t_{CO}	1.145	1.145	2.621	ns
SSTL-2 CLASS II	20 mA	GCLK	t_{CO}	2.719	2.719	6.048	ns
		GCLK PLL	t_{CO}	1.146	1.146	2.608	ns
SSTL-2 CLASS II	24 mA	GCLK	t_{CO}	2.715	2.715	6.046	ns
		GCLK PLL	t_{CO}	1.142	1.142	2.606	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.753	2.753	6.155	ns
		GCLK PLL	t_{CO}	1.183	1.183	2.720	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.758	2.758	6.116	ns
		GCLK PLL	t_{CO}	1.185	1.185	2.676	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.737	2.737	6.097	ns
		GCLK PLL	t_{CO}	1.164	1.164	2.657	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.742	2.742	6.095	ns
		GCLK PLL	t_{CO}	1.169	1.169	2.655	ns
SSTL-18 CLASS I	12 mA	GCLK	t_{CO}	2.736	2.736	6.081	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.641	ns
SSTL-18 CLASS II	8 mA	GCLK	t_{CO}	2.725	2.725	6.047	ns
		GCLK PLL	t_{CO}	1.152	1.152	2.607	ns

Table 4–75. EP1AGX90 Column Pins Output Timing Parameters (Part 2 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
2.5 V	8 mA	GCLK	t_{CO}	2.906	2.906	6.562	ns
		GCLK PLL	t_{CO}	0.842	0.842	2.427	ns
2.5 V	12 mA	GCLK	t_{CO}	2.885	2.885	6.445	ns
		GCLK PLL	t_{CO}	0.821	0.821	2.310	ns
2.5 V	16 mA	GCLK	t_{CO}	2.867	2.867	6.371	ns
		GCLK PLL	t_{CO}	0.803	0.803	2.236	ns
1.8 V	2 mA	GCLK	t_{CO}	2.998	2.998	7.816	ns
		GCLK PLL	t_{CO}	0.934	0.934	3.681	ns
1.8 V	4 mA	GCLK	t_{CO}	3.003	3.003	7.042	ns
		GCLK PLL	t_{CO}	0.939	0.939	2.907	ns
1.8 V	6 mA	GCLK	t_{CO}	2.927	2.927	6.778	ns
		GCLK PLL	t_{CO}	0.863	0.863	2.643	ns
1.8 V	8 mA	GCLK	t_{CO}	2.929	2.929	6.687	ns
		GCLK PLL	t_{CO}	0.865	0.865	2.552	ns
1.8 V	10 mA	GCLK	t_{CO}	2.883	2.883	6.610	ns
		GCLK PLL	t_{CO}	0.819	0.819	2.475	ns
1.8 V	12 mA	GCLK	t_{CO}	2.884	2.884	6.553	ns
		GCLK PLL	t_{CO}	0.820	0.820	2.418	ns
1.5 V	2 mA	GCLK	t_{CO}	2.978	2.978	7.346	ns
		GCLK PLL	t_{CO}	0.914	0.914	3.211	ns
1.5 V	4 mA	GCLK	t_{CO}	2.914	2.914	6.777	ns
		GCLK PLL	t_{CO}	0.850	0.850	2.642	ns
1.5 V	6 mA	GCLK	t_{CO}	2.917	2.917	6.659	ns
		GCLK PLL	t_{CO}	0.853	0.853	2.524	ns
1.5 V	8 mA	GCLK	t_{CO}	2.876	2.876	6.606	ns
		GCLK PLL	t_{CO}	0.812	0.812	2.471	ns
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.859	2.859	6.381	ns
		GCLK PLL	t_{CO}	0.797	0.797	2.250	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.842	2.842	6.331	ns
		GCLK PLL	t_{CO}	0.780	0.780	2.200	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.820	2.820	6.258	ns
		GCLK PLL	t_{CO}	0.758	0.758	2.127	ns
SSTL-2 CLASS II	20 mA	GCLK	t_{CO}	2.821	2.821	6.245	ns
		GCLK PLL	t_{CO}	0.759	0.759	2.114	ns
SSTL-2 CLASS II	24 mA	GCLK	t_{CO}	2.817	2.817	6.243	ns
		GCLK PLL	t_{CO}	0.755	0.755	2.112	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.858	2.858	6.356	ns
		GCLK PLL	t_{CO}	0.794	0.794	2.221	ns

Table 4–107. Arria GX Maximum Output Clock Rate for Dedicated Clock Pins (Part 2 of 4)

I/O Standards	Drive Strength	–6 Speed Grade	Units
SSTL-2 CLASS I	8 mA	280	MHz
	12 mA	327	MHz
SSTL-2 CLASS II	16 mA	280	MHz
	20 mA	327	MHz
	24 mA	327	MHz
SSTL-18 CLASS I	4 mA	140	MHz
	6 mA	186	MHz
	8 mA	280	MHz
	10 mA	373	MHz
	12 mA	373	MHz
SSTL-18 CLASS II	8 mA	140	MHz
	16 mA	327	MHz
	18 mA	373	MHz
	20 mA	420	MHz
1.8-V HSTL CLASS I	4 mA	280	MHz
	6 mA	420	MHz
	8 mA	561	MHz
	10 mA	561	MHz
	12 mA	607	MHz
1.8-V HSTL CLASS II	16 mA	420	MHz
	18 mA	467	MHz
	20 mA	514	MHz
1.5-V HSTL CLASS I	4 mA	280	MHz
	6 mA	420	MHz
	8 mA	561	MHz
	10mA	607	MHz
	12 mA	654	MHz
1.5-V HSTL CLASS II	16 mA	514	MHz
	18 mA	561	MHz
	20 mA	561	MHz
	24 mA	278	MHz
DIFFERENTIAL SSTL-2	8 mA	280	MHz
	12 mA	327	MHz
DIFFERENTIAL 2.5-V SSTL CLASS II	16 mA	280	MHz
	20 mA	327	MHz
	24 mA	327	MHz

Table 4–110. Maximum DCD for DDIO Output on Row I/O Pins Without PLL in the Clock Path *Note (1)*

Maximum DCD (ps) for Row DDIO Output I/O Standard	Input I/O Standard (No PLL in the Clock Path)					Units
	TTL/CMOS		SSTL-2	SSTL/HSTL	LVDS	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	3.3V	
LVDS	180	180	180	180	180	ps

Note to Table 4–110:

(1) Table 4–110 assumes the input clock has zero DCD.

Table 4–111. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path *(Note 1)*

Maximum DCD (ps) for DDIO Column Output I/O Standard	Input IO Standard (No PLL in the Clock Path)				Units
	TTL/CMOS		SSTL-2	SSTL/HSTL	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	
3.3-V LVTTL	440	495	170	160	ps
3.3-V LVCMOS	390	450	120	110	ps
2.5 V	375	430	105	95	ps
1.8 V	325	385	90	100	ps
1.5-V LVCMOS	430	490	160	155	ps
SSTL-2 Class I	355	410	85	75	ps
SSTL-2 Class II	350	405	80	70	ps
SSTL-18 Class I	335	390	65	65	ps
SSTL-18 Class II	320	375	70	80	ps
1.8-V HSTL Class I	330	385	60	70	ps
1.8-V HSTL Class II	330	385	60	70	ps
1.5-V HSTL Class I	330	390	60	70	ps
1.5-V HSTL Class II	330	360	90	100	ps
LVPECL	180	180	180	180	ps

Note to Table 4–111:

(1) Table 4–111 assumes the input clock has zero DCD.

Table 4–112. Maximum DCD for DDIO Output on Row I/O Pins With PLL in the Clock Path

Maximum DCD (ps) for Row DDIO Output I/O Standard	Arria GX Devices (PLL Output Feeding DDIO)	Units
	–6 Speed Grade	
3.3-V LVTTL	105	ps
3.3-V LVCMOS	75	ps
2.5V	90	ps
1.8V	100	ps
1.5-V LVCMOS	100	ps
SSTL-2 Class I	75	ps
SSTL-2 Class II	70	ps