

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

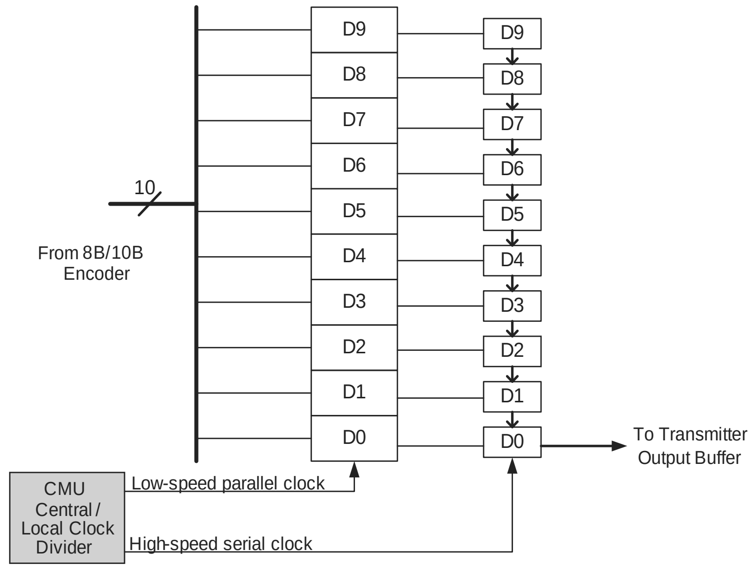
## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 4511 |
| Number of Logic Elements/Cells | 90220 |
| Total RAM Bits | 4477824 |
| Number of I/O | 538 |
| Number of Gates | - |
| Voltage - Supply | 1.15V ~ 1.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1152-BBGA |
| Supplier Device Package | 1152-FBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep1agx90ef1152c6 |

Figure 2–7 shows the serializer block diagram.

**Figure 2–7.** Serializer




## Transmitter Buffer

The Arria GX transceiver buffers support the 1.2- and 1.5-V PCML I/O standard at rates up to 3.125 Gbps. The common mode voltage ($V_{CM}$) of the output driver may be set to 600 or 700 mV.

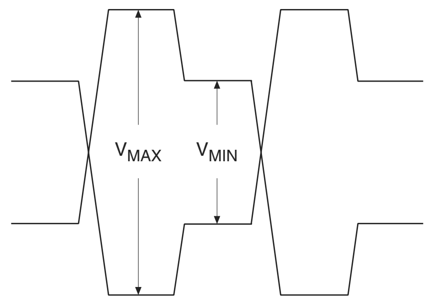
For more information about the Arria GX transceiver buffers, refer to the *Arria GX Transceiver Architecture* chapter.

The output buffer, as shown in Figure 2–8, is directly driven by the high-speed data serializer and consists of a programmable output driver, a programmable pre-emphasis circuit, and OCT circuitry.

### Programmable Pre-Emphasis

The programmable pre-emphasis module controls the output driver to boost high frequency components and compensate for losses in the transmission medium, as shown in Figure 2–10. Pre-emphasis is set statically using the ALTGXB megafunction.

**Figure 2–10.** Pre-Emphasis Signaling




$$\text{Pre-Emphasis \%} = \left(\frac{V_{MAX}}{V_{MIN}} - 1\right) \times 100$$

Pre-emphasis percentage is defined as $(V_{MAX}/V_{MIN} - 1) \times 100$, where $V_{MAX}$ is the differential emphasized voltage (peak-to-peak) and $V_{MIN}$ is the differential steady-state voltage (peak-to-peak).

### PCI Express (PIPE) Receiver Detect

The Arria GX transmitter buffer has a built-in receiver detection circuit for use in PCI Express (PIPE) mode. This circuit provides the ability to detect if there is a receiver downstream by sending out a pulse on the channel and monitoring the reflection. This mode requires a tri-stated transmitter buffer (in electrical idle mode).

### PCI Express (PIPE) Electric Idles (or Individual Transmitter Tri-State)

The Arria GX transmitter buffer supports PCI Express (PIPE) electrical idles. This feature is only active in PCI Express (PIPE) mode. The `tx_forceelecidle` port puts the transmitter buffer in electrical idle mode. This port is available in all PCI Express (PIPE) power-down modes and has specific usage in each mode.

## Receiver Path

This section describes the data path through the Arria GX receiver. The sub-blocks are described in order from the receiver buffer to the PLD-receiver parallel interface.

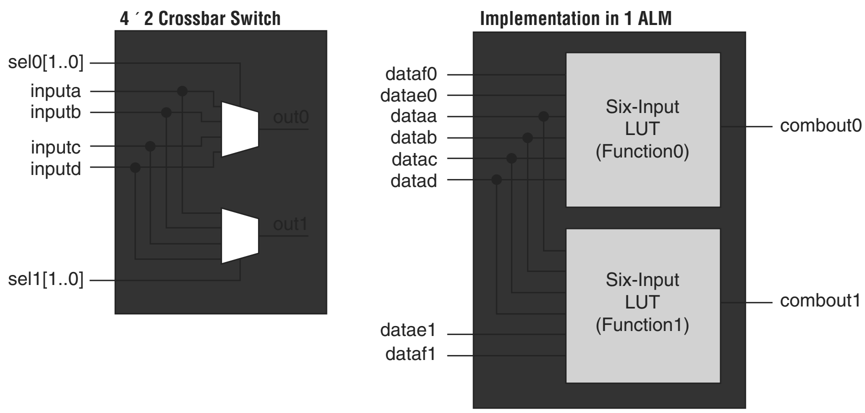
### Receiver Buffer

The Arria GX receiver input buffer supports the 1.2-V and 1.5-V PCML I/O standards at rates up to 3.125 Gbps. The common mode voltage of the receiver input buffer is programmable between 0.85 V and 1.2 V. You must select the 0.85 V common mode voltage for AC- and DC-coupled PCML links and 1.2 V common mode voltage for DC-coupled LVDS links.

To pack two five-input functions into one ALM, the functions must have at least two common inputs. The common inputs are `dataa` and `datab`. The combination of a four-input function with a five-input function requires one common input (either `dataa` or `datab`).

To implement two six-input functions in one ALM, four inputs must be shared and the combinational function must be the same. For example, a 4 × 2 crossbar switch (two 4-to-1 multiplexers with common inputs and unique select lines) can be implemented in one ALM, as shown in Figure 2–31. The shared inputs are `dataa`, `datab`, `datac`, and `datad`, while the unique select lines are `datae0` and `dataf0` for `function0`, and `datae1` and `dataf1` for `function1`. This crossbar switch consumes four LUTs in a four-input LUT-based architecture.

**Figure 2–31.** 4 × 2 Crossbar Switch Example




In a sparsely used device, functions that can be placed into one ALM can be implemented in separate ALMs. The Quartus II Compiler spreads a design out to achieve the best possible performance. As a device begins to fill up, the Quartus II software automatically uses the full potential of the Arria GX ALM. The Quartus II Compiler automatically searches for functions of common inputs or completely independent functions to be placed into one ALM and to make efficient use of the device resources. In addition, you can manually control resource usage by setting location assignments. Any six-input function can be implemented utilizing inputs `dataa`, `datab`, `datac`, `datad`, and either `datae0` and `dataf0` or `datae1` and `dataf1`. If `datae0` and `dataf0` are used, the output is driven to `register0`, and/or `register0` is bypassed and the data drives out to the interconnect using the top set of output drivers (refer to Figure 2–32). If `datae1` and `dataf1` are used, the output drives to `register1` and/or bypasses `register1` and drives to the interconnect using the bottom set of output drivers. The Quartus II Compiler automatically selects the inputs to the LUT. Asynchronous load data for the register comes from the `datae` or `dataf` input of the ALM. ALMs in normal mode support register packing.

**Table 2–12.** M-RAM Row Interface Unit Signals (Part 2 of 2)

| Unit Interface Block | Input Signals | Output Signals |
|---|---|---|
| L4 | datain_a[56..42]<br>byteena_a[5..4] | dataout_a[59..48] |
| L5 | datain_a[71..57]<br>byteena_a[7..6] | dataout_a[71..60] |
| R0 | datain_b[14..0]<br>byteena_b[1..0] | dataout_b[11..0] |
| R1 | datain_b[29..15]<br>byteena_b[3..2] | dataout_b[23..12] |
| R2 | datain_b[35..30]<br>addressb[4..0]<br>addr_ena_b<br>clock_b<br>clocken_b<br>renwe_b<br>aclr_b | dataout_b[35..24] |
| R3 | addressb[15..5]<br>datain_b[41..36] | dataout_b[47..36] |
| R4 | datain_b[56..42]<br>byteena_b[5..4] | dataout_b[59..48] |
| R5 | datain_b[71..57]<br>byteena_b[7..6] | dataout_b[71..60] |

For more information about TriMatrix memory, refer to the *TriMatrix Embedded Memory Blocks in Arria GX Devices* chapter.

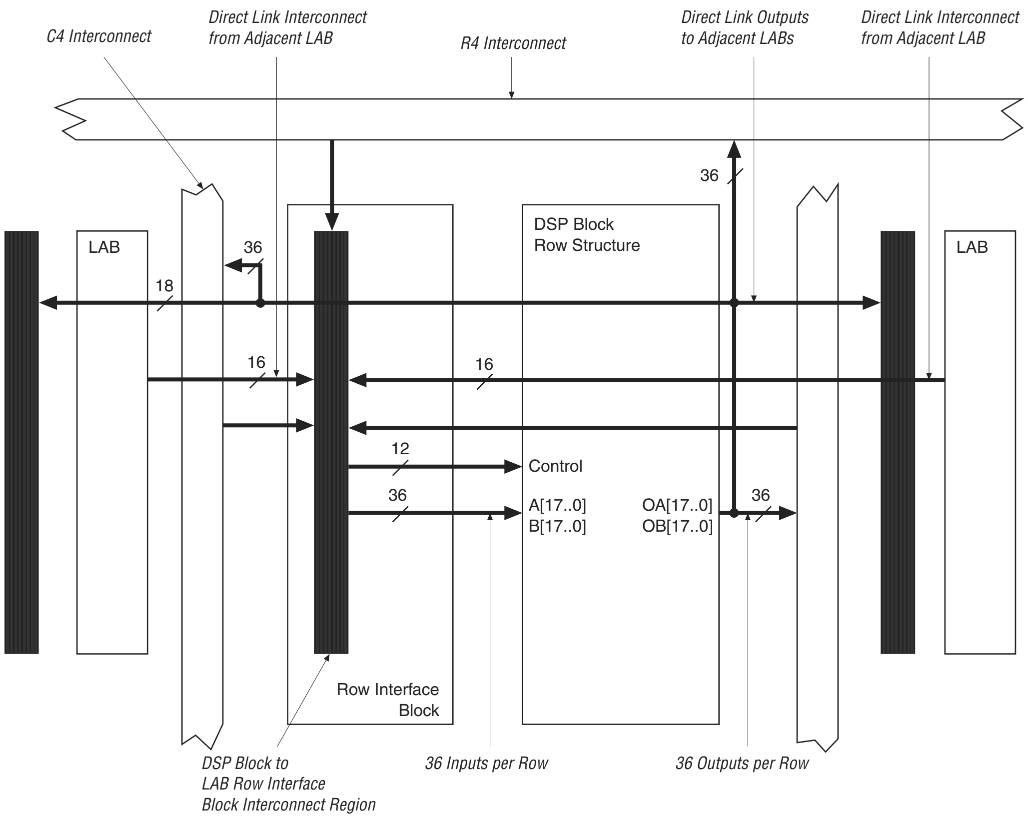
# Digital Signal Processing Block

The most commonly used DSP functions are finite impulse response (FIR) filters, complex FIR filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, direct cosine transform (DCT) functions, and correlators. All of these use the multiplier as the fundamental building block. Additionally, some applications need specialized operations such as multiply-add and multiply-accumulate operations. Arria GX devices provide DSP blocks to meet the arithmetic requirements of these functions.

Each Arria GX device has two to four columns of DSP blocks to efficiently implement DSP functions faster than ALM-based implementations. Each DSP block can be configured to support up to:

- Eight 9 × 9-bit multipliers
- Four 18 × 18-bit multipliers
- One 36 × 36-bit multiplier

**Figure 2–53.** DSP Block Interface to Interconnect



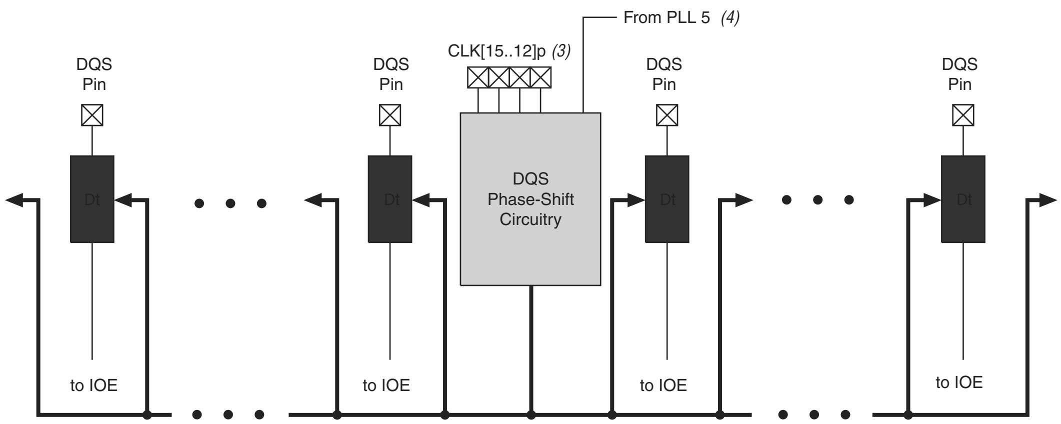

A bus of 44 control signals feeds the entire DSP block. These signals include clocks, asynchronous clears, clock enables, signed and unsigned control signals, addition and subtraction control signals, rounding and saturation control signals, and accumulator synchronous loads. The clock signals are routed from LAB row clocks and are generated from specific LAB rows at the DSP block interface. The LAB row source for control signals, data inputs, and outputs is shown in Table 2–15.

For more information about DSP blocks, refer to the *DSP Blocks in Arria GX Devices* chapter.

The Arria GX device has two phase-shifting reference circuits, one on the top and one on the bottom of the device. The circuit on the top controls the compensated delay elements for all DQS pins on the top. The circuit on the bottom controls the compensated delay elements for all DQS pins on the bottom.

Each phase-shifting reference circuit is driven by a system reference clock, which must have the same frequency as the DQS signal. Clock pins `CLK[15..12]p` feed phase circuitry on the top of the device and clock pins `CLK[7..4]p` feed phase circuitry on the bottom of the device. In addition, PLL clock outputs can also feed the phase-shifting reference circuits. Figure 2–77 shows the phase-shift reference circuit control of each DQS delay shift on the top of the device. This same circuit is duplicated on the bottom of the device.

**Figure 2–77.** DQS Phase-Shift Circuitry *(Note 1), (2)*




**Notes to Figure 2–77:**

(1) There are up to 18 pairs of DQS pins available on the top or bottom of the Arria GX device. There are up to 10 pairs on the right side and 8 pairs on the left side of the DQS phase-shift circuitry.

(2) The “t” module represents the DQS logic block.

(3) Clock pins `CLK[15..12]p` feed phase-shift circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase circuitry on the bottom of the device. You can also use a PLL clock output as a reference clock to phase shift circuitry.

(4) You can only use PLL 5 to feed the DQS phase-shift circuitry on the top of the device and PLL 6 to feed the DQS phase-shift circuitry on the bottom of the device.

These dedicated circuits combined with enhanced PLL clocking and phase-shift ability provide a complete hardware solution for interfacing to high-speed memory.

For more information about external memory interfaces, refer to the *External Memory Interfaces in Arria GX Devices* chapter.

## Programmable Drive Strength

The output buffer for each Arria GX device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL, LVCMOS, SSTL, and HSTL standards have several levels of drive strength that you can control. The default setting used in the Quartus II software is the maximum current strength setting that is used to achieve maximum I/O performance. For all I/O standards, the minimum setting is the lowest drive strength that guarantees the $I_{OH}/I_{OL}$ of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot.

**Table 4–33.** 1.5-V HSTL Class I Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | — | 1.425 | 1.5 | 1.575 | V |
| $V_{REF}$ | Input reference voltage | — | 0.713 | 0.75 | 0.788 | V |
| $V_{TT}$ | Termination voltage | — | 0.713 | 0.75 | 0.788 | V |
| $V_{IH}$ (DC) | DC high-level input voltage | — | $V_{REF}$ + 0.1 | — | — | V |
| $V_{IL}$ (DC) | DC low-level input voltage | — | –0.3 | — | $V_{REF}$ – 0.1 | V |
| $V_{IH}$ (AC) | AC high-level input voltage | — | $V_{REF}$ + 0.2 | — | — | V |
| $V_{IL}$ (AC) | AC low-level input voltage | — | — | — | $V_{REF}$ – 0.2 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = 8 mA *(1)* | $V_{CCIO}$ – 0.4 | — | — | V |
| $V_{OL}$ | Low-level output voltage | $I_{OH}$ = –8 mA *(1)* | — | — | 0.4 | V |

**Note to Table 4–33:**

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Arria GX Architecture* chapter.

**Table 4–34.** 1.5-V HSTL Class II Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | — | 1.425 | 1.50 | 1.575 | V |
| $V_{REF}$ | Input reference voltage | — | 0.713 | 0.75 | 0.788 | V |
| $V_{TT}$ | Termination voltage | — | 0.713 | 0.75 | 0.788 | V |
| $V_{IH}$ (DC) | DC high-level input voltage | — | $V_{REF}$ + 0.1 | — | — | V |
| $V_{IL}$ (DC) | DC low-level input voltage | — | –0.3 | — | $V_{REF}$ – 0.1 | V |
| $V_{IH}$ (AC) | AC high-level input voltage | — | $V_{REF}$ + 0.2 | — | — | V |
| $V_{IL}$ (AC) | AC low-level input voltage | — | — | — | $V_{REF}$ – 0.2 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = 16 mA *(1)* | $V_{CCIO}$ – 0.4 | — | — | V |
| $V_{OL}$ | Low-level output voltage | $I_{OH}$ = –16 mA *(1)* | — | — | 0.4 | V |

**Note to Table 4–34:**

(1) This specification is supported across all the programmable drive settings available for this I/O standard, as shown in the *Arria GX Architecture* chapter.

**Table 4–35.** 1.5-V HSTL Class I & II Differential Specifications

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| $V_{CCIO}$ | I/O supply voltage | 1.425 | 1.5 | 1.575 | V |
| $V_{DIF}$ (DC) | DC input differential voltage | 0.2 | — | — | V |
| $V_{CM}$ (DC) | DC common mode input voltage | 0.68 | — | 0.9 | V |
| $V_{DIF}$ (AC) | AC differential input voltage | 0.4 | — | — | V |
| $V_{OX}$ (AC) | AC differential cross point voltage | 0.68 | — | 0.9 | V |

**Figure 4–9.** Measurement Setup for $t_{zx}$

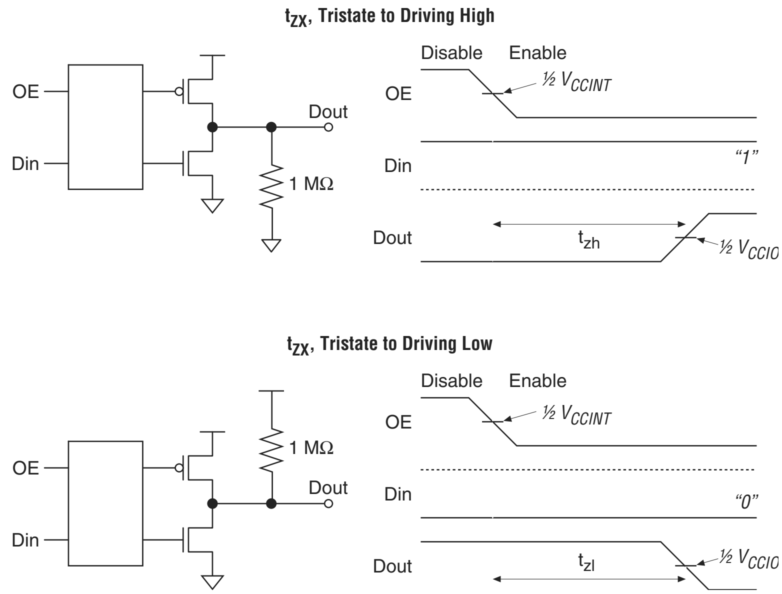



Table 4–45 specifies the input timing measurement setup.

**Table 4–45.** Timing Measurement Methodology for Input Pins *(Note 1)*, *(2)*, *(3)*, *(4)* (Part 1 of 2)

| I/O Standard | Measurement Conditions | | | Measurement Point |
|---|---|---|---|---|
| | $V_{CCIO}$ (V) | $V_{REF}$ (V) | Edge Rate (ns) | VMEAS (V) |
| LVTTL *(5)* | 3.135 | — | 3.135 | 1.5675 |
| LVCMOS *(5)* | 3.135 | — | 3.135 | 1.5675 |
| 2.5 V *(5)* | 2.375 | — | 2.375 | 1.1875 |
| 1.8 V *(5)* | 1.710 | — | 1.710 | 0.855 |
| 1.5 V *(5)* | 1.425 | — | 1.425 | 0.7125 |
| PCI *(6)* | 2.970 | — | 2.970 | 1.485 |
| PCI-X *(6)* | 2.970 | — | 2.970 | 1.485 |
| SSTL-2 Class I | 2.325 | 1.163 | 2.325 | 1.1625 |
| SSTL-2 Class II | 2.325 | 1.163 | 2.325 | 1.1625 |
| SSTL-18 Class I | 1.660 | 0.830 | 1.660 | 0.83 |
| SSTL-18 Class II | 1.660 | 0.830 | 1.660 | 0.83 |
| 1.8-V HSTL Class I | 1.660 | 0.830 | 1.660 | 0.83 |
| 1.8-V HSTL Class II | 1.660 | 0.830 | 1.660 | 0.83 |
| 1.5-V HSTL Class I | 1.375 | 0.688 | 1.375 | 0.6875 |
| 1.5-V HSTL Class II | 1.375 | 0.688 | 1.375 | 0.6875 |
| 1.2-V HSTL with OCT | 1.140 | 0.570 | 1.140 | 0.570 |
| Differential SSTL-2 Class I | 2.325 | 1.163 | 2.325 | 1.1625 |
| Differential SSTL-2 Class II | 2.325 | 1.163 | 2.325 | 1.1625 |
| Differential SSTL-18 Class I | 1.660 | 0.830 | 1.660 | 0.83 |

**Table 4–48.** EP1AGX20 Row Pin Delay Adders for Regional Clock

| Parameter | Fast Corner | | –6 Speed Grade | Units |
|---|---|---|---|---|
| | Industrial | Commercial | | |
| RCLK input adder | 0.117 | 0.117 | 0.273 | ns |
| RCLK PLL input adder | 0.011 | 0.011 | 0.019 | ns |
| RCLK output adder | –0.117 | –0.117 | –0.273 | ns |
| RCLK PLL output adder | –0.011 | –0.011 | –0.019 | ns |

Table 4–49 describes I/O timing specifications.

**Table 4–49.** EP1AGX20 Column Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Corner | | –6 Speed Grade | Units |
|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | | |
| 3.3-V LVTTL | GCLK | $t_{SU}$ | 1.251 | 1.251 | 2.915 | ns |
| | | $t_H$ | –1.146 | –1.146 | –2.638 | ns |
| | GCLK PLL | $t_{SU}$ | 2.693 | 2.693 | 6.021 | ns |
| | | $t_H$ | –2.588 | –2.588 | –5.744 | ns |
| 3.3-V LVCMOS | GCLK | $t_{SU}$ | 1.251 | 1.251 | 2.915 | ns |
| | | $t_H$ | –1.146 | –1.146 | –2.638 | ns |
| | GCLK PLL | $t_{SU}$ | 2.693 | 2.693 | 6.021 | ns |
| | | $t_H$ | –2.588 | –2.588 | –5.744 | ns |
| 2.5 V | GCLK | $t_{SU}$ | 1.261 | 1.261 | 2.897 | ns |
| | | $t_H$ | –1.156 | –1.156 | –2.620 | ns |
| | GCLK PLL | $t_{SU}$ | 2.703 | 2.703 | 6.003 | ns |
| | | $t_H$ | –2.598 | –2.598 | –5.726 | ns |
| 1.8 V | GCLK | $t_{SU}$ | 1.327 | 1.327 | 3.107 | ns |
| | | $t_H$ | –1.222 | –1.222 | –2.830 | ns |
| | GCLK PLL | $t_{SU}$ | 2.769 | 2.769 | 6.213 | ns |
| | | $t_H$ | –2.664 | –2.664 | –5.936 | ns |
| 1.5 V | GCLK | $t_{SU}$ | 1.330 | 1.330 | 3.200 | ns |
| | | $t_H$ | –1.225 | –1.225 | –2.923 | ns |
| | GCLK PLL | $t_{SU}$ | 2.772 | 2.772 | 6.306 | ns |
| | | $t_H$ | –2.667 | –2.667 | –6.029 | ns |
| SSTL-2 CLASS I | GCLK | $t_{SU}$ | 1.075 | 1.075 | 2.372 | ns |
| | | $t_H$ | –0.970 | –0.970 | –2.095 | ns |
| | GCLK PLL | $t_{SU}$ | 2.517 | 2.517 | 5.480 | ns |
| | | $t_H$ | –2.412 | –2.412 | –5.203 | ns |

## EP1AGX35 I/O Timing Parameters

Table 4–54 through Table 4–57 list the maximum I/O timing parameters for EP1AGX35 devices for I/O standards which support general purpose I/O pins.

Table 4–54 lists I/O timing specifications.

**Table 4–54.** EP1AGX35 Row Pins Input Timing Parameters (Part 1 of 2)

| I/O Standard | Clock | Parameter | Fast Model | | –6 Speed Grade | Units |
|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | | |
| 3.3-V LVTTL | GCLK | $t_{SU}$ | 1.561 | 1.561 | 3.556 | ns |
| | | $t_H$ | –1.456 | –1.456 | –3.279 | ns |
| | GCLK PLL | $t_{SU}$ | 2.980 | 2.980 | 6.628 | ns |
| | | $t_H$ | –2.875 | –2.875 | –6.351 | ns |
| 3.3-V LVCMOS | GCLK | $t_{SU}$ | 1.561 | 1.561 | 3.556 | ns |
| | | $t_H$ | –1.456 | –1.456 | –3.279 | ns |
| | GCLK PLL | $t_{SU}$ | 2.980 | 2.980 | 6.628 | ns |
| | | $t_H$ | –2.875 | –2.875 | –6.351 | ns |
| 2.5 V | GCLK | $t_{SU}$ | 1.573 | 1.573 | 3.537 | ns |
| | | $t_H$ | –1.468 | –1.468 | –3.260 | ns |
| | GCLK PLL | $t_{SU}$ | 2.992 | 2.992 | 6.609 | ns |
| | | $t_H$ | –2.887 | –2.887 | –6.332 | ns |
| 1.8 V | GCLK | $t_{SU}$ | 1.639 | 1.639 | 3.744 | ns |
| | | $t_H$ | –1.534 | –1.534 | –3.467 | ns |
| | GCLK PLL | $t_{SU}$ | 3.058 | 3.058 | 6.816 | ns |
| | | $t_H$ | –2.953 | –2.953 | –6.539 | ns |
| 1.5 V | GCLK | $t_{SU}$ | 1.642 | 1.642 | 3.839 | ns |
| | | $t_H$ | –1.537 | –1.537 | –3.562 | ns |
| | GCLK PLL | $t_{SU}$ | 3.061 | 3.061 | 6.911 | ns |
| | | $t_H$ | –2.956 | –2.956 | –6.634 | ns |
| SSTL-2 CLASS I | GCLK | $t_{SU}$ | 1.385 | 1.385 | 3.009 | ns |
| | | $t_H$ | –1.280 | –1.280 | –2.732 | ns |
| | GCLK PLL | $t_{SU}$ | 2.804 | 2.804 | 6.081 | ns |
| | | $t_H$ | –2.699 | –2.699 | –5.804 | ns |
| SSTL-2 CLASS II | GCLK | $t_{SU}$ | 1.385 | 1.385 | 3.009 | ns |
| | | $t_H$ | –1.280 | –1.280 | –2.732 | ns |
| | GCLK PLL | $t_{SU}$ | 2.804 | 2.804 | 6.081 | ns |
| | | $t_H$ | –2.699 | –2.699 | –5.804 | ns |
| SSTL-18 CLASS I | GCLK | $t_{SU}$ | 1.417 | 1.417 | 3.118 | ns |
| | | $t_H$ | –1.312 | –1.312 | –2.841 | ns |
| | GCLK PLL | $t_{SU}$ | 2.836 | 2.836 | 6.190 | ns |
| | | $t_H$ | –2.731 | –2.731 | –5.913 | ns |

**Table 4–62.** EP1AGX50 Row Pins Output Timing Parameters (Part 2 of 3)

| I/O Standard | Drive Strength | Clock | Parameter | Fast Model | | –6 Speed Grade | Units |
|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | | |
| 3.3-V LVTTL | 12 mA | GCLK | $t_{CO}$ | 2.731 | 2.731 | 6.036 | ns |
| | | GCLK PLL | $t_{CO}$ | 1.303 | 1.303 | 2.952 | ns |
| 3.3-V LVCMOS | 4 mA | GCLK | $t_{CO}$ | 2.787 | 2.787 | 6.073 | ns |
| | | GCLK PLL | $t_{CO}$ | 1.359 | 1.359 | 2.989 | ns |
| 3.3-V LVCMOS | 8 mA | GCLK | $t_{CO}$ | 2.681 | 2.681 | 5.767 | ns |
| | | GCLK PLL | $t_{CO}$ | 1.253 | 1.253 | 2.683 | ns |
| 2.5 V | 4 mA | GCLK | $t_{CO}$ | 2.770 | 2.770 | 6.047 | ns |
| | | GCLK PLL | $t_{CO}$ | 1.342 | 1.342 | 2.963 | ns |
| 2.5 V | 8 mA | GCLK | $t_{CO}$ | 2.667 | 2.667 | 5.789 | ns |
| | | GCLK PLL | $t_{CO}$ | 1.239 | 1.239 | 2.705 | ns |
| 2.5 V | 12 mA | GCLK | $t_{CO}$ | 2.648 | 2.648 | 5.675 | ns |
| | | GCLK PLL | $t_{CO}$ | 1.220 | 1.220 | 2.591 | ns |
| 1.8 V | 2 mA | GCLK | $t_{CO}$ | 2.840 | 2.840 | 7.066 | ns |
| | | GCLK PLL | $t_{CO}$ | 1.412 | 1.412 | 3.982 | ns |
| 1.8 V | 4 mA | GCLK | $t_{CO}$ | 2.829 | 2.829 | 6.287 | ns |
| | | GCLK PLL | $t_{CO}$ | 1.401 | 1.401 | 3.203 | ns |
| 1.8 V | 6 mA | GCLK | $t_{CO}$ | 2.718 | 2.718 | 5.986 | ns |
| | | GCLK PLL | $t_{CO}$ | 1.290 | 1.290 | 2.902 | ns |
| 1.8 V | 8 mA | GCLK | $t_{CO}$ | 2.687 | 2.687 | 5.872 | ns |
| | | GCLK PLL | $t_{CO}$ | 1.259 | 1.259 | 2.788 | ns |
| 1.5 V | 2 mA | GCLK | $t_{CO}$ | 2.800 | 2.800 | 6.565 | ns |
| | | GCLK PLL | $t_{CO}$ | 1.372 | 1.372 | 3.481 | ns |
| 1.5 V | 4 mA | GCLK | $t_{CO}$ | 2.693 | 2.693 | 5.964 | ns |
| | | GCLK PLL | $t_{CO}$ | 1.265 | 1.265 | 2.880 | ns |
| SSTL-2 CLASS I | 8 mA | GCLK | $t_{CO}$ | 2.636 | 2.636 | 5.626 | ns |
| | | GCLK PLL | $t_{CO}$ | 1.209 | 1.209 | 2.544 | ns |
| SSTL-2 CLASS I | 12 mA | GCLK | $t_{CO}$ | 2.612 | 2.612 | 5.550 | ns |
| | | GCLK PLL | $t_{CO}$ | 1.185 | 1.185 | 2.468 | ns |
| SSTL-2 CLASS II | 16 mA | GCLK | $t_{CO}$ | 2.578 | 2.578 | 5.419 | ns |
| | | GCLK PLL | $t_{CO}$ | 1.151 | 1.151 | 2.337 | ns |
| SSTL-18 CLASS I | 4 mA | GCLK | $t_{CO}$ | 2.625 | 2.625 | 5.570 | ns |
| | | GCLK PLL | $t_{CO}$ | 1.197 | 1.197 | 2.486 | ns |
| SSTL-18 CLASS I | 6 mA | GCLK | $t_{CO}$ | 2.628 | 2.628 | 5.497 | ns |
| | | GCLK PLL | $t_{CO}$ | 1.201 | 1.201 | 2.415 | ns |
| SSTL-18 CLASS I | 8 mA | GCLK | $t_{CO}$ | 2.604 | 2.604 | 5.480 | ns |
| | | GCLK PLL | $t_{CO}$ | 1.177 | 1.177 | 2.398 | ns |
| SSTL-18 CLASS I | 10 mA | GCLK | $t_{CO}$ | 2.607 | 2.607 | 5.459 | ns |
| | | GCLK PLL | $t_{CO}$ | 1.180 | 1.180 | 2.377 | ns |

**Table 4–66.** EP1AGX60 Row Pins Input Timing Parameters (Part 3 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | –6 Speed Grade | Units |
|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | | |
| 1.5-V HSTL CLASS II | GCLK | $t_{SU}$ | 1.281 | 1.281 | 2.777 | ns |
| | | $t_H$ | –1.176 | –1.176 | –2.500 | ns |
| | GCLK PLL | $t_{SU}$ | 2.853 | 2.853 | 6.220 | ns |
| | | $t_H$ | –2.748 | –2.748 | –5.943 | ns |
| LVDS | GCLK | $t_{SU}$ | 1.208 | 1.208 | 2.664 | ns |
| | | $t_H$ | –1.103 | –1.103 | –2.387 | ns |
| | GCLK PLL | $t_{SU}$ | 2.767 | 2.767 | 6.083 | ns |
| | | $t_H$ | –2.662 | –2.662 | –5.806 | ns |

Table 4–67 lists I/O timing specifications.

**Table 4–67.** EP1AGX60 Column Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Corner | | –6 Speed Grade | Units |
|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | | |
| 3.3-V LVTTL | GCLK | $t_{SU}$ | 1.124 | 1.124 | 2.493 | ns |
| | | $t_H$ | –1.019 | –1.019 | -2.216 | ns |
| | GCLK PLL | $t_{SU}$ | 2.694 | 2.694 | 5.928 | ns |
| | | $t_H$ | –2.589 | –2.589 | -5.651 | ns |
| 3.3-V LVCMOS | GCLK | $t_{SU}$ | 1.124 | 1.124 | 2.493 | ns |
| | | $t_H$ | –1.019 | –1.019 | -2.216 | ns |
| | GCLK PLL | $t_{SU}$ | 2.694 | 2.694 | 5.928 | ns |
| | | $t_H$ | –2.589 | –2.589 | -5.651 | ns |
| 2.5 V | GCLK | $t_{SU}$ | 1.134 | 1.134 | 2.475 | ns |
| | | $t_H$ | –1.029 | –1.029 | -2.198 | ns |
| | GCLK PLL | $t_{SU}$ | 2.704 | 2.704 | 5.910 | ns |
| | | $t_H$ | –2.599 | –2.599 | -5.633 | ns |
| 1.8 V | GCLK | $t_{SU}$ | 1.200 | 1.200 | 2.685 | ns |
| | | $t_H$ | –1.095 | –1.095 | -2.408 | ns |
| | GCLK PLL | $t_{SU}$ | 2.770 | 2.770 | 6.120 | ns |
| | | $t_H$ | –2.665 | –2.665 | -5.843 | ns |
| 1.5 V | GCLK | $t_{SU}$ | 1.203 | 1.203 | 2.778 | ns |
| | | $t_H$ | –1.098 | –1.098 | -2.501 | ns |
| | GCLK PLL | $t_{SU}$ | 2.773 | 2.773 | 6.213 | ns |
| | | $t_H$ | –2.668 | –2.668 | -5.936 | ns |
| SSTL-2 CLASS I | GCLK | $t_{SU}$ | 0.948 | 0.948 | 1.951 | ns |
| | | $t_H$ | –0.843 | –0.843 | -1.674 | ns |
| | GCLK PLL | $t_{SU}$ | 2.519 | 2.519 | 5.388 | ns |
| | | $t_H$ | –2.414 | –2.414 | -5.111 | ns |

**Table 4–69.** EP1AGX60 Column Pins Output Timing Parameters (Part 4 of 4)

| I/O Standard | Drive Strength | Clock | Parameter | Fast Corner | | –6 Speed Grade | Units |
|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | | |
| 3.3-V PCI | — | GCLK | $t_{CO}$ | 2.882 | 2.882 | 6.213 | ns |
| | | GCLK PLL | $t_{CO}$ | 1.312 | 1.312 | 2.778 | ns |
| 3.3-V PCI-X | — | GCLK | $t_{CO}$ | 2.882 | 2.882 | 6.213 | ns |
| | | GCLK PLL | $t_{CO}$ | 1.312 | 1.312 | 2.778 | ns |
| LVDS | — | GCLK | $t_{CO}$ | 3.746 | 3.746 | 7.396 | ns |
| | | GCLK PLL | $t_{CO}$ | 2.185 | 2.185 | 3.973 | ns |

Table 4–70 through Table 4–71 list EP1AGX60 regional clock (RCLK) adder values that should be added to the GCLK values. These adder values are used to determine I/O timing when the I/O pin is driven using the regional clock. This applies for all I/O standards supported by Arria GX with general purpose I/O pins.

Table 4–70 describes row pin delay adders when using the regional clock in Arria GX devices.

**Table 4–70.** EP1AGX60 Row Pin Delay Adders for Regional Clock

| Parameter | Fast Corner | | –6 Speed Grade | Units |
|---|---|---|---|---|
| | Industrial | Commercial | | |
| RCLK input adder | 0.138 | 0.138 | 0.311 | ns |
| RCLK PLL input adder | –0.003 | –0.003 | –0.006 | ns |
| RCLK output adder | –0.138 | –0.138 | –0.311 | ns |
| RCLK PLL output adder | 0.003 | 0.003 | 0.006 | ns |

Table 4–71 lists column pin delay adders when using the regional clock in Arria GX devices.

**Table 4–71.** EP1AGX60 Column Pin Delay Adders for Regional Clock

| Parameter | Fast Corner | | –6 Speed Grade | Units |
|---|---|---|---|---|
| | Industrial | Commercial | | |
| RCLK input adder | 0.153 | 0.153 | 0.344 | ns |
| RCLK PLL input adder | –1.066 | –1.066 | –2.338 | ns |
| RCLK output adder | –0.153 | –0.153 | –0.343 | ns |
| RCLK PLL output adder | 1.721 | 1.721 | 4.486 | ns |

## EP1AGX90 I/O Timing Parameters

Table 4–72 through Table 4–75 list the maximum I/O timing parameters for EP1AGX90 devices for I/O standards which support general purpose I/O pins.

**Table 4–72.** EP1AGX90 Row Pins Input Timing Parameters (Part 2 of 2)

| I/O Standard | Clock | Parameter | Fast Model | | –6 Speed Grade | Units |
|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | | |
| 1.8-V HSTL CLASS I | GCLK | $t_{SU}$ | 1.159 | 1.159 | 2.447 | ns |
| | | $t_H$ | –1.054 | –1.054 | –2.170 | ns |
| | GCLK PLL | $t_{SU}$ | 3.212 | 3.212 | 6.565 | ns |
| | | $t_H$ | –3.107 | –3.107 | –6.288 | ns |
| 1.8-V HSTL CLASS II | GCLK | $t_{SU}$ | 1.157 | 1.157 | 2.441 | ns |
| | | $t_H$ | –1.052 | –1.052 | –2.164 | ns |
| | GCLK PLL | $t_{SU}$ | 3.235 | 3.235 | 6.597 | ns |
| | | $t_H$ | –3.130 | –3.130 | –6.320 | ns |
| 1.5-V HSTL CLASS I | GCLK | $t_{SU}$ | 1.185 | 1.185 | 2.575 | ns |
| | | $t_H$ | –1.080 | –1.080 | –2.298 | ns |
| | GCLK PLL | $t_{SU}$ | 3.238 | 3.238 | 6.693 | ns |
| | | $t_H$ | –3.133 | –3.133 | –6.416 | ns |
| 1.5-V HSTL CLASS II | GCLK | $t_{SU}$ | 1.183 | 1.183 | 2.569 | ns |
| | | $t_H$ | –1.078 | –1.078 | –2.292 | ns |
| | GCLK PLL | $t_{SU}$ | 3.261 | 3.261 | 6.725 | ns |
| | | $t_H$ | –3.156 | –3.156 | –6.448 | ns |
| LVDS | GCLK | $t_{SU}$ | 1.098 | 1.098 | 2.439 | ns |
| | | $t_H$ | –0.993 | –0.993 | –2.162 | ns |
| | GCLK PLL | $t_{SU}$ | 3.160 | 3.160 | 6.566 | ns |
| | | $t_H$ | –3.055 | –3.055 | –6.289 | ns |

Table 4–73 lists I/O timing specifications.

**Table 4–73.** EP1AGX90 Column Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Corner | | –6 Speed Grade | Units |
|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | | |
| 3.3-V LVTTL | GCLK | $t_{SU}$ | 1.018 | 1.018 | 2.290 | ns |
| | | $t_H$ | –0.913 | –0.913 | –2.013 | ns |
| | GCLK PLL | $t_{SU}$ | 3.082 | 3.082 | 6.425 | ns |
| | | $t_H$ | –2.977 | –2.977 | –6.148 | ns |
| 3.3-V LVCMOS | GCLK | $t_{SU}$ | 1.018 | 1.018 | 2.290 | ns |
| | | $t_H$ | –0.913 | –0.913 | –2.013 | ns |
| | GCLK PLL | $t_{SU}$ | 3.082 | 3.082 | 6.425 | ns |
| | | $t_H$ | –2.977 | –2.977 | –6.148 | ns |
| 2.5 V | GCLK | $t_{SU}$ | 1.028 | 1.028 | 2.272 | ns |
| | | $t_H$ | –0.923 | –0.923 | –1.995 | ns |
| | GCLK PLL | $t_{SU}$ | 3.092 | 3.092 | 6.407 | ns |
| | | $t_H$ | –2.987 | –2.987 | –6.130 | ns |

**Table 4–74.** EP1AGX90 Row Pins Output Timing Parameters (Part 2 of 3)

| I/O Standard | Drive Strength | Clock | Parameter | Fast Model | | –6 Speed Grade | Units |
|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | | |
| 1.8 V | 2 mA | GCLK | $t_{CO}$ | 3.087 | 3.087 | 7.723 | ns |
| | | GCLK PLL | $t_{CO}$ | 1.034 | 1.034 | 3.605 | ns |
| 1.8 V | 4 mA | GCLK | $t_{CO}$ | 3.076 | 3.076 | 6.944 | ns |
| | | GCLK PLL | $t_{CO}$ | 1.023 | 1.023 | 2.826 | ns |
| 1.8 V | 6 mA | GCLK | $t_{CO}$ | 2.965 | 2.965 | 6.643 | ns |
| | | GCLK PLL | $t_{CO}$ | 0.912 | 0.912 | 2.525 | ns |
| 1.8 V | 8 mA | GCLK | $t_{CO}$ | 2.934 | 2.934 | 6.529 | ns |
| | | GCLK PLL | $t_{CO}$ | 0.881 | 0.881 | 2.411 | ns |
| 1.5 V | 2 mA | GCLK | $t_{CO}$ | 3.047 | 3.047 | 7.222 | ns |
| | | GCLK PLL | $t_{CO}$ | 0.994 | 0.994 | 3.104 | ns |
| 1.5 V | 4 mA | GCLK | $t_{CO}$ | 2.940 | 2.940 | 6.621 | ns |
| | | GCLK PLL | $t_{CO}$ | 0.887 | 0.887 | 2.503 | ns |
| SSTL-2 CLASS I | 8 mA | GCLK | $t_{CO}$ | 2.890 | 2.890 | 6.294 | ns |
| | | GCLK PLL | $t_{CO}$ | 0.824 | 0.824 | 2.157 | ns |
| SSTL-2 CLASS I | 12 mA | GCLK | $t_{CO}$ | 2.866 | 2.866 | 6.218 | ns |
| | | GCLK PLL | $t_{CO}$ | 0.800 | 0.800 | 2.081 | ns |
| SSTL-2 CLASS II | 16 mA | GCLK | $t_{CO}$ | 2.832 | 2.832 | 6.087 | ns |
| | | GCLK PLL | $t_{CO}$ | 0.766 | 0.766 | 1.950 | ns |
| SSTL-18 CLASS I | 4 mA | GCLK | $t_{CO}$ | 2.872 | 2.872 | 6.227 | ns |
| | | GCLK PLL | $t_{CO}$ | 0.819 | 0.819 | 2.109 | ns |
| SSTL-18 CLASS I | 6 mA | GCLK | $t_{CO}$ | 2.878 | 2.878 | 6.162 | ns |
| | | GCLK PLL | $t_{CO}$ | 0.800 | 0.800 | 2.006 | ns |
| SSTL-18 CLASS I | 8 mA | GCLK | $t_{CO}$ | 2.854 | 2.854 | 6.145 | ns |
| | | GCLK PLL | $t_{CO}$ | 0.776 | 0.776 | 1.989 | ns |
| SSTL-18 CLASS I | 10 mA | GCLK | $t_{CO}$ | 2.857 | 2.857 | 6.124 | ns |
| | | GCLK PLL | $t_{CO}$ | 0.779 | 0.779 | 1.968 | ns |
| 1.8-V HSTL CLASS I | 4 mA | GCLK | $t_{CO}$ | 2.853 | 2.853 | 6.137 | ns |
| | | GCLK PLL | $t_{CO}$ | 0.800 | 0.800 | 2.019 | ns |
| 1.8-V HSTL CLASS I | 6 mA | GCLK | $t_{CO}$ | 2.858 | 2.858 | 6.107 | ns |
| | | GCLK PLL | $t_{CO}$ | 0.780 | 0.780 | 1.951 | ns |
| 1.8-V HSTL CLASS I | 8 mA | GCLK | $t_{CO}$ | 2.840 | 2.840 | 6.103 | ns |
| | | GCLK PLL | $t_{CO}$ | 0.762 | 0.762 | 1.947 | ns |
| 1.8-V HSTL CLASS I | 10 mA | GCLK | $t_{CO}$ | 2.844 | 2.844 | 6.092 | ns |
| | | GCLK PLL | $t_{CO}$ | 0.766 | 0.766 | 1.936 | ns |
| 1.8-V HSTL CLASS I | 12 mA | GCLK | $t_{CO}$ | 2.835 | 2.835 | 6.091 | ns |
| | | GCLK PLL | $t_{CO}$ | 0.757 | 0.757 | 1.935 | ns |
| 1.5-V HSTL CLASS I | 4 mA | GCLK | $t_{CO}$ | 2.852 | 2.852 | 6.114 | ns |
| | | GCLK PLL | $t_{CO}$ | 0.799 | 0.799 | 1.996 | ns |

Table 4–90 lists clock timing specifications.

**Table 4–90.** EP1AGX50 Row Pins Regional Clock Timing Parameters

| Parameter | Fast Model | | –6 Speed Grade | Units |
|---|---|---|---|---|
| | Industrial | Commercial | | |
| $t_{CIN}$ | 1.653 | 1.653 | 3.841 | ns |
| $t_{COUT}$ | 1.651 | 1.651 | 3.839 | ns |
| $t_{PLLCIN}$ | 0.245 | 0.245 | 0.755 | ns |
| $t_{PLLCOUT}$ | 0.245 | 0.245 | 0.755 | ns |

## EP1AGX60 Clock Timing Parameters

Table 4–91 to Table 4–92 on page 4–82 list the GCLK clock timing parameters for EP1AGX60 devices.

Table 4–91 lists clock timing specifications.

**Table 4–91.** EP1AGX60 Row Pins Global Clock Timing Parameters

| Parameter | Fast Model | | –6 Speed Grade | Units |
|---|---|---|---|---|
| | Industrial | Commercial | | |
| $t_{CIN}$ | 1.531 | 1.531 | 3.593 | ns |
| $t_{COUT}$ | 1.536 | 1.536 | 3.587 | ns |
| $t_{PLLCIN}$ | –0.023 | –0.023 | 0.188 | ns |
| $t_{PLLCOUT}$ | –0.018 | –0.018 | 0.182 | ns |

Table 4–92 lists clock timing specifications.

**Table 4–92.** EP1AGX60 Row Pins Global Clock Timing Parameters

| Parameter | Fast Model | | –6 Speed Grade | Units |
|---|---|---|---|---|
| | Industrial | Commercial | | |
| $t_{CIN}$ | 1.792 | 1.792 | 4.165 | ns |
| $t_{COUT}$ | 1.792 | 1.792 | 4.165 | ns |
| $t_{PLLCIN}$ | 0.238 | 0.238 | 0.758 | ns |
| $t_{PLLCOUT}$ | 0.238 | 0.238 | 0.758 | ns |

**Figure 4–12.** DCD Measurement Technique for DDIO (Double-Data Rate) Outputs

When an FPGA PLL generates the internal clock, the PLL output clocks the IOE block. As the PLL only monitors the positive edge of the reference clock input and internally re-creates the output clock signal, any DCD present on the reference clock is filtered out. Therefore, the DCD for a DDIO output with PLL in the clock path is better than the DCD for a DDIO output without PLL in the clock path.

Table 4–108 through Table 4–113 show the maximum DCD in absolution derivation for different I/O standards on Arria GX devices. Examples are also provided that show how to calculate DCD as a percentage.

**Table 4–108.** Maximum DCD for Non-DDIO Output on Row I/O Pins

| Row I/O Output Standard | Maximum DCD (ps) for Non-DDIO Output | |
|---|---|---|
| | –6 Speed Grade | Units |
| 3.3-V LVTTTL | 275 | ps |
| 3.3-V LVCMOS | 155 | ps |
| 2.5 V | 135 | ps |
| 1.8 V | 180 | ps |
| 1.5-V LVCMOS | 195 | ps |
| SSTL-2 Class I | 145 | ps |
| SSTL-2 Class II | 125 | ps |
| SSTL-18 Class I | 85 | ps |
| 1.8-V HSTL Class I | 100 | ps |
| 1.5-V HSTL Class I | 115 | ps |
| LVDS | 80 | ps |

Here is an example for calculating the DCD as a percentage for a non-DDIO output on a row I/O:

If the non-DDIO output I/O standard is SSTL-2 Class II, the maximum DCD is 125 ps (see Table 4–109). If the clock frequency is 267 MHz, the clock period T is:

$T = 1/ f = 1 / 267 \text{ MHz} = 3.745 \text{ ns} = 3{,}745 \text{ ps}$

# Document Revision History

Table 4–124 lists the revision history for this chapter.

**Table 4–124.** Document Revision History

| Date and Document Version | Changes Made | Summary of Changes |
|---|---|---|
| December 2009, v2.0 | ■ Updated Table 4–104, Table 4–105, and Table 4–106.<br>■ Document template update.<br>■ Minor text edits. | — |
| April 2009<br>v1.4 | ■ Updated Table 4–6 and Table 4–7.<br>■ Updated “Maximum Input and Output Clock Toggle Rate” section. | — |
| May 2008<br>v1.3 | Updated:<br>■ Table 4–5<br>■ Table 4–7<br>■ Table 4–8<br>■ Table 4–9<br>■ Table 4–10<br>■ Table 4–11<br>■ Table 4–12<br>■ Table 4–13<br>■ Table 4–14<br>■ Table 4–15<br>■ Table 4–16<br>■ Table 4–17<br>■ Table 4–43<br>■ Table 4–116<br>■ Table 4–117 | — |
| | Updated:<br>■ Figure 4–4 | — |
| | Minor text edits. | — |
| August 2007 v1.2 | Removed “Preliminary” from each page. | — |
| | Removed “Preliminary” note from Tables 4–44, 4–45, and 4–47. | — |
| | Added “Referenced Documents” section. | — |
| June 2007<br>v1.1 | Updated Table 4–99. | — |
| | Added GIGE information. | — |
| May 2007<br>v1.0 | Initial release. | — |

| Visual Cue | Meaning |
|---|---|
| Courier type | Indicates signal, port, register, bit, block, and primitive names. For example, data1, tdi, and input. Active-low signals are denoted by suffix n. For example, resetn.<br>Indicates command line commands and anything that must be typed exactly as it appears. For example, c:\qdesigns\tutorial\chiptrip.gdf.<br>Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword SUBDESIGN), and logic function names (for example, TRI). |
| 1., 2., 3., and<br>a., b., c., and so on. | Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure. |
| ■ ■ | Bullets indicate a list of items when the sequence of the items is not important. |
| ☞ | The hand points to information that requires special attention. |
| CAUTION | A caution calls attention to a condition or possible situation that can damage or destroy the product or your work. |
| | A warning calls attention to a condition or possible situation that can cause you injury. |
| ↵ | The angled arrow instructs you to press **Enter**. |
| | The feet direct you to more information about a particular topic. |