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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

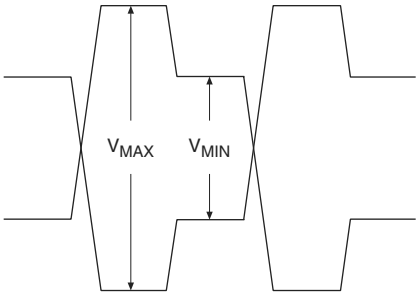
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4511
Number of Logic Elements/Cells	90220
Total RAM Bits	4477824
Number of I/O	538
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1agx90ef1152c6n

Programmable Pre-Emphasis

The programmable pre-emphasis module controls the output driver to boost high frequency components and compensate for losses in the transmission medium, as shown in Figure 2–10. Pre-emphasis is set statically using the ALTGXB megafunction.

Figure 2–10. Pre-Emphasis Signaling



$$\text{Pre-Emphasis \%} = \left(\frac{V_{MAX}}{V_{MIN}} - 1\right) \times 100$$

Pre-emphasis percentage is defined as $(V_{MAX}/V_{MIN} - 1) \times 100$, where V_{MAX} is the differential emphasized voltage (peak-to-peak) and V_{MIN} is the differential steady-state voltage (peak-to-peak).

PCI Express (PIPE) Receiver Detect

The Arria GX transmitter buffer has a built-in receiver detection circuit for use in PCI Express (PIPE) mode. This circuit provides the ability to detect if there is a receiver downstream by sending out a pulse on the channel and monitoring the reflection. This mode requires a tri-stated transmitter buffer (in electrical idle mode).

PCI Express (PIPE) Electric Idles (or Individual Transmitter Tri-State)

The Arria GX transmitter buffer supports PCI Express (PIPE) electrical idles. This feature is only active in PCI Express (PIPE) mode. The `tx_forceelecidle` port puts the transmitter buffer in electrical idle mode. This port is available in all PCI Express (PIPE) power-down modes and has specific usage in each mode.

Receiver Path

This section describes the data path through the Arria GX receiver. The sub-blocks are described in order from the receiver buffer to the PLD-receiver parallel interface.

Receiver Buffer

The Arria GX receiver input buffer supports the 1.2-V and 1.5-V PCML I/O standards at rates up to 3.125 Gbps. The common mode voltage of the receiver input buffer is programmable between 0.85 V and 1.2 V. You must select the 0.85 V common mode voltage for AC- and DC-coupled PCML links and 1.2 V common mode voltage for DC-coupled LVDS links.

Bit-Slip Mode

The word aligner can operate in either pattern detection mode or in bit-slip mode.

The bit-slip mode provides the option to manually shift the word boundary through the FPGA. This feature is useful for:

- Longer synchronization patterns than the pattern detector can accommodate
- Scrambled data stream
- Input stream consisting of over-sampled data

The word aligner outputs a word boundary as it is received from the analog receiver after reset. You can examine the word and search its boundary in the FPGA. To do so, assert the `rx_bitslip` signal. The `rx_bitslip` signal should be toggled and held constant for at least two FPGA clock cycles.

For every rising edge of the `rx_bitslip` signal, the current word boundary is slipped by one bit. Every time a bit is slipped, the bit received earliest is lost. If bit slipping shifts a complete round of bus width, the word boundary is back to the original boundary.

The `rx_syncstatus` signal is not available in bit-slipping mode.

Channel Aligner

The channel aligner is available only in XAUI mode and aligns the signals of all four channels within a transceiver. The channel aligner follows the IEEE 802.3ae, clause 48 specification for channel bonding.

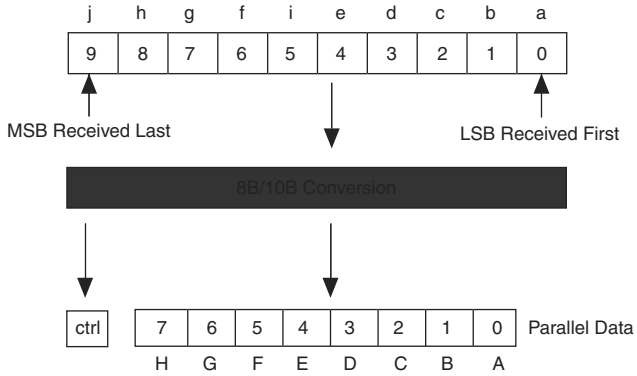
The channel aligner is a 16-word FIFO buffer with a state machine controlling the channel bonding process. The state machine looks for an /A/ (/K28.3/) in each channel and aligns all the /A/ code groups in the transceiver. When four columns of /A/ (denoted by //A//) are detected, the `rx_channelaligned` signal goes high, signifying that all the channels in the transceiver have been aligned. The reception of four consecutive misaligned /A/ code groups restarts the channel alignment sequence and sends the `rx_channelaligned` signal low.

8B/10B Decoder

The 8B/10B decoder is used in all supported functional modes. The 8B/10B decoder takes in 10-bit data from the rate matcher and decodes it into 8-bit data + 1-bit control identifier, thereby restoring the original transmitted data at the receiver. The 8B/10B decoder indicates whether the received 10-bit character is a data or control code through the `rx_ctrldetect` port. If the received 10-bit code group is a control character (`Kx.y`), the `rx_ctrldetect` signal is driven high and if it is a data character (`Dx.y`), the `rx_ctrldetect` signal is driven low.

Figure 2–17 shows a 10-bit code group decoded to an 8-bit data and a 1-bit control indicator.

Figure 2–17. 10-Bit to 8-Bit Conversion



If the received 10-bit code is not a part of valid Dx.y or Kx.y code groups, the 8B/10B decoder block asserts an error flag on the `rx_errdetect` port. If the received 10-bit code is detected with incorrect running disparity, the 8B/10B decoder block asserts an error flag on the `rx_disperr` and `rx_errdetect` ports. The error flag signals (`rx_errdetect` and `rx_disperr`) have the same data path delay from the 8B/10B decoder to the PLD-transceiver interface as the bad code group.

Receiver State Machine

The receiver state machine operates in Basic, GIGE, PCI Express (PIPE), and XAUI modes. In GIGE mode, the receiver state machine replaces invalid code groups with K30.7. In XAUI mode, the receiver state machine translates the XAUI PCS code group to the XAUI XGMII code group.

You can dynamically put the PCI Express (PIPE) mode transceiver in reverse parallel loopback by controlling the `tx_detectrxloopback` port instantiated in the MegaWizard Plug-In Manager. A high on the `tx_detectrxloopback` port in P0 power state puts the transceiver in reverse parallel loopback. A high on the `tx_detectrxloopback` port in any other power state does not put the transceiver in reverse parallel loopback.

As seen in Figure 2–21, the serial data received on the `rx_datain` port in reverse parallel loopback goes through the CRU, deserializer, word aligner, and the rate matcher blocks. The parallel data at the output of the receiver rate matcher block is looped back to the input of the transmitter serializer block. The serializer converts the parallel data to serial data and feeds it to the transmitter output buffer that drives the data out on the `tx_dataout` port. The data at the output of the rate matcher also goes through the 8B/10B decoder, byte deserializer, and receiver phase compensation FIFO before being fed to the PLD on the `rx_dataout` port.

Reset and Powerdown

Arria GX transceivers offer a power saving advantage with their ability to shut off functions that are not needed.

The following three reset signals are available per transceiver channel and can be used to individually reset the digital and analog portions within each channel:

- `tx_digitalreset`
- `rx_analogreset`
- `rx_digitalreset`

The following two powerdown signals are available per transceiver block and can be used to shut down an entire transceiver block that is not being used:

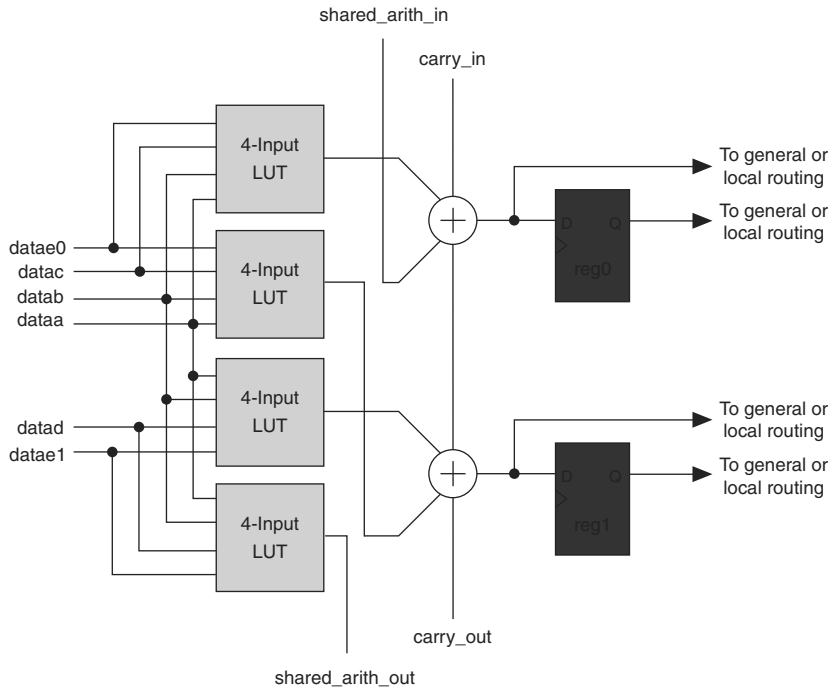
- `gxb_powerdown`
- `gxb_enable`

The other half of the ALMs in the LAB is available for implementing narrower fan-in functions in normal mode. Carry chains that use the top four ALMs in the first LAB carries into the top half of the ALMs in the next LAB within the column. Carry chains that use the bottom four ALMs in the first LAB carries into the bottom half of the ALMs in the next LAB within the column. Every other column of the LABs are top-half bypassable, while the other LAB columns are bottom-half bypassable. For more information about carry chain interconnect, refer to "MultiTrack Interconnect" on page 2–44.

Shared Arithmetic Mode

In shared arithmetic mode, the ALM can implement a three-input add. In this mode, the ALM is configured with four 4-input LUTs. Each LUT either computes the sum of three inputs or the carry of three inputs. The output of the carry computation is fed to the next adder (either to `adder1` in the same ALM or to `adder0` of the next ALM in the LAB) using a dedicated connection called the shared arithmetic chain. This shared arithmetic chain can significantly improve the performance of an adder tree by reducing the number of summation stages required to implement an adder tree. Figure 2–36 shows the ALM in shared arithmetic mode.

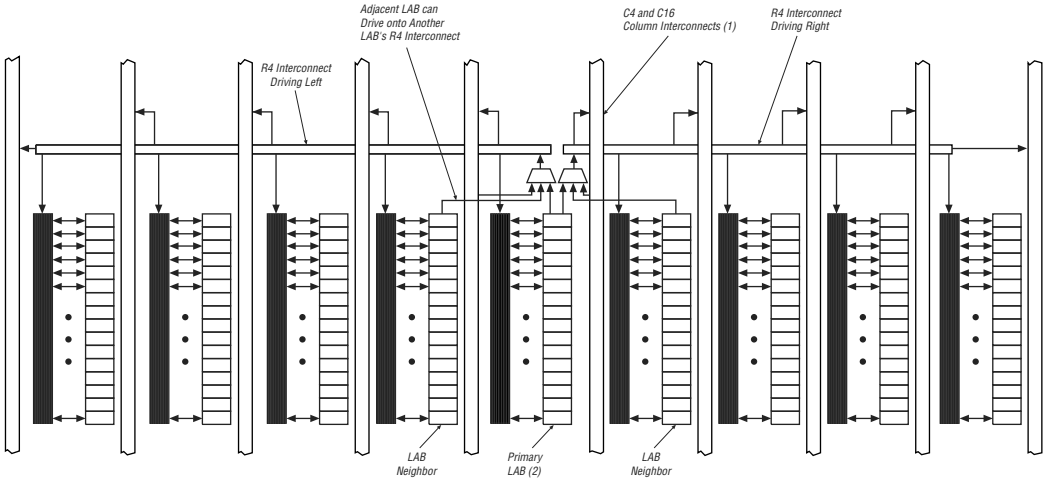
Figure 2–36. ALM in Shared Arithmetic Mode



Note to Figure 2–36:

(1) Inputs `dataf0` and `dataf1` are available for register packing in shared arithmetic mode.

Figure 2–39. R4 Interconnect Connections *(Note 1), (2), (3)*



Notes to Figure 2–39:

(1) C4 and C16 interconnects can drive R4 interconnects.

(2) This pattern is repeated for every LAB in the LAB row.

(3) The LABs in Figure 2–39 show the 16 possible logical outputs per LAB.

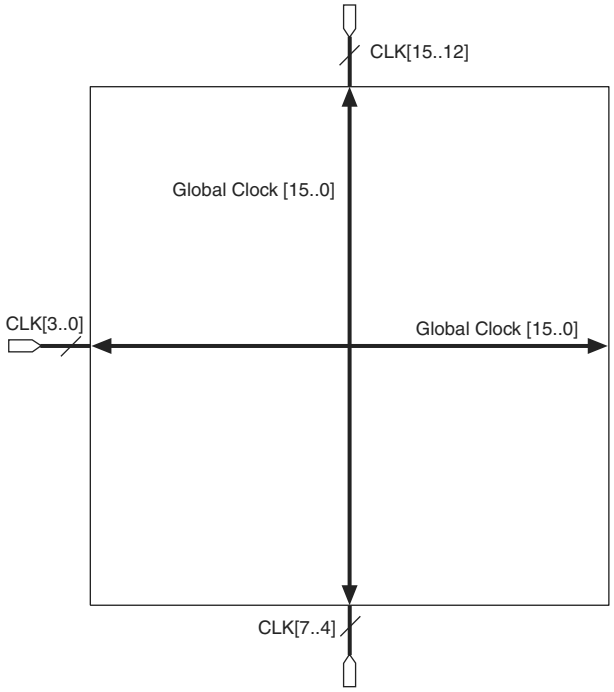
R24 row interconnects span 24 LABs and provide the fastest resource for long row connections between LABs, TriMatrix memory, DSP blocks, and row IOEs. The R24 row interconnects can cross M-RAM blocks. R24 row interconnects drive to other row or column interconnects at every fourth LAB and do not drive directly to LAB local interconnects. R24 row interconnects drive LAB local interconnects via R4 and C4 interconnects. R24 interconnects can drive R24, R4, C16, and C4 interconnects. The column interconnect operates similarly to the row interconnect and vertically routes signals to and from LABs, TriMatrix memory, DSP blocks, and IOEs. Each column of LABs is served by a dedicated column interconnect.

These column resources include:

- Shared arithmetic chain interconnects in a LAB
- Carry chain interconnects in a LAB and from LAB to LAB
- Register chain interconnects in a LAB
- C4 interconnects traversing a distance of four blocks in up and down direction
- C16 column interconnects for high-speed vertical routing through the device

Arria GX devices include an enhanced interconnect structure in LABs for routing shared arithmetic chains and carry chains for efficient arithmetic functions. The register chain connection allows the register output of one ALM to connect directly to the register input of the next ALM in the LAB for fast shift registers. These ALM-to-ALM connections bypass the local interconnect. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–40 shows shared arithmetic chain, carry chain, and register chain interconnects.

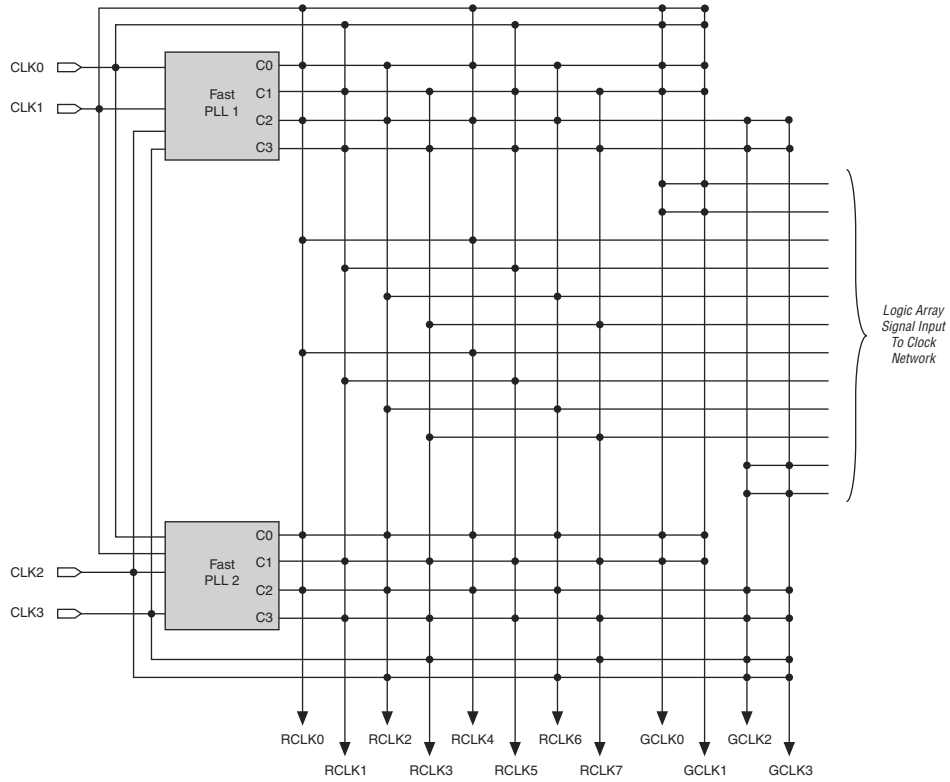
Figure 2–54. Global Clocking



Regional Clock Network

There are eight RCLK networks (RCLK[7..0]) in each quadrant of the Arria GX device that are driven by the dedicated CLK[15..12] and CLK[7..0] input pins, by PLL outputs, or by internal logic. The regional clock networks provide the lowest clock delay and skew for logic contained in a single quadrant. The CLK pins symmetrically drive the RCLK networks in a particular quadrant, as shown in Figure 2–55.

Figure 2–62. Global and Regional Clock Connections from Center Clock Pins and Fast PLL Outputs *(Note 1)*

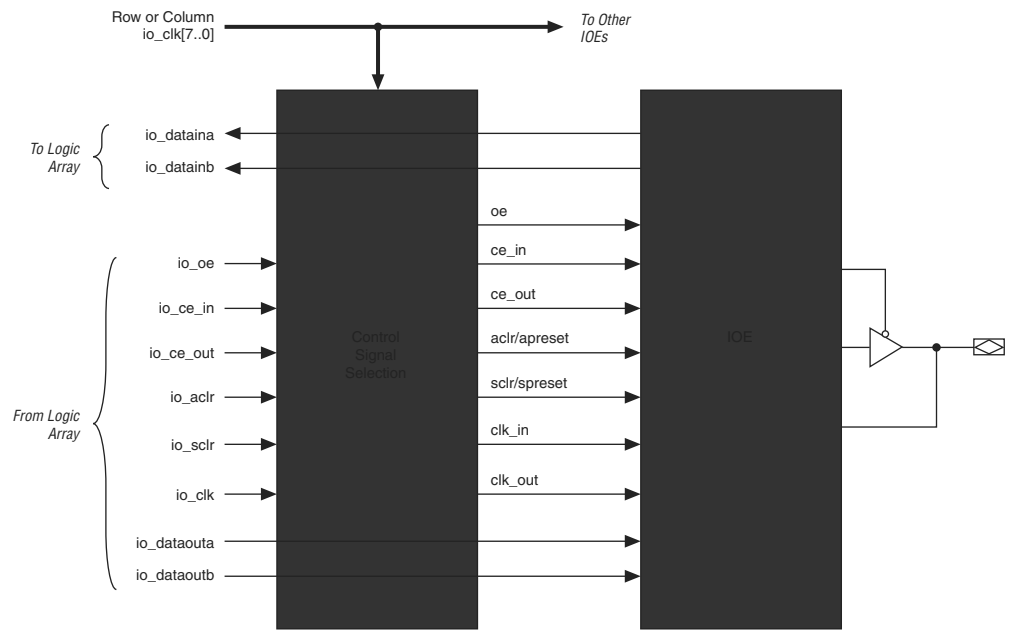


Note to Figure 2–62:

(1) The global or regional clocks in a fast PLL's quadrant can drive the fast PLL input. A dedicated clock input pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

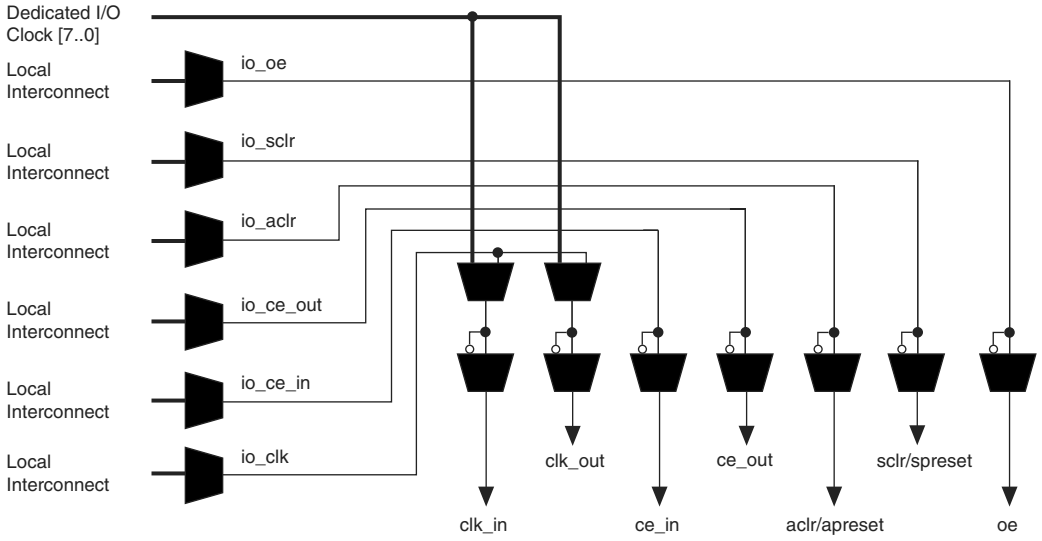
Figure 2–70 shows the signal paths through the I/O block.

Figure 2–70. Signal Path Through the I/O Block



Each IOE contains its own control signal selection for the following control signals: `oe`, `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, `clk_in`, and `clk_out`. Figure 2–71 shows the control signal selection.

Figure 2–71. Control Signal Selection per IOE *(Note 1)*



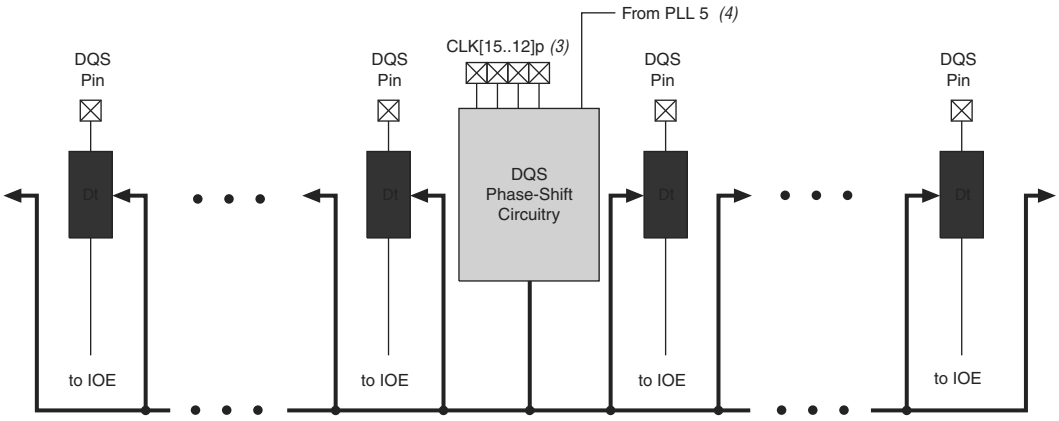
Notes to Figure 2–71:

(1) Control signals `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, and `oe` can be global signals even though their control selection multiplexers are not directly fed by the `ioe_clk[7..0]` signals. The `ioe_clk` signals can drive the I/O local interconnect, which then drives the control selection multiplexers.

The Arria GX device has two phase-shifting reference circuits, one on the top and one on the bottom of the device. The circuit on the top controls the compensated delay elements for all DQS pins on the top. The circuit on the bottom controls the compensated delay elements for all DQS pins on the bottom.

Each phase-shifting reference circuit is driven by a system reference clock, which must have the same frequency as the DQS signal. Clock pins `CLK[15..12]p` feed phase circuitry on the top of the device and clock pins `CLK[7..4]p` feed phase circuitry on the bottom of the device. In addition, PLL clock outputs can also feed the phase-shifting reference circuits. Figure 2–77 shows the phase-shift reference circuit control of each DQS delay shift on the top of the device. This same circuit is duplicated on the bottom of the device.

Figure 2–77. DQS Phase-Shift Circuitry *(Note 1)*, *(2)*



Notes to Figure 2–77:

(1) There are up to 18 pairs of DQS pins available on the top or bottom of the Arria GX device. There are up to 10 pairs on the right side and 8 pairs on the left side of the DQS phase-shift circuitry.

(2) The "t" module represents the DQS logic block.

(3) Clock pins `CLK[15..12]p` feed phase-shift circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase circuitry on the bottom of the device. You can also use a PLL clock output as a reference clock to phase shift circuitry.

(4) You can only use PLL 5 to feed the DQS phase-shift circuitry on the top of the device and PLL 6 to feed the DQS phase-shift circuitry on the bottom of the device.

These dedicated circuits combined with enhanced PLL clocking and phase-shift ability provide a complete hardware solution for interfacing to high-speed memory.

For more information about external memory interfaces, refer to the *External Memory Interfaces in Arria GX Devices* chapter.

Programmable Drive Strength

The output buffer for each Arria GX device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL, LVCMOS, SSTL, and HSTL standards have several levels of drive strength that you can control. The default setting used in the Quartus II software is the maximum current strength setting that is used to achieve maximum I/O performance. For all I/O standards, the minimum setting is the lowest drive strength that guarantees the I_{OH}/I_{OL} of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot.

Table 2–34. EP1AGX90 Device Differential Channels *(Note 1)*

Package	Transmitter/Receiver	Total Channels	Center Fast PLLs		Corner Fast PLLs
			PLL1	PLL2	PLL7
1,152-pin FineLine BGA	Transmitter	45	23	22	23
			22	23	—
	Receiver	47	23	24	23
			24	23	—

Note to Table 2–34:

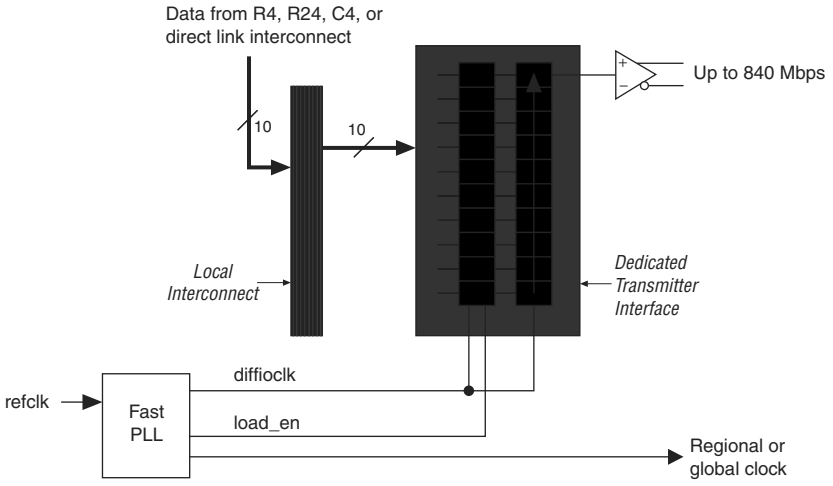
(1) The total number of receiver channels includes the four non-dedicated clock channels that can be optionally used as data channels.

Dedicated Circuitry with DPA Support

Arria GX devices support source-synchronous interfacing with LVDS signaling at up to 840 Mbps. Arria GX devices can transmit or receive serial channels along with a low-speed or high-speed clock.

The receiving device PLL multiplies the clock by an integer factor W = 1 through 32. The SERDES factor J determines the parallel data width to deserialize from receivers or to serialize for transmitters. The SERDES factor J can be set to 4, 5, 6, 7, 8, 9, or 10 and does not have to equal the PLL clock-multiplication W value. A design using the dynamic phase aligner also supports all of these J factor values. For a J factor of 1, the Arria GX device bypasses the SERDES block. For a J factor of 2, the Arria GX device bypasses the SERDES block, and the DDR input and output registers are used in the IOE. Figure 2–79 shows the block diagram of the Arria GX transmitter channel.

Figure 2–79. Arria GX Transmitter Channel



Each Arria GX receiver channel features a DPA block for phase detection and selection, a SERDES, a synchronizer, and a data realigner circuit. You can bypass the dynamic phase aligner without affecting the basic source-synchronous operation of the channel. In addition, you can dynamically switch between using the DPA block or bypassing the block via a control signal from the logic array.

Table 3–1. Arria GX JTAG Instructions

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer.
EXTEST *(1)*	00 0000 1111	Allows external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing IDCODE to be serially shifted out of TDO.
HIGHZ *(1)*	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP *(1)*	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions	—	Used when configuring an Arria GX device via the JTAG port with a USB-Blaster™, MasterBlaster™, ByteBlasterMV™, EthernetBlaster™, or ByteBlaster II download cable, or when using a **.jam** or **.jbc** via an embedded processor or JRunner™.
PULSE_NCONFIG	00 0000 0001	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.
CONFIG_IO *(2)*	00 0000 1101	Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, during, or after configuration. Stops configuration if executed during configuration. Once issued, the CONFIG_IO instruction holds nSTATUS low to reset the configuration device. nSTATUS is held low until the IOE configuration register is loaded and the TAP controller state machine transitions to the UPDATE_DR state.

Notes to Table 3–1:

(1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

(2) For more information about using the CONFIG_IO instruction, refer to the *MorphIO: An I/O Reconfiguration Solution for Altera Devices* White Paper.

For more information about Arria GX PLLs, refer to the *PLLs in Arria GX Devices* chapter.

Automated Single Event Upset (SEU) Detection

Arria GX devices offer on-chip circuitry for automated checking of single event upset (SEU) detection. Some applications that require the device to operate error free at high elevations or in close proximity to Earth's North or South Pole requires periodic checks to ensure continued data integrity. The error detection cyclic redundancy check (CRC) feature controlled by the **Device and Pin Options** dialog box in the Quartus II software uses a 32-bit CRC circuit to ensure data reliability and is one of the best options for mitigating SEU.

You can implement the error detection CRC feature with existing circuitry in Arria GX devices, eliminating the need for external logic. Arria GX devices compute CRC during configuration. The Arria GX device checks the computed-CRC against an automatically computed CRC during normal operation. The `CRC_ERROR` pin reports a soft error when configuration SRAM data is corrupted, triggering device reconfiguration.

Custom-Built Circuitry

Dedicated circuitry is built into Arria GX devices to automatically perform error detection. This circuitry constantly checks for errors in the configuration SRAM cells while the device is in user mode. You can monitor one external pin for the error and use it to trigger a reconfiguration cycle. You can select the desired time between checks by adjusting a built-in clock divider.

Software Interface

Beginning with version 7.1 of the Quartus II software, you can turn on the automated error detection CRC feature in the **Device and Pin Options** dialog box. This dialog box allows you to enable the feature and set the internal frequency of the CRC between 400 kHz to 50 MHz. This controls the rate that the CRC circuitry verifies the internal configuration SRAM bits in the Arria GX FPGA.

For more information about CRC, refer to *AN 357: Error Detection Using CRC in Altera FPGAs*.

AGX51004-2.0

Operating Conditions

Arria® GX devices are offered in both commercial and industrial grades. Both commercial and industrial devices are offered in –6 speed grade only.

This chapter contains the following sections:

Table 4–1 through Table 4–42 on page 4–25 provide information on absolute maximum ratings, recommended operating conditions, DC electrical characteristics, and other specifications for Arria GX devices.

Absolute Maximum Ratings

Table 4–1 contains the absolute maximum ratings for the Arria GX device family.

Table 4–1. Arria GX Device Absolute Maximum Ratings *(Note 1)*, *(2)*, *(3)* (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCINT}	Supply voltage	With respect to ground	–0.5	1.8	V
V_{CCIO}	Supply voltage	With respect to ground	–0.5	4.6	V
V_{CCPD}	Supply voltage	With respect to ground	–0.5	4.6	V
V_I	DC input voltage *(4)*	—	–0.5	4.6	V
I_{OUT}	DC output current, per pin	—	–25	40	mA
T_{STG}	Storage temperature	No bias	–65	150	C

Table 4–51. EP1AGX20 Column Pins Output Timing Parameters (Part 4 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V PCI	—	GCLK	t_{CO}	2.755	2.755	5.791	ns
		GCLK PLL	t_{CO}	1.313	1.313	2.685	ns
3.3-V PCI-X	—	GCLK	t_{CO}	2.755	2.755	5.791	ns
		GCLK PLL	t_{CO}	1.313	1.313	2.685	ns
LVDS	—	GCLK	t_{CO}	3.621	3.621	6.969	ns
		GCLK PLL	t_{CO}	2.190	2.190	3.880	ns

Table 4–52 through Table 4–53 list EP1AGX20 regional clock (RCLK) adder values that should be added to GCLK values. These adder values are used to determine I/O timing when the I/O pin is driven using the regional clock. This applies for all I/O standards supported by Arria GX with general purpose I/O pins.

Table 4–52 describes row pin delay adders when using the regional clock in Arria GX devices.

Table 4–52. EP1AGX20 Row Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.117	0.117	0.273	ns
RCLK PLL input adder	0.011	0.011	0.019	ns
RCLK output adder	–0.117	–0.117	–0.273	ns
RCLK PLL output adder	–0.011	–0.011	–0.019	ns

Table 4–53 lists column pin delay adders when using the regional clock in Arria GX devices.

Table 4–53. EP1AGX20 Column Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.081	0.081	0.223	ns
RCLK PLL input adder	–0.012	–0.012	–0.008	ns
RCLK output adder	–0.081	–0.081	–0.224	ns
RCLK PLL output adder	1.11	1.11	2.658	ns

Table 4–54. EP1AGX35 Row Pins Input Timing Parameters (Part 2 of 2)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
SSTL-18 CLASS II	GCLK	t_{SU}	1.417	1.417	3.118	ns
		t_H	–1.312	–1.312	–2.841	ns
	GCLK PLL	t_{SU}	2.836	2.836	6.190	ns
		t_H	–2.731	–2.731	–5.913	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	1.417	1.417	3.118	ns
		t_H	–1.312	–1.312	–2.841	ns
	GCLK PLL	t_{SU}	2.836	2.836	6.190	ns
		t_H	–2.731	–2.731	–5.913	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	1.417	1.417	3.118	ns
		t_H	–1.312	–1.312	–2.841	ns
	GCLK PLL	t_{SU}	2.836	2.836	6.190	ns
		t_H	–2.731	–2.731	–5.913	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.443	1.443	3.246	ns
		t_H	–1.338	–1.338	–2.969	ns
	GCLK PLL	t_{SU}	2.862	2.862	6.318	ns
		t_H	–2.757	–2.757	–6.041	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.443	1.443	3.246	ns
		t_H	–1.338	–1.338	–2.969	ns
	GCLK PLL	t_{SU}	2.862	2.862	6.318	ns
		t_H	–2.757	–2.757	–6.041	ns
LVDS	GCLK	t_{SU}	1.341	1.341	3.088	ns
		t_H	–1.236	–1.236	–2.811	ns
	GCLK PLL	t_{SU}	2.769	2.769	6.171	ns
		t_H	–2.664	–2.664	–5.894	ns

Table 4–55 lists I/O timing specifications.

Table 4–55. EP1AGX35 Column Pins Input Timing Parameters (Part 1 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.251	1.251	2.915	ns
		t_H	–1.146	–1.146	–2.638	ns
	GCLK PLL	t_{SU}	2.693	2.693	6.021	ns
		t_H	–2.588	–2.588	–5.744	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.251	1.251	2.915	ns
		t_H	–1.146	–1.146	–2.638	ns
	GCLK PLL	t_{SU}	2.693	2.693	6.021	ns
		t_H	–2.588	–2.588	–5.744	ns

Table 4–56. EP1AGX35 Row Pins Output Timing Parameters (Part 2 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
2.5 V	8 mA	GCLK	t_{CO}	2.656	2.656	5.775	ns
		GCLK PLL	t_{CO}	1.237	1.237	2.703	ns
2.5 V	12 mA	GCLK	t_{CO}	2.637	2.637	5.661	ns
		GCLK PLL	t_{CO}	1.218	1.218	2.589	ns
1.8 V	2 mA	GCLK	t_{CO}	2.829	2.829	7.052	ns
		GCLK PLL	t_{CO}	1.410	1.410	3.980	ns
1.8 V	4 mA	GCLK	t_{CO}	2.818	2.818	6.273	ns
		GCLK PLL	t_{CO}	1.399	1.399	3.201	ns
1.8 V	6 mA	GCLK	t_{CO}	2.707	2.707	5.972	ns
		GCLK PLL	t_{CO}	1.288	1.288	2.900	ns
1.8 V	8 mA	GCLK	t_{CO}	2.676	2.676	5.858	ns
		GCLK PLL	t_{CO}	1.257	1.257	2.786	ns
1.5 V	2 mA	GCLK	t_{CO}	2.789	2.789	6.551	ns
		GCLK PLL	t_{CO}	1.370	1.370	3.479	ns
1.5 V	4 mA	GCLK	t_{CO}	2.682	2.682	5.950	ns
		GCLK PLL	t_{CO}	1.263	1.263	2.878	ns
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.626	2.626	5.614	ns
		GCLK PLL	t_{CO}	1.207	1.207	2.542	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.602	2.602	5.538	ns
		GCLK PLL	t_{CO}	1.183	1.183	2.466	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.568	2.568	5.407	ns
		GCLK PLL	t_{CO}	1.149	1.149	2.335	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.614	2.614	5.556	ns
		GCLK PLL	t_{CO}	1.195	1.195	2.484	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.618	2.618	5.485	ns
		GCLK PLL	t_{CO}	1.199	1.199	2.413	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.594	2.594	5.468	ns
		GCLK PLL	t_{CO}	1.175	1.175	2.396	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.597	2.597	5.447	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.375	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.595	2.595	5.466	ns
		GCLK PLL	t_{CO}	1.176	1.176	2.394	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.598	2.598	5.430	ns
		GCLK PLL	t_{CO}	1.179	1.179	2.358	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.580	2.580	5.426	ns
		GCLK PLL	t_{CO}	1.161	1.161	2.354	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.584	2.584	5.415	ns
		GCLK PLL	t_{CO}	1.165	1.165	2.343	ns

Table 4–61 lists I/O timing specifications.

Table 4–61. EP1AGX50 Column Pins Input Timing Parameters (Part 1 of 2)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.242	1.242	2.902	ns
		t_H	–1.137	–1.137	–2.625	ns
	GCLK PLL	t_{SU}	2.684	2.684	6.009	ns
		t_H	–2.579	–2.579	–5.732	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.242	1.242	2.902	ns
		t_H	–1.137	–1.137	–2.625	ns
	GCLK PLL	t_{SU}	2.684	2.684	6.009	ns
		t_H	–2.579	–2.579	–5.732	ns
2.5 V	GCLK	t_{SU}	1.252	1.252	2.884	ns
		t_H	–1.147	–1.147	–2.607	ns
	GCLK PLL	t_{SU}	2.694	2.694	5.991	ns
		t_H	–2.589	–2.589	–5.714	ns
1.8 V	GCLK	t_{SU}	1.318	1.318	3.094	ns
		t_H	–1.213	–1.213	–2.817	ns
	GCLK PLL	t_{SU}	2.760	2.760	6.201	ns
		t_H	–2.655	–2.655	–5.924	ns
1.5 V	GCLK	t_{SU}	1.321	1.321	3.187	ns
		t_H	–1.216	–1.216	–2.910	ns
	GCLK PLL	t_{SU}	2.763	2.763	6.294	ns
		t_H	–2.658	–2.658	–6.017	ns
SSTL-2 CLASS I	GCLK	t_{SU}	1.034	1.034	2.314	ns
		t_H	–0.929	–0.929	–2.037	ns
	GCLK PLL	t_{SU}	2.500	2.500	5.457	ns
		t_H	–2.395	–2.395	–5.180	ns
SSTL-2 CLASS II	GCLK	t_{SU}	1.034	1.034	2.314	ns
		t_H	–0.929	–0.929	–2.037	ns
	GCLK PLL	t_{SU}	2.500	2.500	5.457	ns
		t_H	–2.395	–2.395	–5.180	ns
SSTL-18 CLASS I	GCLK	t_{SU}	1.104	1.104	2.466	ns
		t_H	–0.999	–0.999	–2.189	ns
	GCLK PLL	t_{SU}	2.546	2.546	5.573	ns
		t_H	–2.441	–2.441	–5.296	ns
SSTL-18 CLASS II	GCLK	t_{SU}	1.074	1.074	2.424	ns
		t_H	–0.969	–0.969	–2.147	ns
	GCLK PLL	t_{SU}	2.539	2.539	5.564	ns
		t_H	–2.434	–2.434	–5.287	ns

Table 4–117. Fast PLL Specifications (Part 2 of 2)

Name	Description	Min	Typ	Max	Units
$t_{ARESET\_RECONFIG}$	Minimum pulse width on the areset signal when using PLL reconfiguration. Reset the PLL after scandone goes high.	500	—	—	ns

Note to Table 4–117:

(1) This is limited by the I/O f_{MAX}.

External Memory Interface Specifications

Table 4–118 through Table 4–122 list Arria GX device specifications for the dedicated circuitry used for interfacing with external memory devices.

Table 4–118. DLL Frequency Range Specifications

Frequency Mode	Frequency Range (MHz)
0	100 to 175
1	150 to 230
2	200 to 310

Table 4–119. DQS Jitter Specifications for DLL-Delayed Clock (tDQS_JITTER) , *(Note 1)*

Number of DQS Delay Buffer Stages *(2)*	Commercial (ps)	Industrial (ps)
1	80	110
2	110	130
3	130	180
4	160	210

Notes to Table 4–119:

(1) Peak-to-peak period jitter on the phase-shifted DQS clock. For example, jitter on two delay stages under commercial conditions is 200 ps peak-to-peak or 100 ps.

(2) Delay stages used for requested DQS phase shift are reported in a project's Compilation Report in the Quartus II software.

Table 4–120. DQS Phase-Shift Error Specifications for DLL-Delayed Clock (t_{DQS_PSERR})

Number of DQS Delay Buffer Stages	–6 Speed Grade (ps)
1	35
2	70
3	105
4	140

5. Reference and Ordering Information

AGX51005-2.0

Software

Arria® GX devices are supported by the Altera® Quartus® II design software, which provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap® II logic analyzer, and device configuration.

For more information about the Quartus II software features, refer to the *Quartus II Development Software Handbook* .

The Quartus II software supports the Windows XP/2000/NT, Sun Solaris 8/9, Linux Red Hat v7.3, Linux Red Hat Enterprise 3, and HP-UX operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink interface.

Device Pin-Outs

Arria GX device pin-outs are available on the Altera web site at www.altera.com.

Ordering Information

Figure 5–1 describes the ordering codes for Arria GX devices.

For more information on a specific package, refer to the *Package Information for Arria GX Devices* chapter.