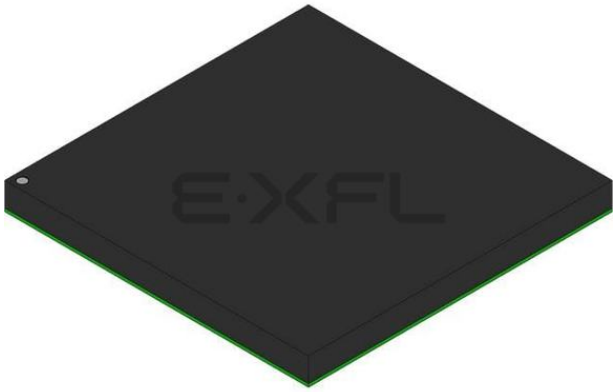
Altera - EP1AGX90EF1152I6 Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	4511
Number of Logic Elements/Cells	90220
Total RAM Bits	4477824
Number of I/O	538
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep1agx90ef1152i6

Each transceiver channel is full-duplex and consists of a transmitter channel and a receiver channel.

The transmitter channel contains the following sub-blocks:

- Transmitter phase compensation first-in first-out (FIFO) buffer
- Byte serializer (optional)
- 8B/10B encoder (optional)
- Serializer (parallel-to-serial converter)
- Transmitter differential output buffer

The receiver channel contains the following:

- Receiver differential input buffer
- Receiver lock detector and run length checker
- CRU
- Deserializer
- Pattern detector
- Word aligner
- Lane deskew
- Rate matcher (optional)
- 8B/10B decoder (optional)
- Byte deserializer (optional)
- Receiver phase compensation FIFO buffer

You can configure the transceiver channels to the desired functional modes using the ALT2GXB MegaCore instance in the Quartus® II MegaWizard™ Plug-in Manager for the Arria GX device family. Depending on the selected functional mode, the Quartus II software automatically configures the transceiver channels to employ a subset of the sub-blocks listed above.

Transmitter Path

This section describes the data path through the Arria GX transmitter. The sub-blocks are described in order from the PLD-transmitter parallel interface to the serial transmitter buffer.

Clock Multiplier Unit

Each transceiver block has a clock multiplier unit (CMU) that takes in a reference clock and synthesizes two clocks: a high-speed serial clock to serialize the data and a low-speed parallel clock to clock the transmitter digital logic (PCS).

The CMU is further divided into three sub-blocks:

- One transmitter PLL
- One central clock divider block
- Four local clock divider blocks (one per channel)

Table 2–6 lists the reset signals available in Arria GX devices and the transceiver circuitry affected by each signal.

Table 2–6. Reset Signal Map to Arria GX Blocks

Reset Signal	Transmitter Phase Compensation FIFO Module/ Byte Serializer	Transmitter 8B/10B Encoder	Transmitter Serializer	Transmitter Analog Circuits	Transmitter PLL	Transmitter XAUI State Machine	BIST Generators	Receiver Deserializer	Receiver Word Aligner	Receiver Deskew FIFO Module	Receiver Rate Matcher	Receiver 8B/10B Decoder	Receiver Phase Comp FIFO Module/ Byte Deserializer	Receiver PLL / CRU	Receiver XAUI State Machine	BIST Verifiers	Receiver Analog Circuits
rx_digitalreset	—	—	—	—	—	—	—	—	✓	—	✓	✓	✓	—	✓	✓	—
rx_analogreset	—	—	—	—	—	—	—	✓	—	—	—	—	—	✓	—	—	✓
tx_digitalreset	✓	✓	—	—	—	✓	✓	—	—	—	—	—	—	—	—	—	—
gxb_powerdown	✓	✓	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓	✓	✓	✓
gxb_enable	✓	✓	✓	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓	✓	✓	✓

Calibration Block

Arria GX devices use the calibration block to calibrate OCT for the PLLs, and their associated output buffers, and the terminating resistors on the transceivers. The calibration block counters the effects of process, voltage, and temperature (PVT). The calibration block references a derived voltage across an external reference resistor to calibrate the OCT resistors on Arria GX devices. You can power down the calibration block. However, powering down the calibration block during operations can yield transmit and receive data errors.

Transceiver Clocking

This section describes the clock distribution in an Arria GX transceiver channel and the PLD clock resource utilization by the transceiver blocks.

Transceiver Channel Clock Distribution

Each transceiver block has one transmitter PLL and four receiver PLLs.

Logic Array Blocks

Each logic array block (LAB) consists of eight adaptive logic modules (ALMs), carry chains, shared arithmetic chains, LAB control signals, local interconnects, and register chain connection lines. The local interconnect transfers signals between ALMs in the same LAB. Register chain connections transfer the output of an ALM register to the adjacent ALM register in a LAB. The Quartus II Compiler places associated logic in a LAB or adjacent LABs, allowing the use of local, shared arithmetic chain, and register chain connections for performance and area efficiency. Table 2–9 lists Arria GX device resources. Figure 2–25 shows the Arria GX LAB structure.

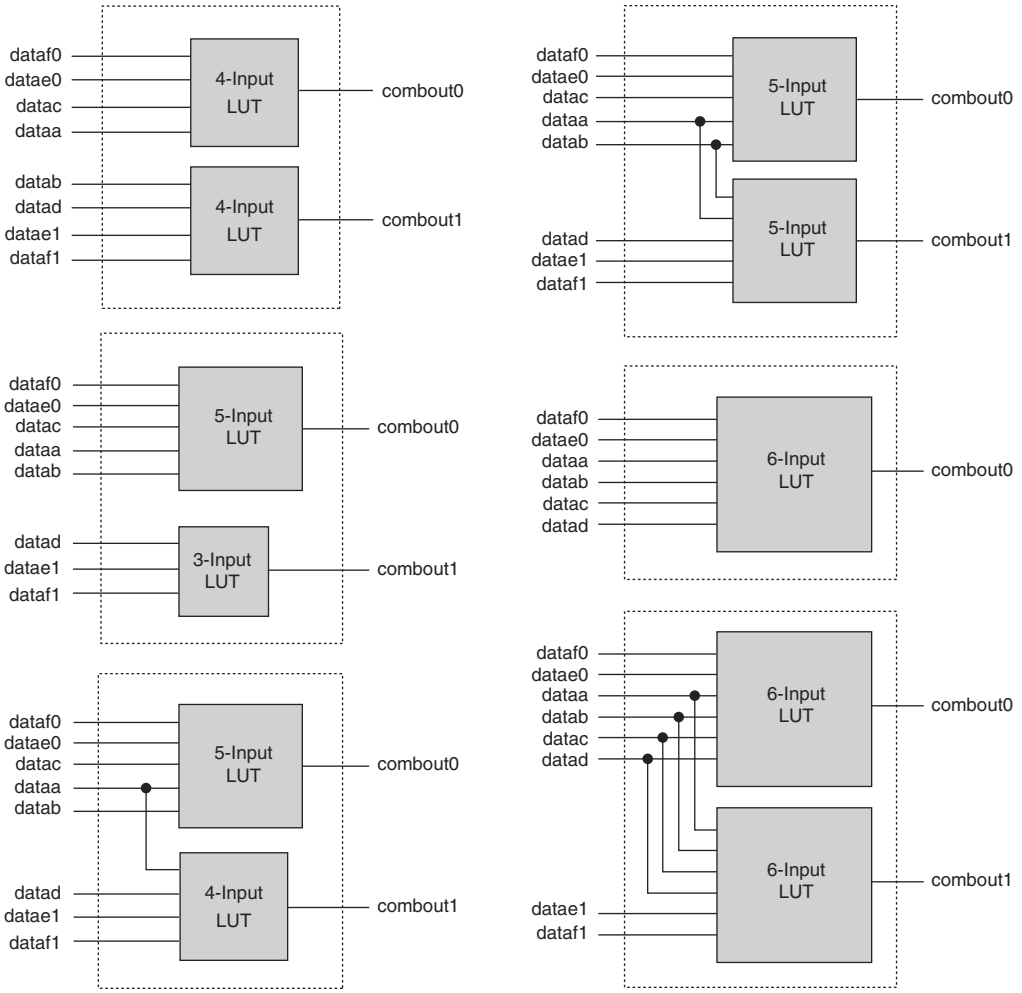
Table 2–9. Arria GX Device Resources

Device	M512 RAM Columns/Blocks	M4K RAM Columns/Blocks	M-RAM Blocks	DSP Block Columns/Blocks
EP1AGX20	166	118	1	10
EP1AGX35	197	140	1	14
EP1AGX50	313	242	2	26
EP1AGX60	326	252	2	32
EP1AGX90	478	400	4	44

Normal Mode

Normal mode is suitable for general logic applications and combinational functions. In this mode, up to eight data inputs from the LAB local interconnect are inputs to the combinational logic. Normal mode allows two functions to be implemented in one Arria GX ALM, or an ALM to implement a single function of up to six inputs. The ALM can support certain combinations of completely independent functions and various combinations of functions which have common inputs. Figure 2–30 shows the supported LUT combinations in normal mode.

Figure 2–30. ALM in Normal Mode *(Note 1)*



Note to Figure 2–30:

(1) Combinations of functions with less inputs than those shown are also supported. For example, combinations of functions with the following number of inputs are supported: 4 and 3, 3 and 3, 3 and 2, 5 and 2, and so on.

Normal mode provides complete backward compatibility with four-input LUT architectures. Two independent functions of four inputs or less can be implemented in one Arria GX ALM. In addition, a five-input function and an independent three-input function can be implemented without sharing inputs.

In addition to the clear and load/preset ports, Arria GX devices provide a device-wide reset pin (DEV_CLRn) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This device-wide reset overrides all other control signals.

MultiTrack Interconnect

In Arria GX architecture, the MultiTrack interconnect structure with DirectDrive technology provides connections between ALMs, TriMatrix memory, DSP blocks, and device I/O pins. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different lengths and speeds used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement in the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when migrating through different device densities. Dedicated row interconnects route signals to and from LABs, DSP blocks, and TriMatrix memory in the same row.

These row resources include:

- Direct link interconnects between LABs and adjacent blocks
- R4 interconnects traversing four blocks to the right or left
- R24 row interconnects for high-speed access across the length of the device

The direct link interconnect allows a LAB, DSP block, or TriMatrix memory block to drive into the local interconnect of its left and right neighbors and then back into itself, providing fast communication between adjacent LABs and/or blocks without using row interconnect resources.

The R4 interconnects span four LABs, three LABs and one M512 RAM block, two LABs and one M4K RAM block, or two LABs and one DSP block to the right or left of a source LAB. These resources are used for fast row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. Figure 2–39 shows R4 interconnect connections from a LAB.

R4 interconnects can drive and be driven by DSP blocks and RAM blocks and row IOEs. For LAB interfacing, a primary LAB or LAB neighbor can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive onto the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive onto the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. R4 interconnects can also drive C4 and C16 interconnects for connections from one row to another. Additionally, R4 interconnects can drive R24 interconnects.

Table 2–13. DSP Blocks in Arria GX Devices *(Note 1)*

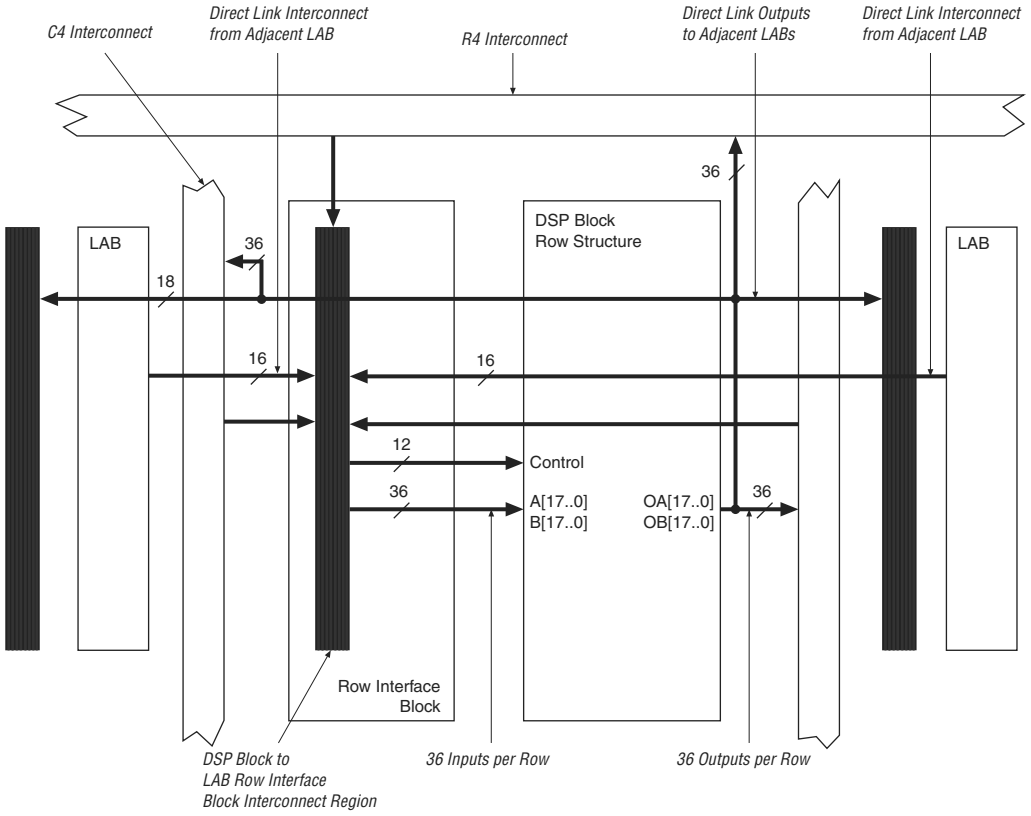
Device	DSP Blocks	Total 9 × 9 Multipliers	Total 18 × 18 Multipliers	Total 36 × 36 Multipliers
EP1AGX20	10	80	40	10
EP1AGX35	14	112	56	14
EP1AGX50	26	208	104	26
EP1AGX60	32	256	128	32
EP1AGX90	44	352	176	44

Note to Table 2–13:

(1) This list only shows functions that can fit into a single DSP block. Multiple DSP blocks can support larger multiplication functions.

Additionally, DSP block input registers can efficiently implement shift registers for FIR filter applications. DSP blocks support Q1.15 format rounding and saturation. Figure 2–51 shows a top-level diagram of the DSP block configured for 18 × 18-bit multiplier mode.

Figure 2–53. DSP Block Interface to Interconnect



A bus of 44 control signals feeds the entire DSP block. These signals include clocks, asynchronous clears, clock enables, signed and unsigned control signals, addition and subtraction control signals, rounding and saturation control signals, and accumulator synchronous loads. The clock signals are routed from LAB row clocks and are generated from specific LAB rows at the DSP block interface. The LAB row source for control signals, data inputs, and outputs is shown in Table 2–15.

For more information about DSP blocks, refer to the *DSP Blocks in Arria GX Devices* chapter.

Table 2–18. Arria GX PLL Features (Part 2 of 2)

Feature	Enhanced PLL	Fast PLL
Number of feedback clock inputs	One single-ended or differential *(7)*, *(8)*	—

Notes to Table 2–18:

(1) For enhanced PLLs, *m*, *n* range from 1 to 256 and post-scale counters range from 1 to 512 with 50% duty cycle.
(2) For fast PLLs, *m*, and post-scale counters range from 1 to 32. The *n* counter ranges from 1 to 4.
(3) The smallest phase shift is determined by the voltage controlled oscillator (V_{CO}) period divided by 8.
(4) For degree increments, Arria GX devices can shift all output frequencies in increments of at least 45. Smaller degree increments are possible depending on the frequency and divide parameters.
(5) Arria GX fast PLLs only support manual clock switchover.
(6) Fast PLLs can drive to any I/O pin as an external clock. For high-speed differential I/O pins, the device uses a data channel to generate `txclkout`.
(7) If the feedback input is used, you lose one (or two, if f_{BIN} is differential) external clock output pin.
(8) Every Arria GX device has at least two enhanced PLLs with one single-ended or differential external feedback input per PLL.

Figure 2–61 shows a top-level diagram of the Arria GX device and PLL floorplan.

Figure 2–61. PLL Locations

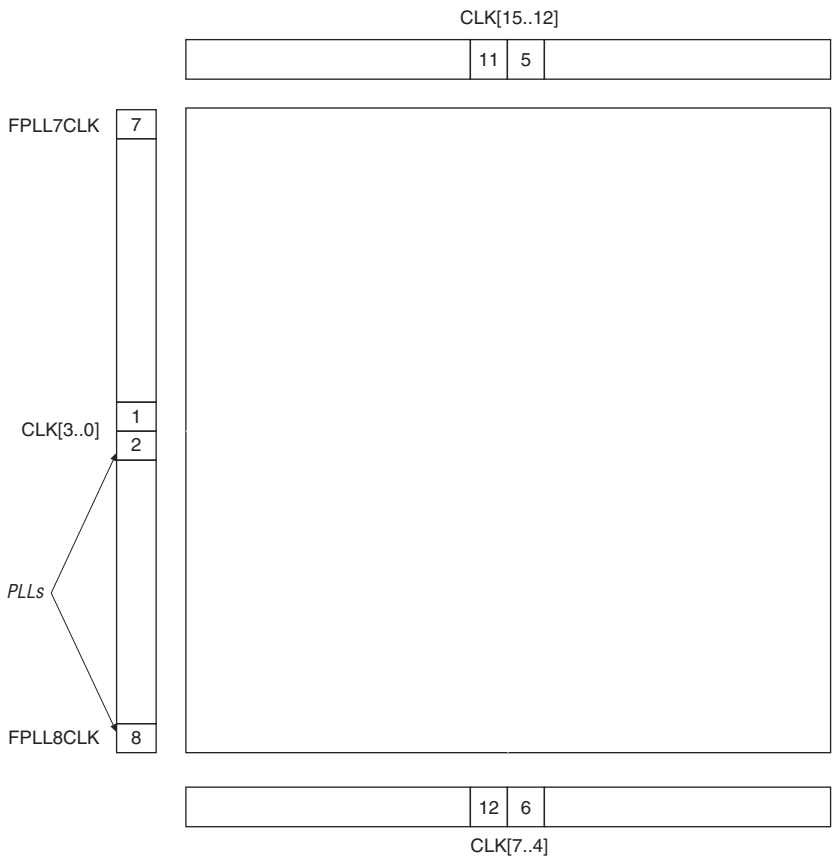


Figure 2–62 and Figure 2–63 shows global and regional clocking from the fast PLL outputs and side clock pins. The connections to the global and regional clocks from the fast PLL outputs, internal drivers, and `CLK` pins on the left side of the device are shown in Table 2–19.

Table 3–1. Arria GX JTAG Instructions

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer.
EXTEST *(1)*	00 0000 1111	Allows external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing IDCODE to be serially shifted out of TDO.
HIGHZ *(1)*	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP *(1)*	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions	—	Used when configuring an Arria GX device via the JTAG port with a USB-Blaster™, MasterBlaster™, ByteBlasterMV™, EthernetBlaster™, or ByteBlaster II download cable, or when using a **.jam** or **.jbc** via an embedded processor or JRunner™.
PULSE_NCONFIG	00 0000 0001	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.
CONFIG_IO *(2)*	00 0000 1101	Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, during, or after configuration. Stops configuration if executed during configuration. Once issued, the CONFIG_IO instruction holds nSTATUS low to reset the configuration device. nSTATUS is held low until the IOE configuration register is loaded and the TAP controller state machine transitions to the UPDATE_DR state.

Notes to Table 3–1:

(1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

(2) For more information about using the CONFIG_IO instruction, refer to the *MorphIO: An I/O Reconfiguration Solution for Altera Devices* White Paper.

Document Revision History

Table 3–5 lists the revision history for this chapter.

Table 3–5. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
December 2009, v2.0	■ Document template update. ■ Minor text edits.	—
May 2009 v1.4	■ Removed "Temperature Sensing Diode" section. ■ Updated Table 3–1 and Table 3–4.	—
May 2008 v1.3	Updated note in "Introduction" section.	
	Minor text edits.	—
August 2007 v1.2	Added the "Referenced Documents" section.	—
June 2007 v1.1	Deleted Signal Tap II information from Table 3–1.	—
May 2007 v1.0	Initial Release	—

Table 4–7. Arria GX Transceiver Block AC Specification *(Note 1), (2), (3)* (Part 3 of 4)

Description	Condition	–6 Speed Grade Commercial & Industrial	Units
Serial RapidIO (1.25 Gbps, 2.5 Gbps, and 3.125 Gbps) Receiver Jitter Tolerance *(6)*			
Total Jitter Tolerance	CJPAT Compliance Pattern; DC Gain = 0 dB	> 0.65	UI p-p
Combined Deterministic and Random Jitter Tolerance (J_{DR})	CJPAT Compliance Pattern; DC Gain = 0 dB	> 0.55	UI p-p
Deterministic Jitter Tolerance (J_D)	CJPAT Compliance Pattern; DC Gain = 0 dB	> 0.37	UI p-p
Sinusoidal Jitter Tolerance	Jitter Frequency = 22.1 KHz	> 8.5	UI p-p
	Jitter Frequency = 200 KHz	> 1.0	UI p-p
	Jitter Frequency = 1.875 MHz	> 0.1	UI p-p
	Jitter Frequency = 20 MHz	> 0.1	UI p-p
SDI Transmitter Jitter Generation *(8)*			
Alignment Jitter (peak-to-peak)	Data Rate = 1.485 Gbps (HD) REFCLK = 74.25 MHz Pattern = Color Bar Vod = 800 mV No Pre-emphasis Low-Frequency Roll-Off = 100 KHz	0.2	UIv
	Data Rate = 2.97 Gbps (3G) REFCLK = 148.5 MHz Pattern = Color Bar Vod = 800 mV No Pre-emphasis Low-Frequency Roll-Off = 100 KHz	0.3	UI

Table 4–24. 3.3-V PCI Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	—	0.5 V_{CCIO}	—	V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage	—	–0.3	—	0.3 V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 V_{CCIO}	—	—	V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA	—	—	0.1 V_{CCIO}	V

Table 4–25. PCI-X Mode 1 Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage	—	3.0	3.6	V
V_{IH}	High-level input voltage	—	0.5 V_{CCIO}	V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 V_{CCIO}	V
V_{IPU}	Input pull-up voltage	—	0.7 V_{CCIO}	—	V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 V_{CCIO}	—	V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA	—	0.1 V_{CCIO}	V

Table 4–26. SSTL-18 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	1.71	1.8	1.89	V
V_{REF}	Reference voltage	—	0.855	0.9	0.945	V
V_{TT}	Termination voltage	—	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{IH} (DC)	High-level DC input voltage	—	V_{REF} + 0.125	—	—	V
V_{IL} (DC)	Low-level DC input voltage	—	—	—	V_{REF} – 0.125	V
V_{IH} (AC)	High-level AC input voltage	—	V_{REF} + 0.25	—	—	V
V_{IL} (AC)	Low-level AC input voltage	—	—	—	V_{REF} – 0.25	V
V_{OH}	High-level output voltage	I_{OH} = –6.7 mA *(1)*	V_{TT} + 0.475	—	—	V
V_{OL}	Low-level output voltage	I_{OL} = 6.7 mA *(1)*	—	—	V_{TT} – 0.475	V

Note to Table 4–26:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Arria GX Architecture* chapter.

Table 4–27. SSTL-18 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage	—	1.71	1.8	1.89	V
V_{REF}	Reference voltage	—	0.855	0.9	0.945	V
V_{TT}	Termination voltage	—	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{IH} (DC)	High-level DC input voltage	—	V_{REF} + 0.125	—	—	V
V_{IL} (DC)	Low-level DC input voltage	—	—	—	V_{REF} – 0.125	V
V_{IH} (AC)	High-level AC input voltage	—	V_{REF} + 0.25	—	—	V
V_{IL} (AC)	Low-level AC input voltage	—	—	—	V_{REF} – 0.25	V

Table 4–44. Output Timing Measurement Methodology for Output Pins *(Note 1), (2), (3)*

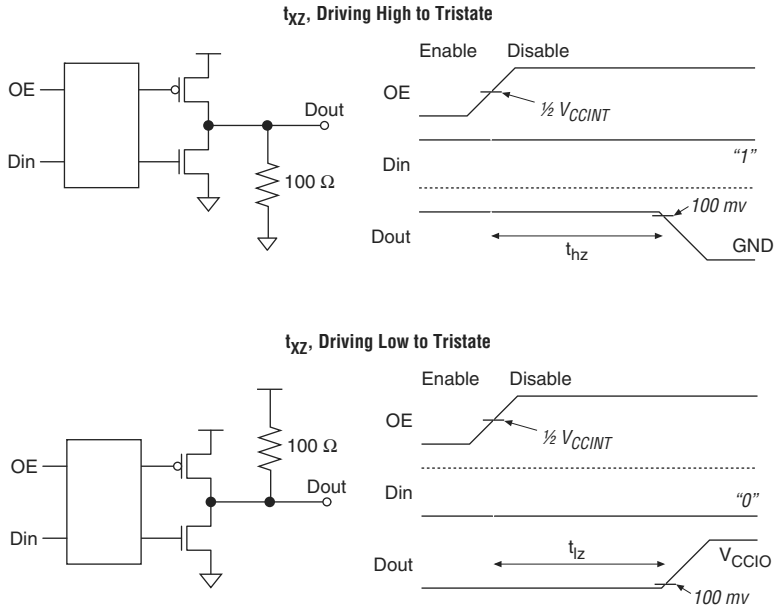
I/O Standard	Loading and Termination						Measurement Point
	R_S (Ω)	R_D (Ω)	R_T (Ω)	V_{CCIO} (V)	V_{TT} (V)	C_L (pF)	V_{MEAS} (V)
1.8-V differential HSTL Class II	—	—	25	1.660	0.790	0	0.83
LVDS	—	100	—	2.325	—	0	1.1625
LVPECL	—	100	—	3.135	—	0	1.5675

Notes to Table 4–44:

(1) Input measurement point at internal node is 0.5 V_{CCINT}.
(2) Output measuring point for V_{MEAS} at buffer output is 0.5 V_{CCIO}.
(3) Input stimulus edge rate is 0 to V_{CC} in 0.2 ns (internal signal) from the driver preceding the I/O buffer.
(4) Less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V with less than 30-mV ripple.
(5) V_{CCPD} = 2.97 V, less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V.

Figure 4–8 and Figure 4–9 show the measurement setup for output disable and output enable timing.

Figure 4–8. Measurement Setup for t_{xz} *(Note 1)*



Note to Figure 4–8:

(1) V_{CCINT} is 1.12 V for this measurement.

Table 4–45. Timing Measurement Methodology for Input Pins *(Note 1)*, *(2)*, *(3)*, *(4)* (Part 2 of 2)

I/O Standard	Measurement Conditions			Measurement Point
	V_{CCIO} (V)	V_{REF} (V)	Edge Rate (ns)	VMEAS (V)
Differential SSTL-18 Class II	1.660	0.830	1.660	0.83
1.5-V differential HSTL Class I	1.375	0.688	1.375	0.6875
1.5-V differential HSTL Class II	1.375	0.688	1.375	0.6875
1.8-V differential HSTL Class I	1.660	0.830	1.660	0.83
1.8-V differential HSTL Class II	1.660	0.830	1.660	0.83
LVDS	2.325	—	0.100	1.1625
LVPECL	3.135	—	0.100	1.5675

Notes to Table 4–45:

(1) Input buffer sees no load at buffer input.
(2) Input measuring point at buffer input is 0.5 V_{CCIO}.
(3) Output measuring point is 0.5 V_{CC} at internal node.
(4) Input edge rate is 1 V/ns.
(5) Less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V with less than 30-mV ripple.
(6) V_{CCPD} = 2.97 V, less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V.

Clock Network Skew Adders

The Quartus II software models skew within dedicated clock networks such as global and regional clocks. Therefore, the intra-clock network skew adder is not specified. Table 4–46 specifies the intra clock skew between any two clock networks driving any registers in the Arria GX device.

Table 4–46. Clock Network Specifications

Name	Description	Min	Typ	Max	Units
Clock skew adder EP1AGX20/35 *(1)*	Inter-clock network, same side	—	—	± 50	ps
	Inter-clock network, entire chip	—	—	± 100	ps
Clock skew adder EP1AGX50/60 *(1)*	Inter-clock network, same side	—	—	± 50	ps
	Inter-clock network, entire chip	—	—	± 100	ps
Clock skew adder EP1AGX90 *(1)*	Inter-clock network, same side	—	—	± 55	ps
	Inter-clock network, entire chip	—	—	± 110	ps

Note to Table 4–46:

(1) This is in addition to intra-clock network skew, which is modeled in the Quartus II software.

Default Capacitive Loading of Different I/O Standards

See Table 4–47 for default capacitive loading of different I/O standards.

Table 4–47. Default Loading of Different I/O Standards for Arria GX Devices (Part 1 of 2)

I/O Standard	Capacitive Load	Units
LVTTL	0	pF
LVCMOS	0	pF
2.5 V	0	pF

Table 4–62. EP1AGX50 Row Pins Output Timing Parameters (Part 3 of 3)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.606	2.606	5.480	ns
		GCLK PLL	t_{CO}	1.178	1.178	2.396	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.608	2.608	5.442	ns
		GCLK PLL	t_{CO}	1.181	1.181	2.360	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.590	2.590	5.438	ns
		GCLK PLL	t_{CO}	1.163	1.163	2.356	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.594	2.594	5.427	ns
		GCLK PLL	t_{CO}	1.167	1.167	2.345	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.585	2.585	5.426	ns
		GCLK PLL	t_{CO}	1.158	1.158	2.344	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.605	2.605	5.457	ns
		GCLK PLL	t_{CO}	1.177	1.177	2.373	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.607	2.607	5.441	ns
		GCLK PLL	t_{CO}	1.180	1.180	2.359	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.592	2.592	5.433	ns
		GCLK PLL	t_{CO}	1.165	1.165	2.351	ns
LVDS	—	GCLK	t_{CO}	2.654	2.654	5.613	ns
		GCLK PLL	t_{CO}	1.226	1.226	2.530	ns

Table 4–63 lists I/O timing specifications.

Table 4–63. EP1AGX50 Column Pins Output Timing Parameters (Part 1 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	2.948	2.948	6.608	ns
		GCLK PLL	t_{CO}	1.476	1.476	3.447	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.797	2.797	6.203	ns
		GCLK PLL	t_{CO}	1.331	1.331	3.075	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.722	2.722	6.204	ns
		GCLK PLL	t_{CO}	1.264	1.264	3.075	ns
3.3-V LVTTL	16 mA	GCLK	t_{CO}	2.694	2.694	6.024	ns
		GCLK PLL	t_{CO}	1.238	1.238	2.906	ns
3.3-V LVTTL	20 mA	GCLK	t_{CO}	2.670	2.670	5.896	ns
		GCLK PLL	t_{CO}	1.216	1.216	2.781	ns
3.3-V LVTTL	24 mA	GCLK	t_{CO}	2.660	2.660	5.895	ns
		GCLK PLL	t_{CO}	1.209	1.209	2.783	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.797	2.797	6.203	ns
		GCLK PLL	t_{CO}	1.331	1.331	3.075	ns

Table 4–67. EP1AGX60 Column Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
LVDS	GCLK	t_{SU}	0.980	0.980	2.062	ns
		t_{H}	–0.875	–0.875	–1.785	ns
	GCLK PLL	t_{SU}	2.557	2.557	5.512	ns
		t_{H}	–2.452	–2.452	–5.235	ns

Table 4–68 lists I/O timing specifications.

Table 4–68. EP1AGX60 Row Pins Output Timing Parameters (Part 1 of 2)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V LVTTL	4 mA	GCLK	t_{CO}	3.052	3.052	7.142	ns
		GCLK PLL	t_{CO}	1.490	1.490	3.719	ns
3.3-V LVTTL	8 mA	GCLK	t_{CO}	2.924	2.924	6.502	ns
		GCLK PLL	t_{CO}	1.362	1.362	3.079	ns
3.3-V LVTTL	12 mA	GCLK	t_{CO}	2.868	2.868	6.465	ns
		GCLK PLL	t_{CO}	1.306	1.306	3.042	ns
3.3-V LVCMOS	4 mA	GCLK	t_{CO}	2.924	2.924	6.502	ns
		GCLK PLL	t_{CO}	1.362	1.362	3.079	ns
3.3-V LVCMOS	8 mA	GCLK	t_{CO}	2.818	2.818	6.196	ns
		GCLK PLL	t_{CO}	1.256	1.256	2.773	ns
2.5 V	4 mA	GCLK	t_{CO}	2.907	2.907	6.476	ns
		GCLK PLL	t_{CO}	1.345	1.345	3.053	ns
2.5 V	8 mA	GCLK	t_{CO}	2.804	2.804	6.218	ns
		GCLK PLL	t_{CO}	1.242	1.242	2.795	ns
2.5 V	12 mA	GCLK	t_{CO}	2.785	2.785	6.104	ns
		GCLK PLL	t_{CO}	1.223	1.223	2.681	ns
1.8 V	2 mA	GCLK	t_{CO}	2.991	2.991	7.521	ns
		GCLK PLL	t_{CO}	1.419	1.419	4.078	ns
1.8 V	4 mA	GCLK	t_{CO}	2.980	2.980	6.742	ns
		GCLK PLL	t_{CO}	1.408	1.408	3.299	ns
1.8 V	6 mA	GCLK	t_{CO}	2.869	2.869	6.441	ns
		GCLK PLL	t_{CO}	1.297	1.297	2.998	ns
1.8 V	8 mA	GCLK	t_{CO}	2.838	2.838	6.327	ns
		GCLK PLL	t_{CO}	1.266	1.266	2.884	ns
1.5 V	2 mA	GCLK	t_{CO}	2.951	2.951	7.020	ns
		GCLK PLL	t_{CO}	1.379	1.379	3.577	ns
1.5 V	4 mA	GCLK	t_{CO}	2.844	2.844	6.419	ns
		GCLK PLL	t_{CO}	1.272	1.272	2.976	ns

Table 4–68. EP1AGX60 Row Pins Output Timing Parameters (Part 2 of 2)

I/O Standard	Drive Strength	Clock	Parameter	Fast Model		–6 Speed Grade	Units
				Industrial	Commercial		
SSTL-2 CLASS I	8 mA	GCLK	t_{CO}	2.774	2.774	6.057	ns
		GCLK PLL	t_{CO}	1.211	1.211	2.633	ns
SSTL-2 CLASS I	12 mA	GCLK	t_{CO}	2.750	2.750	5.981	ns
		GCLK PLL	t_{CO}	1.187	1.187	2.557	ns
SSTL-2 CLASS II	16 mA	GCLK	t_{CO}	2.716	2.716	5.850	ns
		GCLK PLL	t_{CO}	1.153	1.153	2.426	ns
SSTL-18 CLASS I	4 mA	GCLK	t_{CO}	2.776	2.776	6.025	ns
		GCLK PLL	t_{CO}	1.204	1.204	2.582	ns
SSTL-18 CLASS I	6 mA	GCLK	t_{CO}	2.780	2.780	5.954	ns
		GCLK PLL	t_{CO}	1.208	1.208	2.511	ns
SSTL-18 CLASS I	8 mA	GCLK	t_{CO}	2.756	2.756	5.937	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.494	ns
SSTL-18 CLASS I	10 mA	GCLK	t_{CO}	2.759	2.759	5.916	ns
		GCLK PLL	t_{CO}	1.187	1.187	2.473	ns
1.8-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.757	2.757	5.935	ns
		GCLK PLL	t_{CO}	1.185	1.185	2.492	ns
1.8-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.760	2.760	5.899	ns
		GCLK PLL	t_{CO}	1.188	1.188	2.456	ns
1.8-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.742	2.742	5.895	ns
		GCLK PLL	t_{CO}	1.170	1.170	2.452	ns
1.8-V HSTL CLASS I	10 mA	GCLK	t_{CO}	2.746	2.746	5.884	ns
		GCLK PLL	t_{CO}	1.174	1.174	2.441	ns
1.8-V HSTL CLASS I	12 mA	GCLK	t_{CO}	2.737	2.737	5.883	ns
		GCLK PLL	t_{CO}	1.165	1.165	2.440	ns
1.5-V HSTL CLASS I	4 mA	GCLK	t_{CO}	2.756	2.756	5.912	ns
		GCLK PLL	t_{CO}	1.184	1.184	2.469	ns
1.5-V HSTL CLASS I	6 mA	GCLK	t_{CO}	2.759	2.759	5.898	ns
		GCLK PLL	t_{CO}	1.187	1.187	2.455	ns
1.5-V HSTL CLASS I	8 mA	GCLK	t_{CO}	2.744	2.744	5.890	ns
		GCLK PLL	t_{CO}	1.172	1.172	2.447	ns
LVDS	—	GCLK	t_{CO}	2.787	2.787	6.037	ns
		GCLK PLL	t_{CO}	1.228	1.228	2.618	ns

Table 4–69. EP1AGX60 Column Pins Output Timing Parameters (Part 4 of 4)

I/O Standard	Drive Strength	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
				Industrial	Commercial		
3.3-V PCI	—	GCLK	t_{CO}	2.882	2.882	6.213	ns
		GCLK PLL	t_{CO}	1.312	1.312	2.778	ns
3.3-V PCI-X	—	GCLK	t_{CO}	2.882	2.882	6.213	ns
		GCLK PLL	t_{CO}	1.312	1.312	2.778	ns
LVDS	—	GCLK	t_{CO}	3.746	3.746	7.396	ns
		GCLK PLL	t_{CO}	2.185	2.185	3.973	ns

Table 4–70 through Table 4–71 list EP1AGX60 regional clock (RCLK) adder values that should be added to the GCLK values. These adder values are used to determine I/O timing when the I/O pin is driven using the regional clock. This applies for all I/O standards supported by Arria GX with general purpose I/O pins.

Table 4–70 describes row pin delay adders when using the regional clock in Arria GX devices.

Table 4–70. EP1AGX60 Row Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.138	0.138	0.311	ns
RCLK PLL input adder	–0.003	–0.003	–0.006	ns
RCLK output adder	–0.138	–0.138	–0.311	ns
RCLK PLL output adder	0.003	0.003	0.006	ns

Table 4–71 lists column pin delay adders when using the regional clock in Arria GX devices.

Table 4–71. EP1AGX60 Column Pin Delay Adders for Regional Clock

Parameter	Fast Corner		–6 Speed Grade	Units
	Industrial	Commercial		
RCLK input adder	0.153	0.153	0.344	ns
RCLK PLL input adder	–1.066	–1.066	–2.338	ns
RCLK output adder	–0.153	–0.153	–0.343	ns
RCLK PLL output adder	1.721	1.721	4.486	ns

EP1AGX90 I/O Timing Parameters

Table 4–72 through Table 4–75 list the maximum I/O timing parameters for EP1AGX90 devices for I/O standards which support general purpose I/O pins.

Table 4–72 lists I/O timing specifications.

Table 4–72. EP1AGX90 Row Pins Input Timing Parameters (Part 1 of 2)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.295	1.295	2.873	ns
		t_H	–1.190	–1.190	–2.596	ns
	GCLK PLL	t_{SU}	3.366	3.366	7.017	ns
		t_H	–3.261	–3.261	–6.740	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.295	1.295	2.873	ns
		t_H	–1.190	–1.190	–2.596	ns
	GCLK PLL	t_{SU}	3.366	3.366	7.017	ns
		t_H	–3.261	–3.261	–6.740	ns
2.5 V	GCLK	t_{SU}	1.307	1.307	2.854	ns
		t_H	–1.202	–1.202	–2.577	ns
	GCLK PLL	t_{SU}	3.378	3.378	6.998	ns
		t_H	–3.273	–3.273	–6.721	ns
1.8 V	GCLK	t_{SU}	1.381	1.381	3.073	ns
		t_H	–1.276	–1.276	–2.796	ns
	GCLK PLL	t_{SU}	3.434	3.434	7.191	ns
		t_H	–3.329	–3.329	–6.914	ns
1.5 V	GCLK	t_{SU}	1.384	1.384	3.168	ns
		t_H	–1.279	–1.279	–2.891	ns
	GCLK PLL	t_{SU}	3.437	3.437	7.286	ns
		t_H	–3.332	–3.332	–7.009	ns
SSTL-2 CLASS I	GCLK	t_{SU}	1.121	1.121	2.329	ns
		t_H	–1.016	–1.016	–2.052	ns
	GCLK PLL	t_{SU}	3.187	3.187	6.466	ns
		t_H	–3.082	–3.082	–6.189	ns
SSTL-2 CLASS II	GCLK	t_{SU}	1.121	1.121	2.329	ns
		t_H	–1.016	–1.016	–2.052	ns
	GCLK PLL	t_{SU}	3.187	3.187	6.466	ns
		t_H	–3.082	–3.082	–6.189	ns
SSTL-18 CLASS I	GCLK	t_{SU}	1.159	1.159	2.447	ns
		t_H	–1.054	–1.054	–2.170	ns
	GCLK PLL	t_{SU}	3.212	3.212	6.565	ns
		t_H	–3.107	–3.107	–6.288	ns
SSTL-18 CLASS II	GCLK	t_{SU}	1.157	1.157	2.441	ns
		t_H	–1.052	–1.052	–2.164	ns
	GCLK PLL	t_{SU}	3.235	3.235	6.597	ns
		t_H	–3.130	–3.130	–6.320	ns

Table 4–107. Arria GX Maximum Output Clock Rate for Dedicated Clock Pins (Part 3 of 4)

I/O Standards	Drive Strength	–6 Speed Grade	Units
DIFFERENTIAL 1.8-V SSTL CLASS I	4 mA	140	MHz
	6 mA	186	MHz
	8 mA	280	MHz
	10 mA	373	MHz
	12 mA	373	MHz
DIFFERENTIAL 1.8-V SSTL CLASS II	8 mA	140	MHz
	16 mA	327	MHz
	18 mA	373	MHz
	20 mA	420	MHz
DIFFERENTIAL 1.8-V HSTL CLASS I	4 mA	280	MHz
	6 mA	420	MHz
	8 mA	561	MHz
	10 mA	561	MHz
	12 mA	607	MHz
DIFFERENTIAL 1.8-V HSTL CLASS II	16 mA	420	MHz
	18 mA	467	MHz
	20 mA	514	MHz
DIFFERENTIAL 1.5-V HSTL CLASS I	4 mA	280	MHz
	6 mA	420	MHz
	8 mA	561	MHz
	10 mA	607	MHz
	12 mA	654	MHz
DIFFERENTIAL 1.5-V HSTL CLASS II	16 mA	514	MHz
	18 mA	561	MHz
	20 mA	561	MHz
	24 mA	278	MHz
3.3-V PCI	—	626	MHz
3.3-V PCI-X	—	626	MHz
LVDS	—	280	MHz
HYPERTRANSPORT	—	116	MHz
LVPECL	—	280	MHz
3.3-V LVTTL	SERIES_25_OHMS	327	MHz
	SERIES_50_OHMS	327	MHz
3.3-V LVCMOS	SERIES_25_OHMS	280	MHz
	SERIES_50_OHMS	280	MHz
2.5 V	SERIES_25_OHMS	280	MHz
	SERIES_50_OHMS	280	MHz
1.8 V	SERIES_25_OHMS	420	MHz
	SERIES_50_OHMS	420	MHz