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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

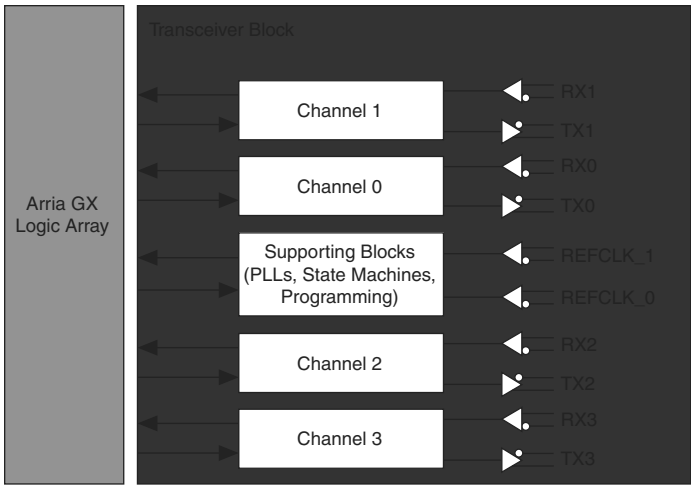
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4511
Number of Logic Elements/Cells	90220
Total RAM Bits	4477824
Number of I/O	538
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep1agx90ef1152i6n

Figure 2–1 shows a high-level diagram of the transceiver block architecture divided into four channels.

Figure 2–1. Transceiver Block

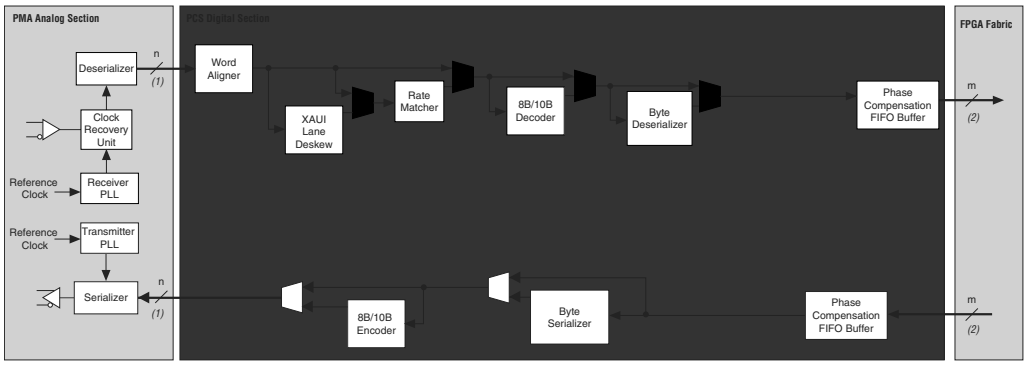


Each transceiver block has:

- Four transceiver channels with dedicated physical coding sublayer (PCS) and physical media attachment (PMA) circuitry
- One transmitter PLL that takes in a reference clock and generates high-speed serial clock depending on the functional mode
- Four receiver PLLs and clock recovery unit (CRU) to recover clock and data from the received serial data stream
- State machines and other logic to implement special features required to support each protocol

Figure 2–2 shows functional blocks that make up a transceiver channel.

Figure 2–2. Arria GX Transceiver Channel Block Diagram



Notes to Figure 2–2:

(1) "n" represents the number of bits in each word that must be serialized by the transmitter portion of the PMA. n = 8 or 10.

(2) "m" represents the number of bits in the word that passes between the FPGA logic and the PCS portion of the transceiver. m = 8, 10, 16, or 20.

XAUI Mode

In XAUI mode, the rate matcher adheres to clause 48 of the IEEE 802.3ae specification for clock rate compensation. The rate matcher performs clock compensation on columns of /R/ (/K28.0/), denoted by //R//. An //R// is added or deleted automatically based on the number of words in the FIFO buffer.

PCI Express (PIPE) Mode Rate Matcher

In PCI Express (PIPE) mode, the rate matcher can compensate up to ± 300 PPM (600 PPM total) frequency difference between the upstream transmitter and the receiver. The rate matcher logic looks for skip ordered sets (SOS), which contains a /K28.5/ comma followed by three /K28.0/ skip characters. The rate matcher logic deletes or inserts /K28.0/ skip characters as necessary from/to the rate matcher FIFO.

The rate matcher in PCI Express (PIPE) mode has a FIFO buffer overflow and underflow protection. In the event of a FIFO buffer overflow, the rate matcher deletes any data after detecting the overflow condition to prevent FIFO pointer corruption until the rate matcher is not full. In an underflow condition, the rate matcher inserts 9'h1FE (/K30.7/) until the FIFO buffer is not empty. These measures ensure that the FIFO buffer can gracefully exit the overflow and underflow condition without requiring a FIFO reset. The rate matcher FIFO overflow and underflow condition is indicated on the `pipestatus` port.

You can bypass the rate matcher in PCI Express (PIPE) mode if you have a synchronous system where the upstream transmitter and local receiver derive their reference clocks from the same source.

GIGE Mode Rate Matcher

In GIGE mode, the rate matcher can compensate up to ± 100 PPM (200 PPM total) frequency difference between the upstream transmitter and the receiver. The rate matcher logic inserts or deletes /I2/ idle ordered sets to/from the rate matcher FIFO during the inter-frame or inter-packet gap (IFG or IPG). /I2/ is selected as the rate matching ordered set because it maintains the running disparity, unlike /I1/ that alters the running disparity. Because the /I2/ ordered-set contains two 10-bit code groups (/K28.5/, /D16.2/), 20 bits are inserted or deleted at a time for rate matching.

The rate matcher logic has the capability to insert or delete /C1/ or /C2/ configuration ordered sets when 'GIGE Enhanced' mode is chosen as the sub-protocol in the MegaWizard Plug-In Manager.

If the frequency PPM difference between the upstream transmitter and the local receiver is high, or if the packet size is too large, the rate matcher FIFO buffer can face an overflow or underflow situation.

Basic Mode

In basic mode, you can program the skip and control pattern for rate matching. There is no restriction on the deletion of a skip character in a cluster. The rate matcher deletes the skip characters as long as they are available. For insertion, the rate matcher inserts skip characters such that the number of skip characters at the output of rate matcher does not exceed five.

The transmitter PLL multiplies the input reference clock to generate a high-speed serial clock at a frequency that is half the data rate of the configured functional mode. This high-speed serial clock (or its divide-by-two version if the functional mode uses byte serializer) is fed to the CMU clock divider block. Depending on the configured functional mode, the CMU clock divider block divides the high-speed serial clock to generate the low-speed parallel clock that clocks the transceiver PCS logic in the associated channel. The low-speed parallel clock is also forwarded to the PLD logic array on the `tx_clkout` or `coreclkout` ports.

The receiver PLL in each channel is also fed by an input reference clock. The receiver PLL along with the clock recovery unit generates a high-speed serial recovered clock and a low-speed parallel recovered clock. The low-speed parallel recovered clock feeds the receiver PCS logic until the rate matcher. The CMU low-speed parallel clock clocks the rest of the logic from the rate matcher until the receiver phase compensation FIFO. In modes that do not use a rate matcher, the receiver PCS logic is clocked by the recovered clock until the receiver phase compensation FIFO.

The input reference clock to the transmitter and receiver PLLs can be derived from:

- One of two available dedicated reference clock input pins (`REFCLK0` or `REFCLK1`) of the associated transceiver block
- PLD clock network (must be driven directly from an input clock pin and cannot be driven by user logic or enhanced PLL)
- Inter-transceiver block lines driven by reference clock input pins of other transceiver blocks

Figure 2–22 shows the input reference clock sources for the transmitter and receiver PLL.

Figure 2–22. Input Reference Clock Sources

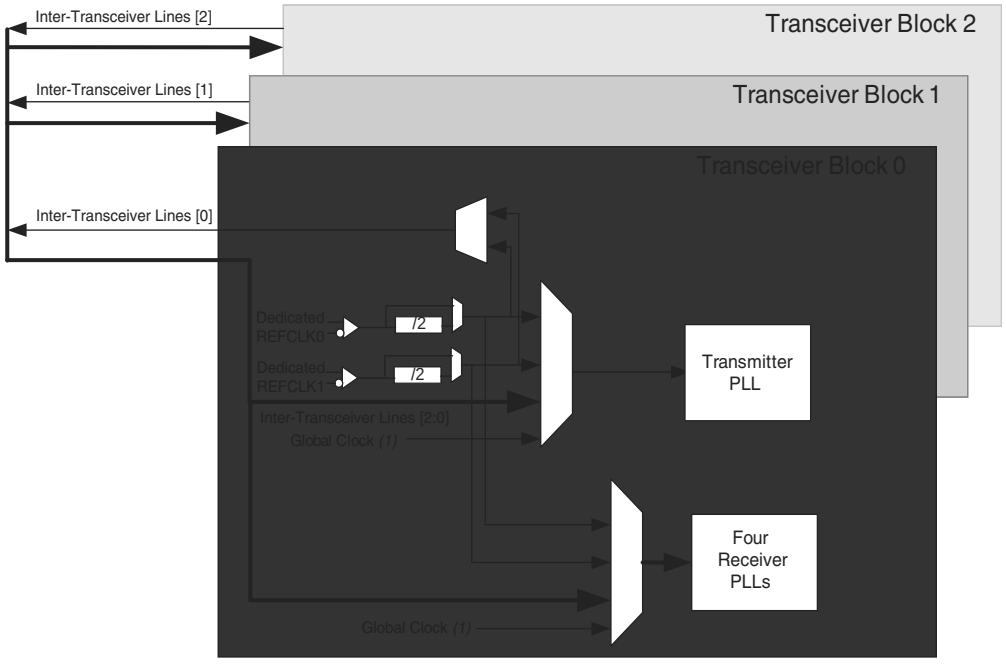
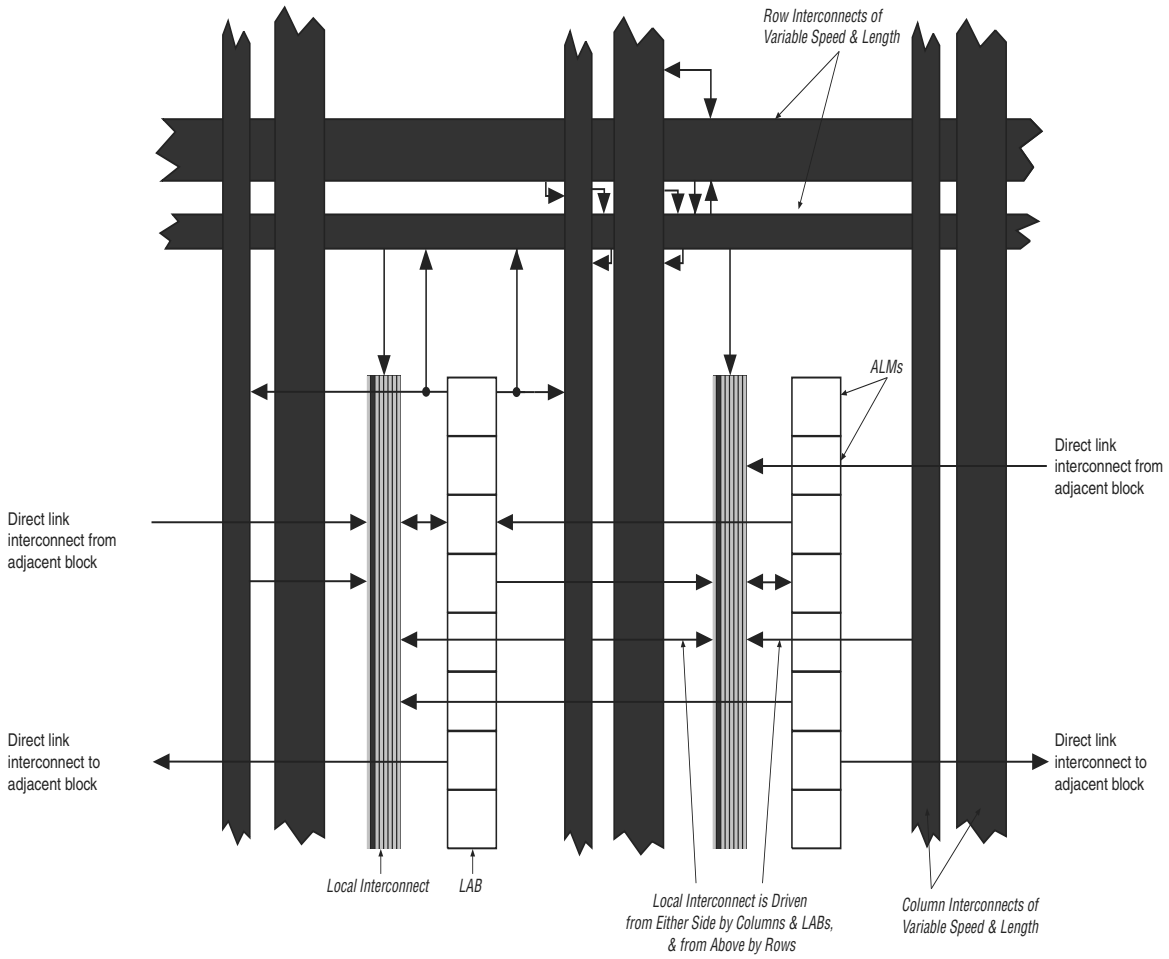


Figure 2–25. Arria GX LAB Structure



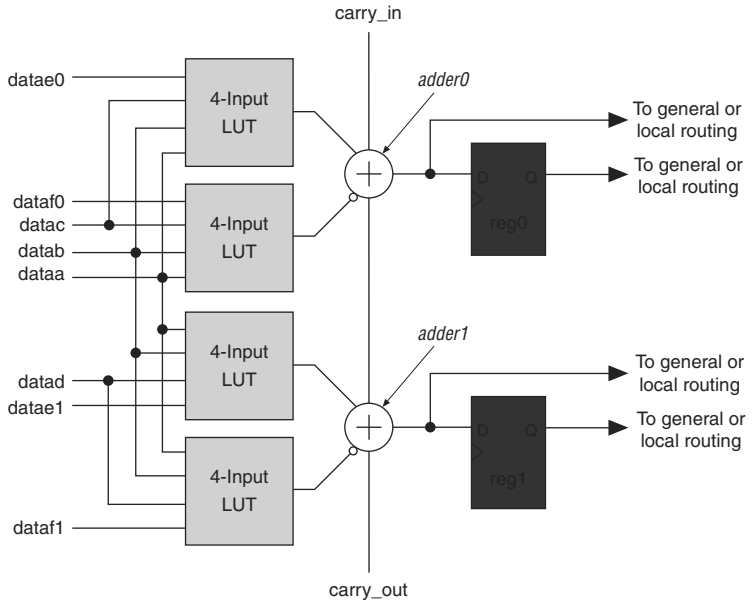
LAB Interconnects

The LAB local interconnect can drive all eight ALMs in the same LAB. It is driven by column and row interconnects and ALM outputs in the same LAB. Neighboring LABs, M512 RAM blocks, M4K RAM blocks, M-RAM blocks, or digital signal processing (DSP) blocks from the left and right can also drive the local interconnect of a LAB through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each ALM can drive 24 ALMs through fast local and direct link interconnects.

Arithmetic Mode

Arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. An ALM in arithmetic mode uses two sets of 2 four-input LUTs along with two dedicated full adders. The dedicated adders allow the LUTs to be available to perform pre-adder logic; therefore, each adder can add the output of two four-input functions. The four LUTs share the `dataa` and `datab` inputs. As shown in Figure 2–34, the carry-in signal feeds to `adder0`, and the carry-out from `adder0` feeds to carry-in of `adder1`. The carry-out from `adder1` drives to `adder0` of the next ALM in the LAB. ALMs in arithmetic mode can drive out registered and/or unregistered versions of the adder outputs.

Figure 2–34. ALM in Arithmetic Mode



While operating in arithmetic mode, the ALM can support simultaneous use of the adder's carry output along with combinational logic outputs. In this operation, adder output is ignored. This usage of the adder with the combinational logic output provides resource savings of up to 50% for functions that can use this ability. An example of such functionality is a conditional operation, such as the one shown in Figure 2–35. The equation for this example is:

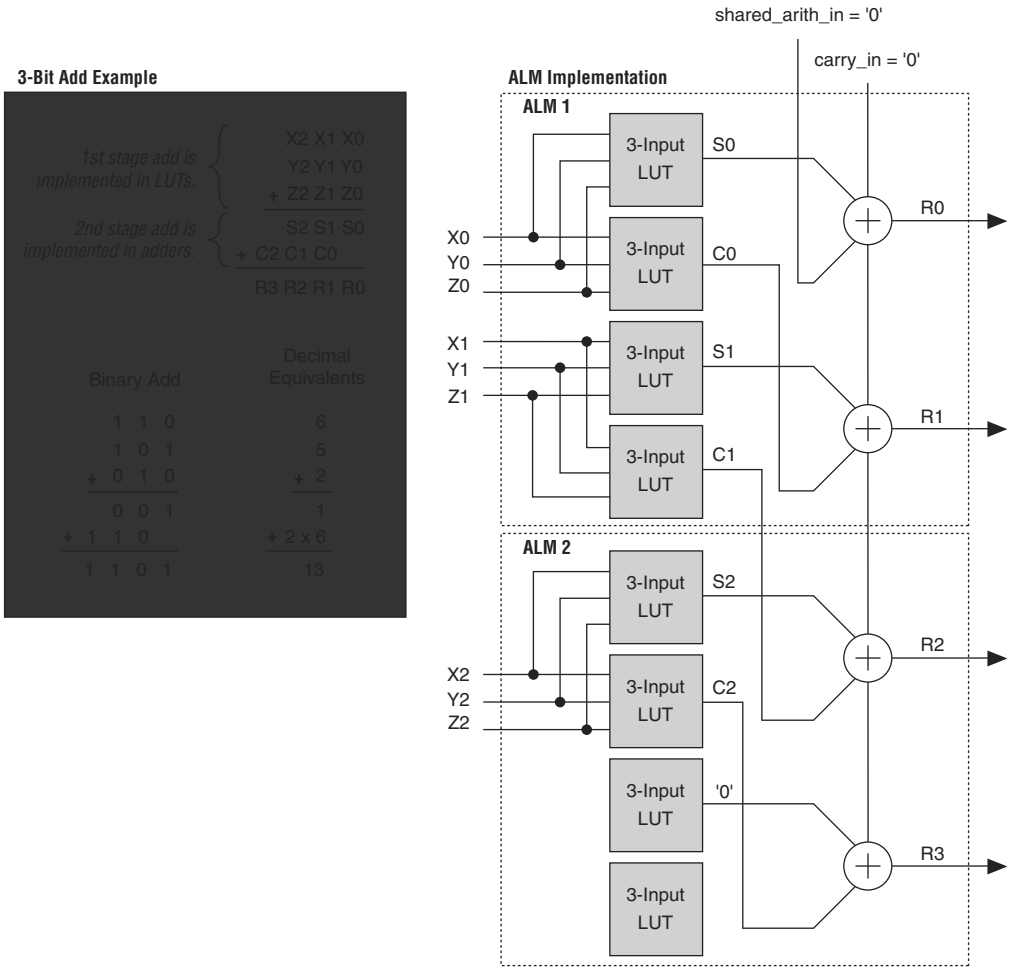
Equation 2–1.

$$R = (X < Y) ? Y : X$$

To implement this function, the adder is used to subtract 'Y' from 'X.' If 'X' is less than 'Y,' the `carry_out` signal is '1.' The `carry_out` signal is fed to an adder where it drives out to the LAB local interconnect. It then feeds to the LAB-wide `syncload` signal. When asserted, `syncload` selects the `syncdata` input. In this case, the data 'Y' drives the `syncdata` inputs to the registers. If 'X' is greater than or equal to 'Y,' the `syncload` signal is deasserted and 'X' drives the data port of the registers.

Adder trees are used in many different applications. For example, the summation of partial products in a logic-based multiplier can be implemented in a tree structure. Another example is a correlator function that can use a large adder tree to sum filtered data samples in a given time frame to recover or to de-spread data which was transmitted utilizing spread spectrum technology. An example of a three-bit add operation utilizing the shared arithmetic mode is shown in Figure 2–37. The partial sum (`S[2..0]`) and the partial carry (`C[2..0]`) is obtained using LUTs, while the result (`R[2..0]`) is computed using dedicated adders.

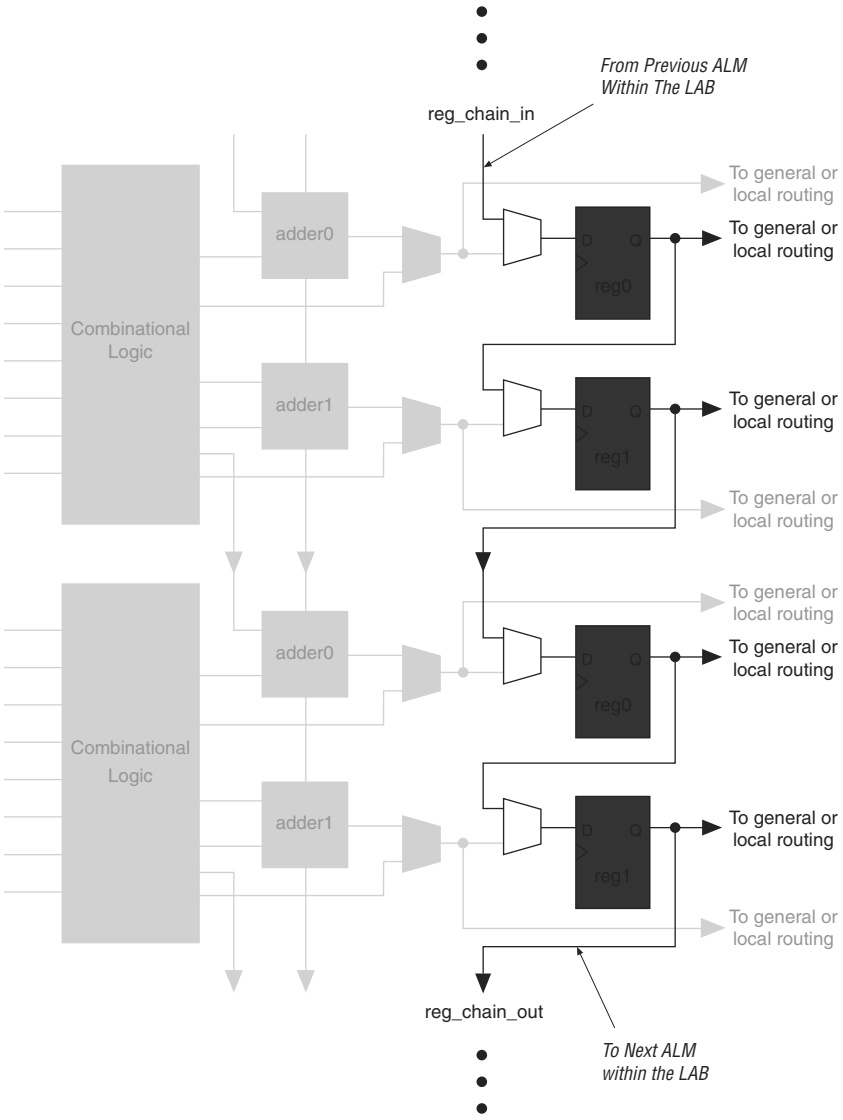
Figure 2–37. Example of a 3-Bit Add Utilizing Shared Arithmetic Mode



Shared Arithmetic Chain

In addition to dedicated carry chain routing, the shared arithmetic chain available in shared arithmetic mode allows the ALM to implement a three-input add, which significantly reduces the resources necessary to implement large adder trees or correlator functions. Shared arithmetic chains can begin in either the first or fifth ALM in a LAB. The Quartus II Compiler automatically links LABs to create shared arithmetic chains longer than 16 (eight ALMs in arithmetic or shared arithmetic mode). For enhanced fitting, a long shared arithmetic chain runs vertically allowing fast horizontal connections to TriMatrix memory and DSP blocks. A shared arithmetic chain can continue as far as a full column. Similar to carry chains, shared arithmetic

Figure 2–38. Register Chain within a LAB *(Note 1)*



Note to Figure 2–38:

(1) The combinational or adder logic can be used to implement an unrelated, unregistered function.

Clear and Preset Logic Control

LAB-wide signals control the logic for the register's clear and load/preset signals. The ALM directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. The direct asynchronous preset does not require a NOT gate push-back technique. Arria GX devices support simultaneous asynchronous load/preset and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one load/preset signal.

In addition to the clear and load/preset ports, Arria GX devices provide a device-wide reset pin (DEV_CLRn) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This device-wide reset overrides all other control signals.

MultiTrack Interconnect

In Arria GX architecture, the MultiTrack interconnect structure with DirectDrive technology provides connections between ALMs, TriMatrix memory, DSP blocks, and device I/O pins. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different lengths and speeds used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement in the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when migrating through different device densities. Dedicated row interconnects route signals to and from LABs, DSP blocks, and TriMatrix memory in the same row.

These row resources include:

- Direct link interconnects between LABs and adjacent blocks
- R4 interconnects traversing four blocks to the right or left
- R24 row interconnects for high-speed access across the length of the device

The direct link interconnect allows a LAB, DSP block, or TriMatrix memory block to drive into the local interconnect of its left and right neighbors and then back into itself, providing fast communication between adjacent LABs and/or blocks without using row interconnect resources.

The R4 interconnects span four LABs, three LABs and one M512 RAM block, two LABs and one M4K RAM block, or two LABs and one DSP block to the right or left of a source LAB. These resources are used for fast row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. Figure 2–39 shows R4 interconnect connections from a LAB.

R4 interconnects can drive and be driven by DSP blocks and RAM blocks and row IOEs. For LAB interfacing, a primary LAB or LAB neighbor can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive onto the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive onto the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. R4 interconnects can also drive C4 and C16 interconnects for connections from one row to another. Additionally, R4 interconnects can drive R24 interconnects.

Table 2–24 shows the possible settings for I/O standards with drive strength control.

Table 2–24. Programmable Drive Strength *(Note 1)*

I/O Standard	I_{OH} / I_{OL} Current Strength Setting (mA) for Column I/O Pins	I_{OH} / I_{OL} Current Strength Setting (mA) for Row I/O Pins
3.3-V LVTTL	24, 20, 16, 12, 8, 4	12, 8, 4
3.3-V LVCMOS	24, 20, 16, 12, 8, 4	8, 4
2.5-V LVTTL/LVCMOS	16, 12, 8, 4	12, 8, 4
1.8-V LVTTL/LVCMOS	12, 10, 8, 6, 4, 2	8, 6, 4, 2
1.5-V LVCMOS	8, 6, 4, 2	4, 2
SSTL-2 Class I	12, 8	12, 8
SSTL-2 Class II	24, 20, 16	16
SSTL-18 Class I	12, 10, 8, 6, 4	10, 8, 6, 4
SSTL-18 Class II	20, 18, 16, 8	—
HSTL-18 Class I	12, 10, 8, 6, 4	12, 10, 8, 6, 4
HSTL-18 Class II	20, 18, 16	—
HSTL-15 Class I	12, 10, 8, 6, 4	8, 6, 4
HSTL-15 Class II	20, 18, 16	—

Note to Table 2–24:

(1) The Quartus II software default current setting is the maximum setting for each I/O standard.

Open-Drain Output

Arria GX devices provide an optional open-drain (equivalent to an open collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (for example, interrupt and write enable signals) that can be asserted by any of several devices.

Bus Hold

Each Arria GX device I/O pin provides an optional bus-hold feature. Bus-hold circuitry can hold the signal on an I/O pin at its last-driven state. Because the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not needed to hold a signal level when the bus is tri-stated.

Bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output drives no higher than V_{CCIO} to prevent overdriving signals. If the bus-hold feature is enabled, the programmable pull-up option cannot be used. Disable the bus-hold feature when the I/O pin has been configured for differential signals.

Bus-hold circuitry uses a resistor with a nominal resistance (RBH) of approximately 7 kΩ to pull the signal level to the last-driven state. This information is provided for each V_{CCIO} voltage level. Bus-hold circuitry is active only after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

Document Revision History

Table 2–35 shows the revision history for this chapter.

Table 2–35. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
December 2009, v2.0	■ Document template update. ■ Minor text edits.	—
May 2008, v1.3	Added "Reverse Serial Pre-CDR Loopback" and "Calibration Block" sub-sections to "Transmitter Path" section.	—
August 2007, v1.2	Added "Referenced Documents" section.	—
June 2007, v1.1	Added GIGE information.	—
May 2007 v1.0	Initial release.	—

Table 4–9. PCS Latency (Part 2 of 2) (Part 2 of 2)

Functional Mode	Configuration	Receiver PCS Latency									
		Word Aligner	Deskew FIFO	Rate Matcher *(3)*	8B/10B Decoder	Receiver State Machine	Byte Deserializer	Byte Order	Receiver Phase Comp FIFO	Receiver PIPE	Sum *(2)*
BASIC Single Width	8/10-bit channel width; with Rate Matcher	4–5	—	11–13	1	—	1	1	1–2	1	19–23
	8/10-bit channel width; without Rate Matcher	4–5	—	—	1	—	1	1	1–2	—	8–10
	16/20-bit channel width; with Rate Matcher	2–2.5	—	5.5–6.5	0.5	—	1	1	1–2	—	11–14
	16/20-bit channel width; without Rate Matcher	2–2.5	—	—	0.5	—	1	1	1–2	—	6–7

Notes to Table 4–9:

(1) The latency numbers are with respect to the PLD-transceiver interface clock cycles.

(2) The total latency number is rounded off in the Sum column.

(3) The rate matcher latency shown is the steady state latency. Actual latency may vary depending on the skip ordered set gap allowed by the protocol, actual PPM difference between the reference clocks, and so forth.

Table 4–10 through Table 4–13 show the typical V_{OD} for data rates from 600 Mbps to 3.125 Gbps. The specification is for measurement at the package ball.

Table 4–10. Typical V_{OD} Setting, TX Term = 100 Ω

V_{cc} HTX = 1.5 V	V_{OD} Setting (mV)				
	400	600	800	1000	1200
V_{OD} Typical (mV)	430	625	830	1020	1200

Table 4–11. Typical V_{OD} Setting, TX Term = 100 Ω

V_{cc} HTX = 1.2 V	V_{OD} Setting (mV)				
	320	480	640	800	960
V_{OD} Typical (mV)	344	500	664	816	960

Table 4–12. Typical Pre-Emphasis (First Post-Tap), *(Note 1)*

V_{cc} HTX = 1.5 V	First Post Tap Pre-Emphasis Level				
V_{OD} Setting (mV)	1	2	3	4	5
	TX Term = 100 Ω				
400	24%	62%	112%	184%	—
600	—	31%	56%	86%	122%
800	—	20%	35%	53%	73%

Table 4–21. 3.3-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO} *(1)*	I/O supply voltage for top and bottom PLL banks (9, 10, 11, and 12)	—	3.135	3.3	3.465	V
V_{ID}	Input differential voltage swing (single-ended)	—	100	350	900	mV
V_{ICM}	Input common mode voltage	—	200	1,250	1,800	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	250	—	710	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	840	—	1,570	mV
R_L	Receiver differential input discrete resistor (external to Arria GX devices)	—	90	100	110	Ω

Note to Table 4–21:

(1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT}, not V_{CCIO}. The PLL clock output/feedback differential buffers are powered by VCC_PLL_OUT. For differential clock output/feedback operation, connect VCC_PLL_OUT to 3.3 V.

Table 4–22. 3.3-V PCML Specifications

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage	3.135	3.3	3.465	V
V_{ID}	Input differential voltage swing (single-ended)	300	—	600	mV
V_{ICM}	Input common mode voltage	1.5	—	3.465	V
V_{OD}	Output differential voltage (single-ended)	300	370	500	mV
ΔV_{OD}	Change in V_{OD} between high and low	—	—	50	mV
V_{OCM}	Output common mode voltage	2.5	2.85	3.3	V
ΔV_{OCM}	Change in V_{OCM} between high and low	—	—	50	mV
V_T	Output termination voltage	—	V_{CCIO}	—	V
R_1	Output external pull-up resistors	45	50	55	Ω
R_2	Output external pull-up resistors	45	50	55	Ω

Table 4–23. LVPECL Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units	Parameter
V_{CCIO} *(1)*	I/O supply voltage	—	3.135	3.3	3.465	V
V_{ID}	Input differential voltage swing (single-ended)	—	300	600	1,000	mV
V_{ICM}	Input common mode voltage	—	1.0	—	2.5	V
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	525	—	970	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	1,650	—	2,250	mV
R_L	Receiver differential input resistor	—	90	100	110	Ω

Note to Table 4–23:

(1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT}, not V_{CCIO}. The PLL clock output/feedback differential buffers are powered by VCC_PLL_OUT. For differential clock output/feedback operation, connect VCC_PLL_OUT to 3.3 V.

Figure 4–9. Measurement Setup for t_{zx}

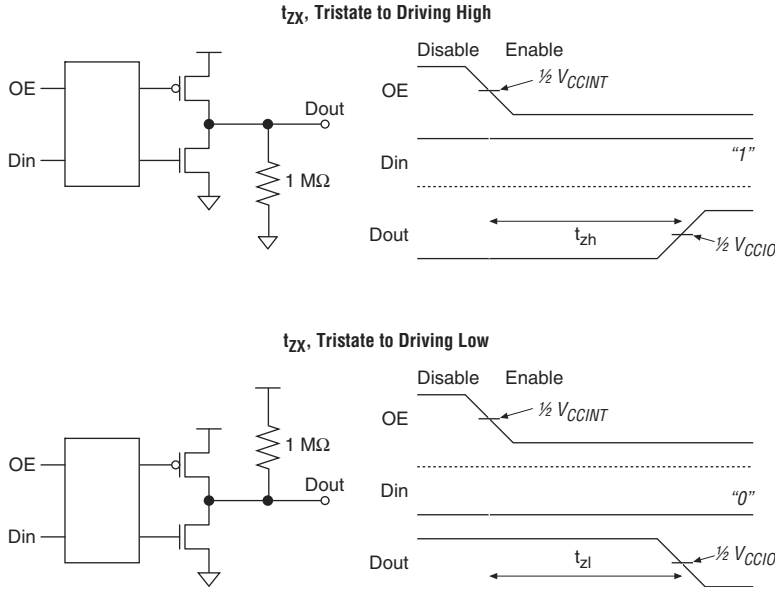


Table 4–45 specifies the input timing measurement setup.

Table 4–45. Timing Measurement Methodology for Input Pins *(Note 1)*, *(2)*, *(3)*, *(4)* (Part 1 of 2)

I/O Standard	Measurement Conditions			Measurement Point
	V_{CCIO} (V)	V_{REF} (V)	Edge Rate (ns)	VMEAS (V)
LVTTL *(5)*	3.135	—	3.135	1.5675
LVCMOS *(5)*	3.135	—	3.135	1.5675
2.5 V *(5)*	2.375	—	2.375	1.1875
1.8 V *(5)*	1.710	—	1.710	0.855
1.5 V *(5)*	1.425	—	1.425	0.7125
PCI *(6)*	2.970	—	2.970	1.485
PCI-X *(6)*	2.970	—	2.970	1.485
SSTL-2 Class I	2.325	1.163	2.325	1.1625
SSTL-2 Class II	2.325	1.163	2.325	1.1625
SSTL-18 Class I	1.660	0.830	1.660	0.83
SSTL-18 Class II	1.660	0.830	1.660	0.83
1.8-V HSTL Class I	1.660	0.830	1.660	0.83
1.8-V HSTL Class II	1.660	0.830	1.660	0.83
1.5-V HSTL Class I	1.375	0.688	1.375	0.6875
1.5-V HSTL Class II	1.375	0.688	1.375	0.6875
1.2-V HSTL with OCT	1.140	0.570	1.140	0.570
Differential SSTL-2 Class I	2.325	1.163	2.325	1.1625
Differential SSTL-2 Class II	2.325	1.163	2.325	1.1625
Differential SSTL-18 Class I	1.660	0.830	1.660	0.83

Table 4–66. EP1AGX60 Row Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Model		–6 Speed Grade	Units
			Industrial	Commercial		
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.281	1.281	2.777	ns
		t_H	–1.176	–1.176	–2.500	ns
	GCLK PLL	t_{SU}	2.853	2.853	6.220	ns
		t_H	–2.748	–2.748	–5.943	ns
LVDS	GCLK	t_{SU}	1.208	1.208	2.664	ns
		t_H	–1.103	–1.103	–2.387	ns
	GCLK PLL	t_{SU}	2.767	2.767	6.083	ns
		t_H	–2.662	–2.662	–5.806	ns

Table 4–67 lists I/O timing specifications.

Table 4–67. EP1AGX60 Column Pins Input Timing Parameters (Part 1 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
3.3-V LVTTL	GCLK	t_{SU}	1.124	1.124	2.493	ns
		t_H	–1.019	–1.019	-2.216	ns
	GCLK PLL	t_{SU}	2.694	2.694	5.928	ns
		t_H	–2.589	–2.589	-5.651	ns
3.3-V LVCMOS	GCLK	t_{SU}	1.124	1.124	2.493	ns
		t_H	–1.019	–1.019	-2.216	ns
	GCLK PLL	t_{SU}	2.694	2.694	5.928	ns
		t_H	–2.589	–2.589	-5.651	ns
2.5 V	GCLK	t_{SU}	1.134	1.134	2.475	ns
		t_H	–1.029	–1.029	-2.198	ns
	GCLK PLL	t_{SU}	2.704	2.704	5.910	ns
		t_H	–2.599	–2.599	-5.633	ns
1.8 V	GCLK	t_{SU}	1.200	1.200	2.685	ns
		t_H	–1.095	–1.095	-2.408	ns
	GCLK PLL	t_{SU}	2.770	2.770	6.120	ns
		t_H	–2.665	–2.665	-5.843	ns
1.5 V	GCLK	t_{SU}	1.203	1.203	2.778	ns
		t_H	–1.098	–1.098	-2.501	ns
	GCLK PLL	t_{SU}	2.773	2.773	6.213	ns
		t_H	–2.668	–2.668	-5.936	ns
SSTL-2 CLASS I	GCLK	t_{SU}	0.948	0.948	1.951	ns
		t_H	–0.843	–0.843	-1.674	ns
	GCLK PLL	t_{SU}	2.519	2.519	5.388	ns
		t_H	–2.414	–2.414	-5.111	ns

Table 4–67. EP1AGX60 Column Pins Input Timing Parameters (Part 2 of 3)

I/O Standard	Clock	Parameter	Fast Corner		–6 Speed Grade	Units
			Industrial	Commercial		
SSTL-2 CLASS II	GCLK	t_{SU}	0.948	0.948	1.951	ns
		t_H	–0.843	–0.843	–1.674	ns
	GCLK PLL	t_{SU}	2.519	2.519	5.388	ns
		t_H	–2.414	–2.414	–5.111	ns
SSTL-18 CLASS I	GCLK	t_{SU}	0.986	0.986	2.057	ns
		t_H	–0.881	–0.881	–1.780	ns
	GCLK PLL	t_{SU}	2.556	2.556	5.492	ns
		t_H	–2.451	–2.451	–5.215	ns
SSTL-18 CLASS II	GCLK	t_{SU}	0.987	0.987	2.058	ns
		t_H	–0.882	–0.882	–1.781	ns
	GCLK PLL	t_{SU}	2.558	2.558	5.495	ns
		t_H	–2.453	–2.453	–5.218	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	0.986	0.986	2.057	ns
		t_H	–0.881	–0.881	–1.780	ns
	GCLK PLL	t_{SU}	2.556	2.556	5.492	ns
		t_H	–2.451	–2.451	–5.215	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	0.987	0.987	2.058	ns
		t_H	–0.882	–0.882	–1.781	ns
	GCLK PLL	t_{SU}	2.558	2.558	5.495	ns
		t_H	–2.453	–2.453	–5.218	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	1.004	1.004	2.185	ns
		t_H	–0.899	–0.899	–1.908	ns
	GCLK PLL	t_{SU}	2.574	2.574	5.620	ns
		t_H	–2.469	–2.469	–5.343	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	1.005	1.005	2.186	ns
		t_H	–0.900	–0.900	–1.909	ns
	GCLK PLL	t_{SU}	2.576	2.576	5.623	ns
		t_H	–2.471	–2.471	–5.346	ns
3.3-V PCI	GCLK	t_{SU}	1.129	1.129	2.481	ns
		t_H	–1.024	–1.024	–2.204	ns
	GCLK PLL	t_{SU}	2.699	2.699	5.916	ns
		t_H	–2.594	–2.594	–5.639	ns
3.3-V PCI-X	GCLK	t_{SU}	1.129	1.129	2.481	ns
		t_H	–1.024	–1.024	–2.204	ns
	GCLK PLL	t_{SU}	2.699	2.699	5.916	ns
		t_H	–2.594	–2.594	–5.639	ns

Table 4–93 through Table 4–94 list the RCLK clock timing parameters for EP1AGX60 devices.

Table 4–93 lists clock timing specifications.

Table 4–93. EP1AGX60 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.382	1.382	3.268	ns
t_{COUT}	1.387	1.387	3.262	ns
t_{PLLCIN}	–0.031	–0.031	0.174	ns
$t_{PLLCOUT}$	–0.026	–0.026	0.168	ns

Table 4–94 lists clock timing specifications.

Table 4–94. EP1AGX60 Row Pins Regional Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.649	1.649	3.835	ns
t_{COUT}	1.651	1.651	3.839	ns
t_{PLLCIN}	0.245	0.245	0.755	ns
$t_{PLLCOUT}$	0.245	0.245	0.755	ns

EP1AGX90 Clock Timing Parameters

Table 4–95 through Table 4–96 list the GCLK clock timing parameters for EP1AGX90 devices.

Table 4–95 lists clock timing specifications.

Table 4–95. EP1AGX90 Row Pins Global Clock Timing Parameters

Parameter	Fast Model		–6 Speed Grade	Units
	Industrial	Commercial		
t_{CIN}	1.630	1.630	3.799	ns
t_{COUT}	1.635	1.635	3.793	ns
t_{PLLCIN}	–0.422	–0.422	–0.310	ns
$t_{PLLCOUT}$	–0.417	–0.417	–0.316	ns

Table 4–104. Arria GX Maximum Input Clock Rate for Dedicated Clock Pins (Part 2 of 2)

I/O Standards	–6 Speed Grade	Units
3.3-V PCI-X	373	MHz
SSTL-18 CLASS I	467	MHz
SSTL-18 CLASS II	467	MHz
1.8-V HSTL CLASS I	467	MHz
1.8-V HSTL CLASS II	467	MHz
1.5-V HSTL CLASS I	467	MHz
1.5-V HSTL CLASS II	467	MHz
1.2-V HSTL	233	MHz
DIFFERENTAL SSTL-2	467	MHz
DIFFERENTIAL 2.5-V SSTL CLASS II	467	MHz
DIFFERENTIAL 1.8-V SSTL CLASS I	467	MHz
DIFFERENTIAL 1.8-V SSTL CLASS II	467	MHz
DIFFERENTIAL 1.8-V HSTL CLASS I	467	MHz
DIFFERENTIAL 1.8-V HSTL CLASS II	467	MHz
DIFFERENTIAL 1.5-V HSTL CLASS I	467	MHz
DIFFERENTIAL 1.5-V HSTL CLASS II	467	MHz
DIFFERENTIAL 1.2-V HSTL	233	MHz
LVDS	640	MHz
LVDS *(1)*	373	MHz

Note to Table 4–104:

(1) This set of numbers refers to the VIO dedicated input clock pins.

Table 4–105 shows the maximum output clock toggle rates for Arria GX device column I/O pins.

Table 4–105. Arria GX Maximum Output Toggle Rate for Column I/O Pins (Part 1 of 3)

I/O Standards	Drive Strength	–6 Speed Grade	Units
3.3-V LVTTL	4 mA	196	MHz
	8 mA	303	MHz
	12 mA	393	MHz
	16 mA	486	MHz
	20 mA	570	MHz
	24 mA	626	MHz

Table 4–105. Arria GX Maximum Output Toggle Rate for Column I/O Pins (Part 2 of 3)

I/O Standards	Drive Strength	–6 Speed Grade	Units
3.3-V LVCMOS	4 mA	215	MHz
	8 mA	411	MHz
	12 mA	626	MHz
	16 mA	819	MHz
	20 mA	874	MHz
	24 mA	934	MHz
2.5 V	4 mA	168	MHz
	8 mA	355	MHz
	12 mA	514	MHz
	16 mA	766	MHz
1.8 V	2 mA	97	MHz
	4 mA	215	MHz
	6 mA	336	MHz
	8 mA	486	MHz
	10 mA	706	MHz
	12 mA	925	MHz
1.5 V	2 mA	168	MHz
	4 mA	303	MHz
	6 mA	350	MHz
	8 mA	392	MHz
SSTL-2 CLASS I	8 mA	280	MHz
	12 mA	327	MHz
SSTL-2 CLASS II	16 mA	280	MHz
	20 mA	327	MHz
	24 mA	327	MHz
SSTL-18 CLASS I	4 mA	140	MHz
	6 mA	186	MHz
	8 mA	280	MHz
	10 mA	373	MHz
	12 mA	373	MHz
SSTL-18 CLASS II	8 mA	140	MHz
	16 mA	327	MHz
	18 mA	373	MHz
	20 mA	420	MHz
1.8-V HSTL CLASS I	4 mA	280	MHz
	6 mA	420	MHz
	8 mA	561	MHz
	10 mA	561	MHz
	12 mA	607	MHz

Table 4–121. DQS Bus Clock Skew Adder Specifications ($t_{DQS\_CLOCK\_SKEW\_ADDER}$)

Mode	DQS Clock Skew Adder (ps)
4 DQ per DQS	40
9 DQ per DQS	70
18 DQ per DQS	75
36 DQ per DQS	95

Table 4–122. DQS Phase Offset Delay Per Stage (ps) *Note (1), (2), (3)*

Speed Grade	Positive Offset		Negative Offset	
	Min	Max	Min	Max
–6	10	16	8	12

Notes to Table 4–122:

(1) The delay settings are linear.
(2) The valid settings for phase offset are –32 to +31.
(3) The typical value equals the average of the minimum and maximum values.

JTAG Timing Specifications

Figure 4–13 shows the timing requirements for the JTAG signals

Figure 4–13. Arria GX JTAG Waveforms.

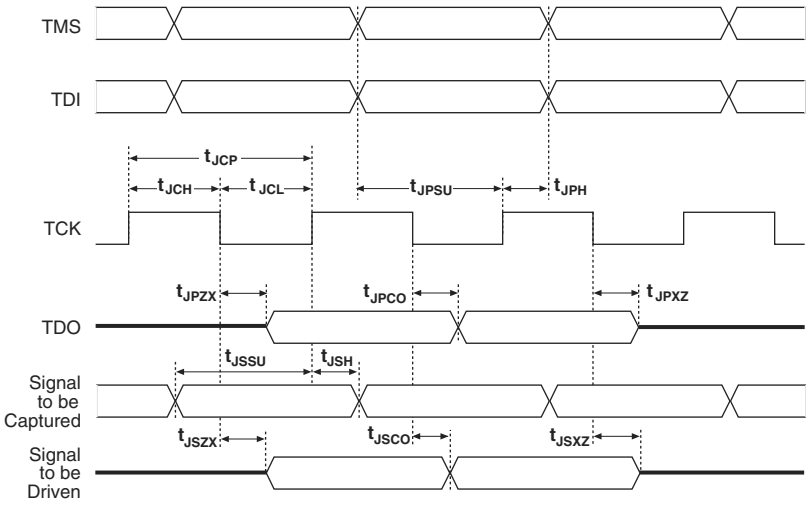


Table 4–123 lists the JTAG timing parameters and values for Arria GX devices.

Table 4–123. Arria GX JTAG Timing Parameters and Values

Symbol	Parameter	Min	Max	Units
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	12	—	ns
t_{JCL}	TCK clock low time	12	—	ns
t_{JPSU}	JTAG port setup time	4	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	9	ns
t_{JPZX}	JTAG port high impedance to valid output	—	9	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	9	ns
t_{JSSU}	Capture register setup time	4	—	ns
t_{JSH}	Capture register hold time	5	—	ns
t_{JSCO}	Update register clock to output	—	12	ns
t_{JSZX}	Update register high impedance to valid output	—	12	ns
t_{JSXZ}	Update register valid output to high impedance	—	12	ns