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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

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Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	EBI/EMI, I <sup>2</sup> C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	40
Program Memory Size	384KB (384K × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	34K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-LQFP-64-13
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xe162hm-48f80l-aa

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



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#### **Summary of Features**

### **Ordering Information**

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. This ordering code identifies:

- the function set of the corresponding product type
- the temperature range:
  - SAF-...: -40°C to 85°C
- the package and the type of delivery.

For ordering codes for the XE162xM please contact your sales representative or local distributor.

This document describes several derivatives of the XE162xM group:

 Table 1 lists these derivatives and summarizes the differences.

As this document refers to all of these derivatives, some descriptions may not apply to a specific product, in particular to the special device types.

For simplicity the term XE162xM is used for all derivatives throughout this document.

XE162xM device types are available and can be ordered through Infineon's direct and/or distribution channels.



#### **Summary of Features**

## 1.2 Definition of Feature Variants

The XE162xM types are offered with several Flash memory sizes. **Table 2** describes the location of the available memory areas for each Flash memory size.

Total Flash Size	Flash Area A <sup>1)</sup>	Flash Area B	Flash Area C
576 Kbytes	C0'0000 <sub>H</sub>	C1'0000 <sub>H</sub>	СС'0000 <sub>н</sub>
	C0'EFFF <sub>H</sub>	C7'FFFF <sub>H</sub>	СС'FFFF <sub>н</sub>
384 Kbytes	C0'0000 <sub>H</sub>	C1'0000 <sub>H</sub>	СС'0000 <sub>н</sub>
	C0'EFFF <sub>H</sub>	C4'FFFF <sub>H</sub>	СС'FFFF <sub>н</sub>
192 Kbytes	C0'0000 <sub>H</sub>	C1'0000 <sub>H</sub>	СС'0000 <sub>н</sub>
	C0'EFFF <sub>H</sub>	C1'FFFF <sub>H</sub>	СС'FFFF <sub>н</sub>

#### Table 2 Flash Memory Allocation

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000<sub>H</sub> to C0'FFFF<sub>H</sub>).

Table 3	Flash Memory	Module Allocation	(in Kbv	tes)
		medale / medalen		

Total Flash Size	Flash 0 <sup>1)</sup>	Flash 1	Flash 2	Flash 3
576 Kbytes	256	256		64
384 Kbytes	256	64		64
192 Kbytes	128			64

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000<sub>H</sub> to C0'FFFF<sub>H</sub>).

The XE162xM types are offered with different interface options. Table 4 lists the available channels for each option.

Table 4	Interface	Channel	Association

Total Number	Available Channels	
7 ADC0 channels	CH0, CH2, CH4, CH8, CH10, CH13, CH15	
2 ADC1 channels	CH0, CH4	
2 CAN nodes	CAN0, CAN1 64 message objects	
6 serial channels	U0C0, U0C1, U1C0, U1C1, U2C0, U2C1	



## XE162FM, XE162HM XE166 Family / Base Line

## **General Device Information**

Table	Fin Definitions and Functions (cont'd)						
Pin	Symbol	Ctrl.	Туре	Function			
28	P2.3	O0 / I	St/B	Bit 3 of Port 2, General Purpose Input/Output			
	U0C0_DOUT	01	St/B	USIC0 Channel 0 Shift Data Output			
	CC2_CC16	O3 / I	St/B	CAPCOM2 CC16IO Capture Inp./ Compare Out.			
	ESR2_0	I	St/B	ESR2 Trigger Input 0			
	U0C0_DX0E	I	St/B	USIC0 Channel 0 Shift Data Input			
	U0C1_DX0D	I	St/B	USIC0 Channel 1 Shift Data Input			
_	RxDC0A	Ι	St/B	CAN Node 0 Receive Data Input			
29	P2.4	O0 / I	St/B	Bit 4 of Port 2, General Purpose Input/Output			
	U0C1_DOUT	01	St/B	USIC0 Channel 1 Shift Data Output			
	TxDC0	02	St/B	CAN Node 0 Transmit Data Output			
	CC2_CC17	O3 / I	St/B	CAPCOM2 CC17IO Capture Inp./ Compare Out.			
	ESR1_0	I	St/B	ESR1 Trigger Input 0			
	U0C0_DX0F	I	St/B	USIC0 Channel 0 Shift Data Input			
	RxDC1A	I	St/B	CAN Node 1 Receive Data Input			
30	P2.5	O0 / I	St/B	Bit 5 of Port 2, General Purpose Input/Output			
	U0C0_SCLK OUT	O1	St/B	USIC0 Channel 0 Shift Clock Output			
	TxDC0	02	St/B	CAN Node 0 Transmit Data Output			
	CC2_CC18	O3 / I	St/B	CAPCOM2 CC18IO Capture Inp./ Compare Out.			
	U0C0_DX1D	I	St/B	USIC0 Channel 0 Shift Clock Input			
_	ESR1_10	I	St/B	ESR1 Trigger Input 10			
31	P2.6	O0 / I	St/B	Bit 6 of Port 2, General Purpose Input/Output			
	U0C0_SELO 0	O1	St/B	USIC0 Channel 0 Select/Control 0 Output			
	U0C1_SELO 1	O2	St/B	USIC0 Channel 1 Select/Control 1 Output			
	CC2_CC19	O3 / I	St/B	CAPCOM2 CC19IO Capture Inp./ Compare Out.			
	U0C0_DX2D	I	St/B	USIC0 Channel 0 Shift Control Input			
	RxDC0D	I	St/B	CAN Node 0 Receive Data Input			
	ESR2_6	I	St/B	ESR2 Trigger Input 6			



## **General Device Information**

Pin	Symbol	Ctrl.	Туре	Function		
62	PORST	1	In/B	<b>Power On Reset Input</b> A low level at this pin resets the XE162xM completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns. An internal pull-up device will hold this pin high when nothing is driving it.		
63	ESR0	O0 / I	St/B	<b>External Service Request 0</b> After power-up, ESR0 operates as open-drain bidirectional reset with a weak pull-up.		
	U1C0_DX0E	I	St/B	USIC1 Channel 0 Shift Data Input		
	U1C0_DX2B	I	St/B	USIC1 Channel 0 Shift Control Input		
6	V <sub>DDIM</sub>	-	PS/M	<b>Digital Core Supply Voltage for Domain M</b> Decouple with a ceramic capacitor, see Data Sheet for details.		
24, 41, 57	V <sub>DDI1</sub>	-	PS/1	<b>Digital Core Supply Voltage for Domain 1</b> Decouple with a ceramic capacitor, see Data Sheet for details. All $V_{\text{DD11}}$ pins must be connected to each other.		
9	V <sub>DDPA</sub>	-	PS/A	Digital Pad Supply Voltage for Domain A Connect decoupling capacitors to adjacent V <sub>DDP</sub> /V <sub>SS</sub> pin pairs as close as possible to the pins. Note: The A/D_Converters and ports P5, P6 and P15 are fed from supply voltage V <sub>DDPA</sub> .		

# Table 5 Pin Definitions and Functions (cont'd)



## 3 Functional Description

The architecture of the XE162xM combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a well-balanced design. On-chip memory blocks allow the design of compact systems-on-silicon with maximum performance suited for computing, control, and communication.

The on-chip memory blocks (program code memory and SRAM, dual-port RAM, data SRAM) and the generic peripherals are connected to the CPU by separate high-speed buses. Another bus, the LXBus, connects additional on-chip resources and external resources (see **Figure 4**). This bus structure enhances overall system performance by enabling the concurrent operation of several subsystems of the XE162xM.

The block diagram gives an overview of the on-chip components and the advanced internal bus structure of the XE162xM.



Figure 4 Block Diagram



Compare Modes	Function
Mode 2	Interrupt-only compare mode; Only one compare interrupt per timer period is generated
Mode 3	Pin set '1' on match; pin reset '0' on compare timer overflow; Only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; Pin toggles on each compare match; Several compare events per timer period are possible
Single Event Mode	Generates single edges or pulses; Can be used with any compare mode

## Table 8 Compare Modes (cont'd)



## XE162FM, XE162HM XE166 Family / Base Line

### **Functional Description**



Figure 6 CAPCOM2 Unit Block Diagram

![](_page_9_Picture_0.jpeg)

## XE162FM, XE162HM XE166 Family / Base Line

## **Functional Description**

![](_page_9_Figure_3.jpeg)

### Figure 7 CCU6 Block Diagram

Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns that can be modulated by timer T12 and/or timer T13. The modulation sources can be selected and combined for signal modulation.

![](_page_10_Picture_0.jpeg)

With its maximum resolution of 2 system clock cycles, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The counting direction (up/down) for each timer can be programmed by software or altered dynamically with an external signal on a port pin (TxEUD). Concatenation of the timers is supported with the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can also be used to clock the CAPCOM2 timers and to initiate a reload from the CAPREL register.

The CAPREL register can capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN); timer T5 may optionally be cleared after the capture procedure. This allows the XE162xM to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) can also be generated upon transitions of GPT1 timer T3 inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

![](_page_11_Picture_0.jpeg)

## 3.11 A/D Converters

For analog signal measurement, up to two 10-bit A/D converters (ADC0, ADC1) with 7 + 2 multiplexed input channels and a sample and hold circuit have been integrated onchip. 2 inputs can be converted by both A/D converters. Conversions use the successive approximation method. The sample time (to charge the capacitors) and the conversion time are programmable so that they can be adjusted to the external circuit. The A/D converters can also operate in 8-bit conversion mode, further reducing the conversion time.

Several independent conversion result registers, selectable interrupt requests, and highly flexible conversion sequences provide a high degree of programmability to meet the application requirements. Both modules can be synchronized to allow parallel sampling of two input channels.

For applications that require more analog input channels, external analog multiplexers can be controlled automatically. For applications that require fewer analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converters of the XE162xM support two types of request sources which can be triggered by several internal and external events.

- Parallel requests are activated at the same time and then executed in a predefined sequence.
- Queued requests are executed in a user-defined sequence.

In addition, the conversion of a specific channel can be inserted into a running sequence without disturbing that sequence. All requests are arbitrated according to the priority level assigned to them.

Data reduction features reduce the number of required CPU access operations allowing the precise evaluation of analog inputs (high conversion rate) even at a low CPU speed. Result data can be reduced by limit checking or accumulation of results.

The Peripheral Event Controller (PEC) can be used to control the A/D converters or to automatically store conversion results to a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer. Each A/D converter contains eight result registers which can be concatenated to build a result FIFO. Wait-for-read mode can be enabled for each result register to prevent the loss of conversion data.

In order to decouple analog inputs from digital noise and to avoid input trigger noise, those pins used for analog input can be disconnected from the digital input stages. This can be selected for each pin separately with the Port x Digital Input Disable registers.

The Auto-Power-Down feature of the A/D converters minimizes the power consumption when no conversion is in progress.

Broken wire detection for each channel and a multiplexer test mode provide information to verify the proper operation of the analog signal sources (e.g. a sensor system).

![](_page_12_Picture_0.jpeg)

#### **MultiCAN Features**

- CAN functionality conforming to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Independent CAN nodes
- Set of independent message objects (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to 1 Mbit/s, individually programmable for each node
- · Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality for message objects:
  - Can be assigned to one of the CAN nodes
  - Configurable as transmit or receive objects, or as message buffer FIFO
  - Handle 11-bit or 29-bit identifiers with programmable acceptance mask for filtering
  - Remote Monitoring Mode, and frame counter for monitoring
- Automatic Gateway Mode support
- 16 individually programmable interrupt nodes
- Analyzer mode for CAN bus monitoring

## 3.14 System Timer

The System Timer consists of a programmable prescaler and two concatenated timers (10 bits and 6 bits). Both timers can generate interrupt requests. The clock source can be selected and the timers can also run during power reduction modes.

Therefore, the System Timer enables the software to maintain the current time for scheduling functions or for the implementation of a clock.

![](_page_13_Picture_0.jpeg)

## 3.15 Watchdog Timer

The Watchdog Timer is one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after an application reset of the chip. It can be disabled and enabled at any time by executing the instructions DISWDT and ENWDT respectively. The software has to service the Watchdog Timer before it overflows. If this is not the case because of a hardware or software failure, the Watchdog Timer overflows, generating a prewarning interrupt and then a reset request.

The Watchdog Timer is a 16-bit timer clocked with the system clock divided by 16,384 or 256. The Watchdog Timer register is set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the Watchdog Timer is reloaded and the prescaler is cleared.

Time intervals between 3.2  $\mu$ s and 13.42 s can be monitored (@ 80 MHz). The default Watchdog Timer interval after power-up is 6.5 ms (@ 10 MHz).

## 3.16 Clock Generation

The Clock Generation Unit can generate the system clock signal  $f_{SYS}$  for the XE162xM from a number of external or internal clock sources:

- External clock signals with pad voltage or core voltage levels
- External crystal or resonator using the on-chip oscillator
- On-chip clock source for operation without crystal/resonator
- Wake-up clock (ultra-low-power) to further reduce power consumption

The programmable on-chip PLL with multiple prescalers generates a clock signal for maximum system performance from standard crystals, a clock input signal, or from the on-chip clock source. See also **Section 4.6.2**.

The Oscillator Watchdog (OWD) generates an interrupt if the crystal oscillator frequency falls below a certain limit or stops completely. In this case, the system can be supplied with an emergency clock to enable operation even after an external clock failure.

All available clock signals can be output on one of two selectable pins.

![](_page_14_Picture_0.jpeg)

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Absolute sum of overload currents	$\Sigma  I_{\rm OV} $ SR	-	-	50	mA	not subject to production test
Digital core supply voltage for domain M <sup>8)</sup>	V <sub>DDIM</sub> CC	-	1.5	_		
Digital core supply voltage for domain 1 <sup>8)</sup>	V <sub>DDI1</sub> CC	-	1.5	-		
Digital supply voltage for IO pads and voltage regulators	$V_{\rm DDP}{ m SR}$	4.5	-	5.5	V	
Digital ground voltage	$V_{\rm SS}{\rm SR}$	_	0	_	V	

## Table 12 Operating Conditions (cont'd)

To ensure the stability of the voltage regulators the EVRs must be buffered with ceramic capacitors. Separate buffer capacitors with the recomended values shall be connected as close as possible to each V<sub>DDIM</sub> and V<sub>DDI1</sub> pin to keep the resistance of the board tracks below 2 Ohm. Connect all V<sub>DDI1</sub> pins together. The minimum capacitance value is required for proper operation under all conditions (e.g. temperature). Higher values slightly increase the startup time.

2) Use one Capacitor for each pin.

- This is the reference load. For bigger capacitive loads, use the derating factors listed in the PAD properties section.
- 4) The timing is valid for pin drivers operating in default current mode (selected after reset). Reducing the output current may lead to increased delays or reduced driving capability (C<sub>L</sub>).
- 5) The operating frequency range may be reduced for specific device types. This is indicated in the device designation (...FxxL). 80 MHz devices are marked ...F80L.
- 6) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range: V<sub>OV</sub> > V<sub>IHmax</sub> (I<sub>OV</sub> > 0) or V<sub>OV</sub> < V<sub>ILmin</sub> ((I<sub>OV</sub> < 0). The absolute sum of input overload currents on all pins may not exceed 50 mA. The supply voltages must remain within the specified limits. Proper operation under overload conditions depends on the application. Overload conditions must not occur on pin XTAL1 (powered by V<sub>DDIM</sub>).
- 7) An overload current  $(I_{OV})$  through a pin injects a certain error current  $(I_{INJ})$  into the adjacent pins. This error current adds to the respective pins leakage current  $(I_{OZ})$ . The amount of error current depends on the overload current and is defined by the overload coupling factor  $K_{OV}$ . The polarity of the injected error current is inverse compared to the polarity of the overload current that produces it. The total current through a pin is  $|I_{TOT}| = |I_{OZ}| + (|I_{OV}| K_{OV})$ . The additional error current may distort the input voltage on analog inputs.
- 8) Value is controlled by on-chip regulator

![](_page_15_Picture_0.jpeg)

Table 22	Flash	Parameters (	(cont'd)
		i alamotoro i	

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Number of erase cycles	N <sub>Er</sub> SR	-	-	15 000	cycle s	$t_{RET} \ge 5$ years; Valid for up to 64 user- selected sectors (data storage)
		-	-	1 000	cycle s	$t_{RET} \ge 20$ years

 All Flash module(s) can be erased/programmed while code is executed and/or data is read from only one Flash module or from PSRAM. The Flash module that delivers code/data can, of course, not be erased/programmed.

 Flash module 3 can be erased/programmed while code is executed and/or data is read from any other Flash module.

3) Value of IMB\_IMBCTRL.WSFLASH.

4) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This increases the stated durations noticably only at extremely low system clock frequencies.

Access to the XE162xM Flash modules is controlled by the IMB. Built-in prefetch mechanisms optimize the performance for sequential access.

Flash access waitstates only affect non-sequential access. Due to prefetch mechanisms, the performance for sequential access (depending on the software structure) is only partially influenced by waitstates.

![](_page_16_Picture_0.jpeg)

The timing in the AC Characteristics refers to TCSs. Timing must be calculated using the minimum TCS possible under the given circumstances.

The actual minimum value for TCS depends on the jitter of the PLL. Because the PLL is constantly adjusting its output frequency to correspond to the input frequency (from crystal or oscillator), the accumulated jitter is limited. This means that the relative deviation for periods of more than one TCS is lower than for a single TCS (see formulas and Figure 20).

This is especially important for bus cycles using waitstates and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective timeframe. The VCO output clock is divided by the output prescaler K2 to generate the system clock signal  $f_{SYS}$ . The number of VCO cycles is K2 × **T**, where **T** is the number of consecutive  $f_{SYS}$  cycles (TCS).

The maximum accumulated jitter (long-term jitter) D<sub>Tmax</sub> is defined by:

 $D_{\text{Tmax}}$  [ns] = ±(220 / (K2 ×  $f_{\text{SYS}}$ ) + 4.3)

This maximum value is applicable, if either the number of clock cycles T > ( $f_{SYS}$  / 1.2) or the prescaler value K2 > 17.

In all other cases for a timeframe of  $\mathbf{T} \times TCS$  the accumulated jitter  $D_T$  is determined by:

 $D_{T}$  [ns] =  $D_{Tmax} \times [(1 - 0.058 \times K2) \times (T - 1) / (0.83 \times f_{SYS} - 1) + 0.058 \times K2]$ 

 $f_{SYS}$  in [MHz] in all formulas.

Example, for a period of 3 TCSs @ 33 MHz and K2 = 4:

 $D_{max} = \pm (220 / (4 \times 33) + 4.3) = 5.97$  ns (Not applicable directly in this case!)

 $D_3 = 5.97 \times [(1 - 0.058 \times 4) \times (3 - 1) / (0.83 \times 33 - 1) + 0.058 \times 4]$ 

= 5.97 × [0.768 × 2 / 26.39 + 0.232]

Example, for a period of 3 TCSs @ 33 MHz and K2 = 2:

 $D_{max} = \pm(220 / (2 \times 33) + 4.3) = 7.63$  ns (Not applicable directly in this case!)

 $\begin{array}{l} \mathsf{D}_3 = 7.63 \times [(1 - 0.058 \times 2) \times (3 - 1) \ / \ (0.83 \times 33 - 1) + 0.058 \times 2] \\ = 7.63 \times [0.884 \times 2 \ / \ 26.39 + 0.116] \end{array}$ 

![](_page_17_Picture_0.jpeg)

![](_page_17_Figure_3.jpeg)

Figure 22 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration where the slave select signal is low-active and the serial clock signal is not shifted and not inverted.

![](_page_18_Picture_0.jpeg)

#### Debug via JTAG

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply;  $C_L$ = 20 pF.

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
TCK clock period	t <sub>1</sub> SR	50 <sup>1)</sup>	_	_	ns	2)
TCK high time	$t_2$ SR	16	-	-	ns	
TCK low time	t <sub>3</sub> SR	16	-	-	ns	
TCK clock rise time	t <sub>4</sub> SR	-	-	8	ns	
TCK clock fall time	t <sub>5</sub> SR	-	-	8	ns	
TDI/TMS setup to TCK rising edge	t <sub>6</sub> SR	6	-	_	ns	
TDI/TMS hold after TCK rising edge	t <sub>7</sub> SR	6	-	-	ns	
TDO valid from TCK falling edge (propagation delay) <sup>3)</sup>	t <sub>8</sub> CC	-	25	29	ns	
TDO high impedance to valid output from TCK falling edge <sup>4)3)</sup>	t <sub>9</sub> CC	-	25	29	ns	
TDO valid output to high impedance from TCK falling edge <sup>3)</sup>	<i>t</i> <sub>10</sub> CC	-	25	29	ns	
TDO hold after TCK falling edge <sup>3)</sup>	<i>t</i> <sub>18</sub> CC	5	-	-	ns	

Table 33JTAG Interface Timing for Upper Voltage Range

1) The debug interface cannot operate faster than the overall system, therefore  $t_1 \ge t_{SYS}$ .

2) Under typical conditions, the interface can operate at transfer rates up to 20 MHz.

3) The falling edge on TCK is used to generate the TDO timing.

4) The setup time for TDO is given implicitly by the TCK cycle time.

![](_page_19_Picture_0.jpeg)

Parameter	Symbol	Values			Unit	Note /	
		Min.	Тур.	Max.		Test Condition	
TCK clock period	t <sub>1</sub> SR	50 <sup>1)</sup>	-	-	ns	2)	
TCK high time	$t_2$ SR	16	-	-	ns		
TCK low time	$t_3$ SR	16	-	-	ns		
TCK clock rise time	t <sub>4</sub> SR	-	-	8	ns		
TCK clock fall time	t <sub>5</sub> SR	-	-	8	ns		
TDI/TMS setup to TCK rising edge	t <sub>6</sub> SR	6	-	-	ns		
TDI/TMS hold after TCK rising edge	t <sub>7</sub> SR	6	-	-	ns		
TDO valid from TCK falling edge (propagation delay) <sup>3)</sup>	t <sub>8</sub> CC	-	32	36	ns		
TDO high impedance to valid output from TCK falling edge <sup>4)3)</sup>	t <sub>9</sub> CC	-	32	36	ns		
TDO valid output to high impedance from TCK falling edge <sup>3)</sup>	<i>t</i> <sub>10</sub> CC	-	32	36	ns		
TDO hold after TCK falling edge <sup>3)</sup>	<i>t</i> <sub>18</sub> CC	5	-	-	ns		

## Table 34 JTAG Interface Timing for Lower Voltage Range

1) The debug interface cannot operate faster than the overall system, therefore  $t_1 \ge t_{SYS}$ .

2) Under typical conditions, the interface can operate at transfer rates up to 20 MHz.

3) The falling edge on TCK is used to generate the TDO timing.

4) The setup time for TDO is given implicitly by the TCK cycle time.

![](_page_20_Picture_0.jpeg)

#### Package and Reliability

## 5.2 Thermal Considerations

When operating the XE162xM in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The "Thermal resistance  $R_{\Theta JA}$ " quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 125 °C.

The difference between junction temperature and ambient temperature is determined by  $\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta,IA}$ 

The internal power consumption is defined as

 $P_{\text{INT}} = V_{\text{DDP}} \times I_{\text{DDP}}$  (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as  $P_{\text{IOSTAT}} = \Sigma((V_{\text{DDP}} \cdot V_{\text{OH}}) \times I_{\text{OH}}) + \Sigma(V_{\text{OL}} \times I_{\text{OL}})$ 

The dynamic external power consumption caused by the output drivers ( $P_{\text{IODYN}}$ ) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce  $V_{\text{DDP}}$ , if possible in the system
- Reduce the system frequency
- · Reduce the number of output pins
- Reduce the load on active output drivers